IT66121/IT66120
HDMI Tx Register Defintions v1.0

The registers are separated into three register banks:
Reg00 ~ Reg2F are accessible in any register bank.
Reg30~ RegFF are accessible in register bank0
Reg130~ Reg1BF are accessible in register bank1. These are HDMI packet registers.

Register banks are selected using Reg0F[1:0].
When Reg0F[1:0]=00, register bank 0 is active.
When Reg0F[1:0]=01, register bank1 is active.
Be careful to switch to the accurate register bank when you program registers.

The CEC function uses another slave address which is defined in Reg8D[7:0].
Before accessing CEC register, RegGateCRCLK in HDMI Reg0F[3] must be set 0 to enable CEC function.

Note: All reserved registers should not be written to non-default value except those used in the programming guide.

1. Registers in Bank 0

1.1. General Registers

Reg	Register Name	Bit	Definition	Default
00	Vender ID	7:0		0x54
01	Vender ID	7:0		0x49
02	Device ID	7:0		0x12
03	Revision ID	7:4		0x0
	Device ID	3:0		0x6
04	Reserved	7	Reserved for test function.	0
	Reserved	6		0
	RegSoftRefRst	5	Software RCLK reset.	0
	RegSoftARst	4	Software Audio clock base signal reset.	1
	REGSoftVRst	3	Software Video clock base signal reset.	1
	REGAudReset	2	Audio FIFO reset.	1
	Reserved	1		0
	REGHDCP_rst	0	HDCP reset.	0
05	REG_INTPol	7	0: INT active low 1: INT active high	0
	REG_INTIOMode	6	1: Open-Drain mode 0: Push-Pull Mode	1
	RegEnHDMIInt	5	0: Disable HDMI interrupt to IO 1: Enable HDMI interrupt to IO	1
	Reserved	4		0
	REGPDREFCNT[1:0]	3:2	00: REFCLK Div2 01: REFCLK Div4 10: REFCLK Div8 Dont set 11	00
	REGPDREFCLK	1	Reduce REFCLK frequency 1: Reduce 0: Normal	0
	RegPDTxCLK	0	1: TxCLK power down 0: TxCLK active	0
06	RInt_AudioOvFlwStus	7	R, Reset by REGAudReset	X
	Reserved	6	R	X
	RDDC_Stus_NoACK	5	R	X

	Rint_DDCFIFOErr	4	R, Reset by RDDC_Req=0x9 REG_MastersSel=1	X
	Reserved	3	R	X
	RInt_DDCBusHang	2	R, Reset by RDDC_Req=0xF REG_MastersSel=1 REG_MasterROM=0	X
	RInt_RxSENStus	1	R, Reset by REG_RxSENClr	X
	RInt_HPDStus	0	R, Reset by REG_HPDClr	X
07	RInt_Pkt3DStus	7	R, Reset by REG_Pkt3DClr	X
	RInt_VidUnstableStus	6	R, Reset by REG_VidUnStaleClr	X
	RInt_PktACPStus	5	R, Reset by REG_PktACPClr	X
	RInt_PktNullStus	4	R, Reset by REG_PktNullClr	X
	RInt_PktGenStus	3	R, Reset by REG_PktGenCr	X
	RInt_KSVListChkStus	2	R, Reset by REG_KSVListChkClr	X
	RInt_AuthDoneStus	1	R, Reset by REG_AuthenDoneClr	X
	RInt_AuthFailStus	0	R, Reset by REG_AuthFailClr	X
08	Reserved	7		X
	Rint_AudCTSStus	6	R , Reset by REG_AudCTSClr	X
	RInt_VSyncStus	5	R, Reset by REG_VsyncClr	X
	RInt_VidStableStus	4	R, Reset by REG_VidStaleClr	X
	RInt_PktMpgStus	3	R, Reset by REG_PktMpgClr	X
	Reserved	2	R	X
	RInt_PktAudStus	1	R, Reset By REG_PktAudClr	X
	RInt_PktAVIStus	0	R, Reset by REG_PktAVIClr	X
Interrupt Mask Registers				
09	REG_AudioOvFlwMask	7	1: disable this interrupt. 0: Enable this interrupt	1
	Reserved	6		1
	REG_DDCNoACKMask	5		1
	REG_DDCFIFOErrMask	4		1
	Reserved	3		1
	REG_DDCBusHangMask	2		1
	REG_RxSENMask	1		1
	REG_HPDMask	0		1
0A	REG_PktAVIMask	7		1
	REG_VidUnStableMask	6		1
	REG_PktACPMask	5		1
	REG_PktNullMask	4		1
	REG_PktGenMask	3		1
	REG_KSVListChkMask	2		1
	REG_AuthDoneMask	1		1
	REG_AuthFailMask	0		1
0B		7		1
	REG_Pkt3DMask	6		1
	REG_AudCTSMask	5		1
	REG_VsyncMask	4		1
	REG_VidStableMask	3		1
	REG_PktMpgMask	2		1
	Reserved	1		1
	REG__PktAudMask	0		1
Interrupt Clear				
0C	REG__PktACPClr	7	1: Clear the interrupt	0
	REG__PktNullClr	6		0
	REG__PktGenClr	5		0

	REG__KSVListChkClr	4		0
	REG__AuthDoneClr	3		0
	REG__AuthFailClr	2		0
	REG__RxSENClr	1		0
	REG__HPDClr	0		0
0D	REG__VsyncClr	7	1: Clear the interrupt	0
	REG__VidStableClr	6		0
	REG__PktMpgClr	5		0
	Reserved	4		0
	REG__PktAudClr	3		0
	REG__PktAVIClr	2		0
	REG_Pkt3DClr	1		0
	REG__VidUnstableClr	0		0
System Status				
0E	RInt_FSMON	7	R. 1: Interrupt is active.	
	RHPDetect	6	R. Hot Plug Detect: 1: plug on. 0: plug off	
	RxSENDetect	5	R	
	TxVidStable	4	R. Video input status: 1: stable video input. 0: unstable video input.	
	RegCTSIntStep[1:0]	3:2	R/W	11
	Reg_AudCTSClr	1	Clear AduCTS interrupt	0
	Reg_IntActDone_	0	1: Make interrupt clear active. 0: Disable interrupt clear action	0
0F		7		
	RegGateRCLK	6	1: power down RCLK(for I2C)	0
	RegGateIACLK	5	1: power down IACLK (for audio fifo)	0
	RegGateTxCLK	4	1: power down Txclk (for CSC)	0
	RegGateCRCLK	3	1: power down CRCLK (for CEC)	1
		2		
	RegBankSel	1:0	00: Bank 0, reg00h~ regffh 01: Bank 1, reg130h ~ reg1ffh	0

1.2. System DDC Control Registers

Reg	Register Name	Bit	Definition	Default
10	REGGenCLKPulse[3:0]	7:4		0x9
	REGSoftDDC	3		0
	REGSoftDDCSCL	2		1
	REGSoftDDCSDA	1		1
	Reg_MasterSel	0	Switch HDCP controller or PC host to command the DDC port 0: HDCP 1: PC	0
11	RDDC_Header[7:0]	7:0	PC DDC request slave address: 0x74 when access Rx HDCP 0xA0 when access Rx EDID 0xA0/0xA2 when access EEPROM	
12	RDDC_ReqOffSet[7:0]	7:0	Register address	
13	RDDC_ReqByte[7:0]	7:0	Register R/W byte number	
14	RDDC_Segment[7:0]	7:0	EDID segment	
15	DDC_SDA	7	R. DDC SDA pin status	
	DDC_SCL	6	R. DDC SCL pin status	
		5		
		4		
	RDDC_Req[3:0]	3:0	PC DDC request command 0x0: Sequential Burst Read 0x2: Link check read 0x3: EDID read 0x4: AKSV write 0x5: Ainfo write 0x6: An write 0x9: DDC FIFO clear 0xA: GenerateSCL clock pulse 0xF: Abort DDC command.	
16	RDDC_Status[7:0]	7	Read Only. RDDC_Stus_Done 0: DDC is not complete 1: DDC transfer is complete	
		6	RDDC_Active	
		5	RDDC_Stus_NoACK 1: DDC has something error	
		4	RDDC_Stus_WaitBus 1: DDC has something error	
		3	RDDC_Stus_ArbiLose 1: DDC has something error	
		2	RDDC_FIFOFull	
		1	RDDC_FIFOEmpty	
		0	TxFIFO status VRValid	
17	RDDC_ReadFIFO	7:0	R. Read DDC FIFO content. There are 32 DDC FIFO, which can read back from the byte. See Fig. 1	
18		7:0		
19	REG_HDCPHeader	7:0		0x74
1A		7:0		
1B		7:6		
	REG_BusHoldT[5:0]	5:0	DDC Bus start/stop setup/hold time requirement	0x03
1C		7:2		
	ROM_Stus[1:0]	1	Read-Only.	

		1 0	TxFIFO status :over read TxFIFO status :over write	
1D	Reserved for IT6261			
1E	Reserved for IT6261			

1.3. HDCP Registers

Reg	Register Name	Bit	Definition	Default
1F	RAuthen_CS	7:1	R. Authentication FSM current state	
	Reg_AnGen	0	Write this bit 1 to enable Cipher Hardware generating a random number. Write 0 to stop the Cipher Hardware. The generated Random number can be read back from register 30~37	0
20	Reserved	7		0
	Reserved	6		
	Reserved	5		0
	Reserved	4		
	Reserved	3		1
	REGHDCPSyncDet	2	Enable HDCP 1.2 SyncDetect	0
	REGAEnable1p1Feature	1	Enable HDMI Tx HDCP1.1 Feature	0
	REGCPDesired	0	Write 1 to enable HDCP	0
21		7:1		
	Rauthen_Fire	7:0	Write 1 to stare HDCP authentication process	X
22		7:2		
	REGList_Fail	1	Write this bit when process KSVList Check interrupt Routine. Write 1 when KSV FIFO list check fail.	0
	REGList_Done	0	Write this bit when process KSVList Check interrupt routine. Write 1 when KSV FIFO list check pass	0
23~27	AKSV[39:0]	7:0	When RegEnSiPROM=0 : Reg23~Reg27 are Read Only registers for AKSV[39:0]	XX
28~2F	An	63:0	Random number used at HDCP Authentication.	XX
30~37	VgenAn	63:0	When RegEnSiPROM=0 : Reg28~2F are Read Only registers for VgenAn[63:0] These 8 bytes are generated random number. To generate random number, see Reg1F[0].	XX
38/39	Ari	15:0	Read only	XX
3A	Apj	7:0	Read only.	XX
3B~3F	BKSV[39:0]	39:0	When RegEnSiPROM=0 : Reg3B~3F are Read Only registers for BKSV[39:0]	XX
40	BRi[7:0]	7:0	Read only.	XX
41	BRi[15:8]	7:0	Read only.	XX
42	BPj[7:0]	7:0	Read only.	XX
43	Bcaps[7:0]	7	HDMI_Reserved	X
		6	HDCP Repeater capability.	X
		5	KSV FIFO ready.	X
		4	FAST. 1: the device supports 400KHz transfers.	X
		3	reserved. must be zero.	X
		2	reserved. must be zero.	X
		1	1: HDCP 1.1 Features. Support HDCP Enhanced encryption status signaling (EESS), Advance Cipher, and Enhanced Link Verification options.	X
		0	1: Fast reauthenticagtion. When set to 1, the receiver is capable of receiving	X

			(unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP receiver is active.	
44	Bstatus[7:0]	7	MAX_DEVS_EXCEEDED 1: more than 127 downstream devices or KSV fifo.	X
		6:0	DEVICE_COUNT Total number of attached downstream string devices.	X
45	Bstatus[15:8]	7	reserved 0.	X
		6	reserved 0.	X
		5	Reserved for future possible HDMI used.	X
		4	HDMI_Mode 1: HDMI mode. 0: DVI mode.	X
		3	MAX_CASCADE_EXCEEDED Topology error indicator. 1: more than seven levels of video repeater have been cascaded together.	X
		2:0	Three-bit repeater cascade depth.	X
46	RAuthenticated	7	Read Only	X
	RAuthFailStatus	6	Read Only. DDC HANG Timeout	-
		5	Read Only. Sync Detect Fail	-
		4	Read Only. Pj Link Integrity Check Fail	-
		3	Read Only. Ri Link Integrity Check Fail	-
		2	Read Only. R0 Link Integrity Check Fail	-
		1	Read Only. Invalid BKSV	-
		0	Read Only. DDC NACK Timeout	-
47	REGTimeLoMax[7:0]	7:0	Timer Reference.	0x00
48	REGTimeLoMax[15:8]	7:0	Timer Reference.	0x4A
49	REGTimeBaseSel	7:6	Ri/Pj Read Timer Reference switch (only when REGHDCPSyncDet=1) 00: REGTimeLowMax 01: REGTimeLowMax/32 10: REGTimeLowMax/64 11: REGTimeLoxMax/128;	0x0
	REGI2CnakMax[1:0]	5:4	Timer Reference.	0x2
		3:2		
	REGTimeLoMax[17:16]	1:0	Timer Reference.	0x2
4A	REGTimeRetryAuthen[7:0]	7:0	Timer Reference.	0xC8
4B		7		
	Reserved	6		0
	REGHDCPTest[1:0]	5:4	For test only (WP)	01
	Reserved	3:0		0x3
4C	Reserved	7:0		0x2A
4D	Reserved	7:0		0xA5
4E		7:2		
	Reserved	1		
		0		
4F		7:4		
	REGEnHDCPAutoMute	3	Auto-AVMute before HDCP authentication done 0: Disable, 1: Enable	1
	REGEnSyncDet2FailInt	2	HDCP 1.2 Sync. detection fail to trigger authentication fail interrupt 0: Disable, 1: Enable	0

	REGEnRiChk2DoneInt	1	Ri/Pj check pass to trigger authentication done interrupt 0: Disable, 1: Enable	1
	REGEnAutoReAuthen	0	HW automatically fire authentication when authentication fail. 0: Disable, 1: Enable	1
50		7:4		
	REGPrevRiSel	3	See RegPrevRi registers reg56, reg57	0
	SHASel[2:0]	2:0	See SHA_Rd_ByteX registers below	
51	SHA_Rd_Byte1[7:0]	7:0	V0h[7:0] when SHASel=000 V1h[7:0] when SHASel=001 V2h[7:0] when SHASel=010 V3h[7:0] when SHASel=011 V4h[7:0] when SHASel=100 Mi [7:0] when SHASel=101	
52	SHA_Rd_Byte2[7:0]	7:0	V0h[15:8] when SHASel=000 V1h[15:8] when SHASel=001 V2h[15:8] when SHASel=010 V3h[15:8] when SHASel=011 V4h[15:8]when SHASel=100 Mi[15:8] when SHASel=101	
53	SHA_Rd_Byte3[7:0]	7:0	V0h[23:16] when SHASel=000 V1h[23:16] when SHASel=001 V2h[23:16] when SHASel=010 V3h[23:16] when SHASel=011 V4h[23:16] when SHASel=100 Mi[23:16] when SHASel=101	
54	SHA_Rd_Byte4[7:0]	7:0	V0h[31:124] when SHASel=000 V1h[31:24] when SHASel=001 V2h[31:24] when SHASel=010 V3h[31:24] when SHASel=011 V4h[31:24] when SHASel=100 Mi[31:24] when SHASel=101	
55	Aksv_Rd_Byte5[7:0]	7:0	Mi[39:32] when SHASel=000 Mi[47:39] when SHASel=001 Mi[55:48] when SHASel=010 Mi[63:56] when SHASel=011	
56	Prev_Ri[7:0]	7:0	Prev_Ari[7:0] when REGPrevRiSel=0 Prev_Bri[7:0] when REGPrevRiSel=1	
57	Prev_Ri[15:8]	7:0	Prev_Ari[15:8] when REGPrevRiSel=0 Prev_Bri[15:8] when REGPrevRiSel=1	

1.4. Clock Control Registers

Reg	Register Name	Bit	Definition	Default
58	REGMCLKSamp	7	1: use external MCLK sampling	0
	REGOSCLKSel	6:5		0
	REGAutoOSCLK	4	Auto over-sampling clock 1: auto 0: user defined	1
	REGMCLKFreq[1:0]	3:2	External MCLK Frequency 00: 1x128 Fs 01: 2x128 Fs 10: 4x128 Fs 11: 8x128 Fs	0
	REGMCLKCTS	1	0: SPDIF CTS count from internal MCLK 1: SPDIF CTS count from external MCLK	0
	REGAutoIPCLK	0	Auto IPCLK selection 1: auto 0: user defined	1
59	REGManualPLLPR	7:6		0
	REGEnTxCnt	5	Enable TxCLK to count REFCLK 1 : enable 0 : disable	0
	RegDisLockPR	4		0
	REGVidLatEdge	3	Video Data Latch Edge	0
	RegNoAud2Mute	2	Force Audio Mute when no audio input 0: Disable, 1: Enable	0
	Reserved	1:0		
5A	REGSPDIFRst	7	SPDIF decoder function reset 0: Normal operation, 1: Reset	0
		6:4		
	RegACLKPWD	3	0: normal operation 1: power-down ACLK/NIACLK/GIACLK (RegAudioEn[3:0] must be “0000” in power-down)	0
	RegSCLKPWD	2	0: normal operation 1: power-down SCLK domain	0
	RegIACLKAutoPWD	1	1 : auto power down (depend on REGAudioEn[3:0]) , 0 : manual power down (Default value = 1)	1
	RegTxCLKAutoPWD	0	1 : auto power down (depend on Reg_CSCSel[1:0]) , 0 : manual power down (Default value = 1)	1
5B	RegOSFreqNum[13:6]	7:0	Read back RegOSFreqNum[13:0] When RegFixedOSFreq=1 Else Read back RefOSFreqCnt[13:0]	
5C	RegFixedOSFreq	7	Read back RegOSFreqNum[13:0] When RegFixedOSFreq=1 Else Read back RefOSFreqCnt[13:0]	0
	RegEnhSpdifOS	6		0
	RegOSFreqNum[5:0]	5:0		
5D				
5E	TxCLKCnt[7:0]	7:0	Ring OSC counter read back. Read only. Pixel clock cycle counted during 256 internal oscillator clock period. Reference register 0x59, D[5]: REGEnTxCnt.	XX
5F	IP_LOCK	7	Read only. Internal pixel clock PLL Lock. 1: PLL lock. 0: PLL fail to lock.	X

	XP_LOCK	6	Read only. TMDS clock PLL Lock 1: PLL lock. 0: PLL fail to lock.	X
	OSFreqLock	5	SPDIF over-sampling lock flag	X
	RefNoAudFlag	4	No Audio Input Interrupt flag	X
	TxCLKCnt[11:8]	3:0	R. Ring OSC counter read back.	X
60	RefAudFreqNum[7:0]	7:0	Read-Only. Audio sampling frequency counter	XX

1.5. AFE Control Registers

Reg	Register Name	Bit	Definition	Default
61		7:6		
	REG_DRV_PWD	5	Reset signal for HDMI_TX_DRV. 1: all flip-flops in the transmitter are reset while all other analog parts are powered off.	0
	REG_DRV_RST	4	Reset signal for HDMI_TX_DRV. 1: all flip-flops in the transmitter are reset.	1
		3		
	REG_DRV_PDRXDET	2		0
	REG_DRV_TERMON	1		0
		0		
62	REG_XP_GAINBIT	7	Video frequency band selection 0: when output TMDS clock frequency <80MHz 1: when output TMDS clock frequency >80MHz	1
	REG_XP_PWDPLL	6	Power down signal for TMDSTXPLL18VA0 0: Normal operation 1: TMDSTXPLL18VA0 is powerdowned	0
	REG_XP_ENI	5	1: the charge pump current of TMDSTXPLL18VA0 is increased.	0
	REG_XP_ER0	4	Adjust filter parameters of TMDSTXPLL18VA0 0: base filter resistance value (>80MHz) 1: increased filter resistance value (<80MHz)	0
	REG_XP_RESETB	3	Low-active reset signal for TMDSTXPLL18VA0 0: TMDSTXPLL18VA0 is reset. 1: Normal operation	1
	REG_XP_PWDI	2	0: TXPLL current bias is not in powerdown mode. 1: TXPLL current bias in powerdown mode, no current source available for all other blocks such as IPLL. Normally, PWDI should always be set to 0.	0
		1		
		0		0
63		7		0
	REG_IP_BYPASS	6		0
	REG_DRV_ISW	5:3		011
		2:0		000
64	REG_IP_GAINBIT	7	Video frequency band selection 0: when PCLKIN<80MHz 1: when PCLKIN>80MHz	1
	REG_IP_PWDPLL	6	Powerdown signal for TMDSIPLL18VA0 0: Normal operation 1: TMDSIPLL18VA0 is powerdowned	0
	REG_IP_CKSEL	5:4		01
	REG_IP_ER0	3	Adjust filter parameters of TMDSIPLL18VA0 0: base filter resistance value (>80MHz) 1: increased filter resistance value (<80MHz)	0
	REG_IP_RESETB	2	Low-active reset signal for TMDSIPLL18VA0 0: TMDSIPLL18VA0 is reset. 1: Normal operation	1
	REG_IP_ENC	1		0
	REG_IP_EC1	0	Adjust filter parameters of TMDSIPLL18VA0 0: when PCLKIN>80MHz 1: when PCLKIN<80MHz	0
65		7		

		6		
		4:5		
		3:2		
	REG_RING_SLOW	1	1: slow down the frequency of RING_CK	0
	REG_RING_FAST	0	1: speed up the frequency of RING_CK	0
66	REG_DRV_HS	7		0
	Reserved	6		0
	Reserved	5		0
	Reserved	4:0		00000
67	Reserved	7		0
	Reserved	6		0
		5:0		
68	Reserved	7:5		000
	REG_XP_EC1	4	0: when output TMDS clock frequency >80MHz 1: when output TMDS clock frequency <80MHz	0
	REG_XP_DEK	3		0
	REG_IP_DEK	2		0
	REG_IP_ER1	1	0: will not increase filter resistance 1: will increase filter resistance	0
	REG_IP_DISVC	0		0
69	REG_PAT_RSTB	7	HDMI1.3 TX AFE pattern generator reset (active low)	0
		6		
	Reserved	5		1
	Reserved	4		1
		3:2		
	Reserved	1:0		00
6A	REG_XP_TEST[7:0]	7:0		0x00
6B ~6F				

1.6. Input Data Processing Registers

Reg	Register Name	Bit	Definition	Default
Input Data Format Registers				
70	Reg_InColMod[1:0]	7:6	00: RGB mode 01: YUV422 mode 10: YUV444 mode	00
	Reg_PCLKDiv2	5	0: IO latch clock = TxCLK 1: IO latch clock = 1/2*TxCLK	0
	Reg_2x656Clk	4	1: CCIR656 mode(YUV422, 8/12 bit mode) 0: non- CCIR656 mode	0
	Reg_SyncEmb	3	1: Sync Embedded mode 0: Sync Sep mode	0
	Reg_InDDR	2	1: Input DDR 0: Input SDR	0
	Reg_InClkDly	1:0	Input PCLK delay	00
71	RegXPStableTime[1:0]	7:6	XP_Lock stable time 01: 50us, 10:100us, others:75us	00
	RegEnXPLockChk	5	Enable to Check XP_lock for TX fifo reset 0: disable. 1: enable	0
	RegEnPLLBufRst	4	Enable to reset TX fifo when PLL unlock 0: disable. 1: enable	0
	RegEnFFAutoRst	3	TX fifo auto reset enable 0: disable, 1: enable	1
	Reg_TxIOMod	2	0: 10/12-bit YCbCr422 sequential IO mode 1: 10/12-bit YCbCr422 non-sequential IO mode	0
	Reg_TxFFRst	1	1: Reset TxFIFO	0
		0		0
72		7		
		6		
		5		
		4		
		3		
	Reg_BTAFmt	2	1: YCbCr422 BTA-T1004 format	0
	Reg_CSCSel[1:0]	1:0	00 : No color space converstion. 10: RGB to YUV 11: YUV to RGB	00
Color Space Conversion				
73	Reg_YoffSet	7:0	Y blank level	0x10
74	Reg_CoffSet[7:0]	7:0	C blank level	0x80
75	Reg_RGBOffSet[7:0]	7:0	R/G/B blank level	0x00
76	Reg_Matrix11V[7:0]	7:0	Color space conversion Matrix	
77		7:5		
	Reg_Matrix11V[13:8]	4:0		
78	Reg_Matrix12V[7:0]	7:0	Color space conversion Matrix	
79		7:6		
	Reg_Matrix12V[13:8]	5:0		
7A	Reg_Matrix13V[7:0]	7:0	Color space conversion Matrix	
7B		7:6		
	Reg_Matrix13V[13:8]	5:0		
7C	Reg_Matrix21V[7:0]	7:0	Color space conversion Matrix	
7D		7:6		
	Reg_Matrix21V[13:8]	5:0		
7E	Reg_Matrix22V[7:0]	7:0	Color space conversion Matrix	
7F		7:6		

	Reg_Matrix22V[13:8]	5:0		
80	Reg_Matrix23V[7:0]	7:0	Color space conversion Matrix	
81		7:6		
	Reg_Matrix23V[13:8]	5:0		
82	Reg_Matrix31V[7:0]	7:0	Color space conversion Matrix	
83		7:6		
	Reg_Matrix31V[13:8]	5:0		
84	Reg_Matrix32V[7:0]	7:0	Color space conversion Matrix	
85		7:6		
	Reg_Matrix32V[13:8]	5:0		
86	Reg_Matrix33V[7:0]	7:0	Color space conversion Matrix	
87		7:6		
	Reg_Matrix33V[13:8]	5:0		
88~8C				
8D	RegCECSlvAdr	7:0	PCI2C CEC slave address	0xC8
8E	RegReservedA	7:0		0x00
8F	RegReservedB	7:0		0x00

1.7. Pattern Generation / Sync/ DE Generation Registers

Reg	Register Name	Bit	Definition	Default
Pattern Sync/DE Generation Registers				
90	Reg_PGHTotal[3:0]	7:4	PG Horizontal Total[3:0] When Reg_PGEn=1 or Reg_DEOnlyIn=1, this is Horizontal Total When Reg_GenSync=1 or Reg_SyncEmb=1 this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_HTotal[3:0] when(RegA8[3]='1') else Reg_PGHTotal[3:0]	00
	RegGenSync	3	1 : Instead of the H/V sync input,. HDMITx will Generate Sync for HDMI output 0:The H/V sync input received are used for HDMI output	0
	RegVSPol	2	Generated Vertical Sync Polarity when RegGenSync=1 or Reg_PGEn=1 1: active high. 0: active low. Read Value <= Rec_VSPol when(RegA8[3]='1') else Reg_VSPol;	0
	RegHSPol	1	Generated Horizontal Sync Polarity when RegGenSync=1 or Reg_PGEn=1 . 1: active high. 0: active low. Read Value <= Rec_HSPol when(RegA8[3]='1') else Reg_HSPol;	0
	Reg_GenDE	0	DE generation Enable 1 : Instead of the DE sync input,. IT6613 will Generate DE for HDMI output 0:The DE input received are used for HDMI output	0
91	Reg_PGHTotal[11:4]	7:0	PG Horizontal Total[11:4] When Reg_PGEn=1 or Reg_DEOnlyIn=1, this is Horizontal Total When Reg_GenSync=1 or Reg_SyncEmb=1 this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_HTotal[11:4] when(RegA8[3]='1') else Reg_PGHTotal[11:4];	XX
92	Reg_PGHDES[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG Horizontal Display Start; Low Byte. Read Value <= Rec_HDES[7:0] when(RegA8[3]='1') else Reg_PGHDES[7:0]	XX
93	Reg_PGHDEE[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG Horizontal Display End; Low Byte. Read Value <= Rec_HDEE[7:0] when(RegA8[3]='1') else Reg_PGHDEE[7:0]	XX
94	Reg_PGHDEE[11:8]	7:4	When Reg_GenDE=1 or Reg_PGEn=1, this nibble is PG Horizontal Display End ; High nibble. Read Value <= Rec_HDEE[11:8] when(RegA8[3]='1') else Reg_PGHDEE[11:8];	X
	Reg_PGHDES[11:8]	3:0	When Reg_GenDE=1 or Reg_PGEn=1, this nibble is PG Horizontal Display Start ; High nibble. Read Value <= Rec_HDES[11:8] when(RegA8[3]='1') else Reg_PGHDES[11:8];	X

95	Reg_PGHRS[7:0]	7:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this byte is PG Horizontal Sync Start; Low Byte. Read Value <= Rec_HSW[7:0] when(RegA8[3]='1') else Reg_PGHRS[7:0];	XX
96	Reg_PGHRE[7:0]	7:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this byte is PG Horizontal Sync End; Low Byte.	XX
97	Reg_PGHRE[11:8]	7:4	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG Horizontal Sync End ; High nibble.	X
	Reg_PGHRS[11:8]	3:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG Horizontal Sync Start ; High nibble. Read Value <= Rec_HSW[11:8] when(RegA8[3]='1') else Reg_PGHRS[11:8];	X
98	Reg_PGVTotal[7:0]	7:0	PG Vertical Total. When Reg_PGEn=1 or Reg_DEOnlyIn=1, this is Vertical Total Read Value <= Rec_VTotal[7:0] when(RegA8[3]='1') else Reg_PGVTotal[7:0];	XX
99		7:4		
	Reg_PGVTotal[11:8]	3:0	When Reg_PGEn=1 or Reg_DEOnlyIn=1, this nibble is PG Vertical Total; High nibble. Read Value <= Rec_VTotal[11:8] when(RegA8[3]='1') else RegPGVTotal[11:8];	X
9A	Reg_PGVDES[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG Vertical Display Start; Low Byte. Read Value <= Rec_VDES[7:0] when(RegA8[3]='1') else Reg_PGVDES[7:0];	XX
9B	Reg_PGVDEE[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG Vertical Display End; Low Byte. Read Value <= Rec_VDEE[7:0] when(RegA8[3]='1') else Reg_PGVDEE[7:0];	XX
9C	Reg_PGVDEE[11:8]	7:4	When Reg_GenDE=1 or Reg_PGEn=1, this nibble is PG Vertical Display End; High nibble. Read Value <= Rec_VDEE[11:8] when(RegA8[3]='1') else Reg_PGVDEE[11:8];	X
	Reg_PGVDES[11:8]	3:0	When Reg_GenDE=1 or Reg_PGEn=1, this nibble is PG Vertical Display Start; High nibble. Read Value <= Rec_VDES[11:8] when(RegA8[3]='1') else Reg_PGVDES[11:8];	X
9D	Reg_PGVDES2nd[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG 2nd Field Vertical Display Start; Low Byte. Read Value <= Rec_VDES2nd[7:0] when(RegA8[3]='1') else Reg_PGVDES2nd[7:0];	XX
9E	Reg_PGVDEE2nd[7:0]	7:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG 2nd Field Vertical Display End; Low Byte. Read Value <= Rec_VDEE2nd[7:0] when(RegA8[3]='1') else Reg_PGVDEE2nd[7:0];	XX
9F	Reg_PGVDEE2nd[11:8]	7:4	When Reg_GenDE=1 or Reg_PGEn=1, this nibble is PG 2nd Field Vertical Display Start; High nibble. Read Value <= Rec_VDEE2nd[11:8] when(RegA8[3]='1') else Reg_PGVDEE2nd[11:8];	X

	Reg_PGVDES2nd[11:8]	3:0	When Reg_GenDE=1 or Reg_PGEn=1, this byte is PG 2nd Field Vertical Display End; High nibble. Read Value <= Rec_VDES2nd[11:8] when(RegA8[3]='1') else Reg_PGVDES2nd[11:8];	X
A0	Reg_PGVRS[7:0]	7:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this byte is PG Vertical Sync Start; Low Byte.	XX
A1	Reg_PGVRE[3:0]	7:4	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG Vertical Sync Ends; Low nibble. Read Value <= Rec_VSW[3:0] when(RegA8[3]='1') else Reg_PGVRE[3:0];	X
	Reg_PGVRS[11:8]	3:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG Vertical Sync Start; High nibble.	X
A2	Reg_PGVRS2nd[7:0]	7:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this byte is PG 2nd Field Vertical Sync Start; Low Byte. Read Value <= Rec_VRS2nd[7:0] when(RegA8[3]='1') else Reg_PGVRS2nd[7:0];	XX
A3	Reg_PGVRE2nd[3:0]	7:4	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG 2nd Field Vertical Sync Ends; Low nibble. Read Value <= Rec_VSW2nd[3:0] when(RegA8[3]='1') else Reg_PGVRE2nd[3:0];	X
	Reg_PGVRS2nd[11:8]	3:0	When Reg_GenSync=1 or Reg_PGEn=1 or Reg_SyncEmb=1 or Reg_DEOnlyIn=1, this nibble is PG 2nd Field Vertical Sync Start; High nibble. Read Value <= Rec_VRS2nd[11:8] when(RegA8[3]='1') else Reg_PGVRS2nd[11:8];	X
A4	Reg_PGEn2ndVRRise[7:0]	7:0	When Reg_PGEn=1 or Reg_DEOnlyIn=1 and REG_PGInterlaced=1, this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_2ndVRRise[7:0] when(RegA8[3]='1') else Reg_PGEn2ndVRRise[7:0];	xx
A5		7:6		
	Reg_DEOnlyIn	5	When Reg_DEOnlyIn=1 , don't care input vsync and hsyc	0
	Reg_PGInterlaced	4	When Reg_PGEn=1 and REG_PGInterlaced=1, PGEn output interlaced mode Read Value <= Rec_Interlaced when(RegA8[3]='1') else Reg_PGInterlaced;	0
	Reg_PGEn2ndVRRise[11:8]	3:0	When Reg_PGEn=1 or Reg_DEOnlyIn=1 and REG_PGInterlaced=1 ,this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_2ndVRRise[11:8] when(RegA8[3]='1') else Reg_PGEn2ndVRRise[11:8];	x
A6	Reg_PGVRE2nd[7:4]	7:4	When Reg_GenSync=1 or Reg_PGEn=1, this nibble is PG 2nd Field Vertical Sync Ends high nibble. Read Value <= Rec_VSW2nd[7:4] when(RegA8[3]='1') else Reg_PGVRE2nd[7:4];	

	Reg_PGVRE[7:4]	3:0	When Reg_GenSync=1 or Reg_PGEn=1, this nibble is PG Vertical Sync Ends high nibble. Read Value <= Rec_VSW[7:4] when(RegA8[3]='1') else Reg_PGVRE[7:4];	
A7				
Pattern Generator Registers				
	Reg_PGVMD [1:0]	7:6	Vertical Pattern Mode 00: Gradient Mode 01: Inversion Mode 1x: Line Mode	00
	Reg_PGHMD[1:0]	5:4	Horizontal Pattern Mode 00: Gradient Mode 01: Inversion Mode 1x: Line Mode	00
A8	Reg_VHTimeRec	3	Video H/V status register read back	0
	Reg_PGVRep2	2	Vertical Repeat 1: value change every 2 pixels 0: value change every pixel	0
	Reg_PGHRep2	1	Horizontal Repeat 1: value change every 2 pixels 0: value change every pixel	0
	Reg_PGEn	0	1: Enable Pattern Generation 0: Disable Pattern Generation	0
		7		
	Reg_EnPatMux	6	Internal Pattern Mux function 0: Disable, 1: Enable	0
	Reg_PGSelB[1:0]	5:4	B/Cb color select 00: Select pattern generated value. 01: always 0x00 10: always 0x80 11 always 0xFF	
A9	Reg_PGSelG[1:0]	3:2	B/Y color select 00: Select pattern generated value. 01: always 0x00 10: always 0x80 11 always 0xFF	
	Reg_PGSelR[1:0]	1:0	R/Cr color select 00: Select pattern generated value. 01: always 0x00 10: always 0x80 11 always 0xFF	
AA	Reg_PGColR[7:0]	7:0	The initial R/Cr value of pattern generation.	
AB	Reg_PGColG[7:0]	7:0	The initial G/Y value of pattern generation.	
AC	Reg_PGColB[7:0]	7:0	The initial B/Cb value of pattern generation.	
AD	Reg_PGColBlank[7:0]	7:0	Value during blank interval	
AE	Reg_PGColBlankY[7:0]	7:0	Value during blank interval.	
AF	Reg_PGCHInc[7:0]	7:0	Horizontal Color Value Increment in Gradient Mode.	
B0	Reg_PGCVInc[7:0]	7:0	Vertical Color Value Increment in Gradient Mode.	
B1		7		
	Reg_PGHRE[12]	6	When Reg_GenSync=1 or Reg_PGEn=1, this bit is PG Horizontal Sync End Bit[12].	X
		5		

	Reg_PGHRS[12]	4	When Reg_GenSync=1 or Reg_PGEn=1, this bit is PG Horizontal Sync Start Bit[12]. Read Value <= Rec_HSW[12] when(RegA8[3]='1') else Reg_PGHRS[12];	X
		3		
	Reg_PGHDEE[12]	2	When Reg_GenDE=1 or Reg_PGEn=1, this bit is PG Horizontal Display End Bit[12]. Read Value <= Rec_HDEE[12] when(RegA8[3]='1') else Reg_PGHDEE[12];	X
		1		
	Reg_PGHDES[12]	0	When Reg_GenDE=1 or Reg_PGEn=1, this bit is PG Horizontal Display Start Bit[12]. Read Value <= Rec_HDES[12] when(RegA8[3]='1') else Reg_PGHDES[12];	X
B2		7:4		
		3		
	Reg_PGEn2ndVRRise[12]	2	When Reg_PGEn=1 and REG_PGInterlaced=1 ,this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_2ndVRRise[12] when(RegA8[3]='1') else Reg_PGEn2ndVRRise[12];	X
		1		
	Reg_PGHTotal[12]	0	PG Horizontal Total[12] When Reg_PGEn=1, this is Horizontal Total Bit[12] When Reg_GenSync=1 this define the location of the 2nd Vsync Rise edge at the Horizontal line. Read Value <= Rec_HTotal[12] when(RegA8[3]='1') else Reg_PGHTotal[12];	X
B3 ~ BE				
BF		7:4		
	Reg_PackSwap	3	1: R/B or Cr/Cb swap after data packing	0
	Reg_LMSwap	2	1: video channel MSB/LSB swap	0
	Reg_YCSwap	1	1: input Y/C component swap enable	0
	Reg_RBSwap	0	1: input R/B component swap enable	0

1.8. HDMI Control Registers

Reg	Register Name	Bit	Definition	Default
C0		7:1		
	REGHDMIMode	0	Set TX Mode 0: DVI mode 1: HDMI mode	0
C1	VAVMuteSts	7	Read Only. AVMute status	-
		6:2		
	REGBlueScrMute	1	1: Set blue screen output when AVMute=1 0: Set black screen output when AVMute=1	0
	REGAVMute	0	Set AVMute 0: not AVMute 1: AVMute	1
C2	Reserved	7	Reserved for 6623	
	RegEnVidBlack	6	Enable video black source	0
	Reserved	5:0		
C3	Reserved	7:5		
	REGOESSCycle[4:0]	4:0	OESS cycles period. The keep_out clock cycle in DVI mode. For definition of keep_out, please reference HDCP1.3a specification Appendix D.	0x08
C4		7:1		
	Reserved	0		0
C5	Reserved	7:6		
	RegEnhAudCts	5		0
	RegEnAudOff	4		0
	Reserved	3		0
	Reserved	2		1
	REGPktAudNCTSSel	1	Audio CTS selection 0: hardware auto count 1: user defined	0
	Reserved	0		0
C6		7:2		
	REGPktGenCtrlRpt	1	Repeat General Control packet 0: send once 1: one for each field	0
	REGPktGenCtrlEn	0	Enable General Control packet 0 : disable 1: enable	0
C7 ~ C8				
C9		7:2		
	REGPktNullRpt	1	Repeat Null packet 0: send once 1: one for each field	0
	REGPktNullEn	0	Enable Null packet 0: disable 1: enable (mutual exclusive with ACP/ISRC1/ISRC2 packet)	0
CA		7:2		
	REGPktACPRpt	1	Repeat ACP packet 0: send once 1: one for each field	0

	REGPktACPEn	0	Enable ACP packet 0: disable 1: enable (mutual exclusive with Null/ISRC1/ISRC2 packet)	0
CB ~ CC				
CD		7:2		
	REGPktAVIInfoRpt	1	Repeat AVI InfoFrame packet 0: send once 1: one for each field	0
	REGPktAVIInfoEn	0	Enable AVI InfoFrame packet 0: disable 1: enable	0
CE		7:2		
	REGPktAudInfoRpt	1	Repeat Audio InfoFrame packet 0: send once 1: one for each field	0
	REGPktAudInfoEn	0	Enable Audio InfoFrame packet 0: disable 1: enable	0
CF				
D0		7:2		
	REGPktMpgInfoRpt	1	Repeat MPEG InfoFrame packet 0: send once 1: one for each field	0
	REGPktMpgInfoEn	0	Enable MPEG InfoFrame packet 0: disable 1: enable	0
D1	RefVidParaChgSts[3:0]	7:4	Video parameter change status (read only) 0x0: no change	0x-
		3		0
		2		1
		1		0
		0		0
D2		7:2		
	REGPkt3DinfoRpt	1	Repeat 3D InfoFrame packet 0: send once 1: one for each field	0
	REGPk3DinfoEn	0	Enable 3D InfoFrame packet 0: disable 1: enable	0
D3 ~ D6				
D7	RegEnPCLKCnt	7	1 Enable PCLK counter	0
	RegPreDivSel[2:0]	6:4	Extra PCLK division counter	000
	RPCLKCnt[11:8]	3:0	Read-Only. PCLK frequency counter	X
D8	RPCLKCnt[7:0]	7:0		XX

1.9. Audio Channel Regisers

Reg	Register Name	Bit	Definition	Default
E0	REGAudSWL[1:0]	7:6	00: 16 bits 01: 18 bits 10: 20 bits 11: 24 bits	11
	REGSPDIFTC	5	Time period length to identify whether SPDI input is locked. 1: long period 0: shorter period	0
	REGAudSel	4	0: I2S 1: SPDIF	0
	REGAudioEn	3:0	Enable Audio Source [0] for audio source 0 [1] for audio source 1 [2] for audio source 2 [3] for audio source 3 0: disable 1: enable	0
E1		7		
	REGAudFullPkt	6	Enable audio full packet mode 0: not full packet mode 1: full packet mode	1
	REGAudLatEdge	5	0: use rising edge to sample WS and I2S 1: use falling edge to sample WS and I2S	0
	REGAudFmt[4:0]	4:0	REGAudFmt[0] 0: Standard I2S 1: 32-bit I2S REGAudFmt[1] 0: Left-justified 1: Right-justified REGAudFmt[2] 0: Data delay 1T correspond to WS 1: No data delay correspond to WS REGAudFmt[3] 0: WS=0 is left channel 1: WS=0 is right channel REGAudFmt[4] 0: MSB shift first 1: LSB shift first	0x01
E2	REGFifo3Sel	7:6	Audio FIFO 3 source selection 00: from audio source 0 01: from audio source 1 10: from audio source 2 11: from audio source 3	E4
	REGFifo2Sel	5:4	Audio FIFO 2 source selection 00: from audio source 0 01: from audio source 1 10: from audio source 2 11: from audio source 3	
	REGFifo1Sel	3:2	Audio FIFO 1 source selection 00: from audio source 0 01: from audio source 1 10: from audio source 2 11: from audio source 3	

	REGFifo0Sel	1:0	Audio FIFO 0 source selection 00: from audio source 0 01: from audio source 1 10: from audio source 2 11: from audio source 3	
E3	REGAudMulCh	7	Read only. Depends on REGAudioEn	
	REGPktZeroCTS	6	Enable zero CTS value 0: disable 1: enable	0
	REGChStSel	4	Channel status selction 0: from user defined 1: from SPDIF interface	0
	REGS3RLChg	3	Audio source 3 R/L swap 0: not swap R/L channel 1: swap R/L channel	0
	REGS2RLChg	2	Audio source 2 R/L swap 0: not swap R/L channel 1: swap R/L channel	0
	REGS1RLChg	1	Audio source 1 R/L swap 0: not swap R/L channel 1: swap R/L channel	0
	REGS0RLChg	0	Audio source 0 R/L swap 0: not swap R/L channel 1: swap R/L channel	0
E4	REGAudSPxFlat[3:0]	7:4	User defined audio flat bit [0] for source 0 [1] for source 1 [2] for source 2 [3] for source 3	0x0
	REGAudErr2Flat	3	Auto audio error to flat setting 0: disable 1: enable	0
	RegAudMut2Flat	2		0
	RegEnASCLKDiv4	1		0
	RegEnASCLKDiv2	0		0
E5	RegForceASCLKDiv	7		0
		6:5		
	SpdifCompFit	4	Read Only.	X
	RegAudHBR	3	0: Low Bit Rate 1: High Bit Rate	0
		2:0		
E6		7:6		
	RegPCLKSMT	5	PCLK schmitt trigger option	0
		4		0
	RegSPDIFSMT	3	SPDIF schmitt trigger option	0
	RegMCLKSMT	2	MCLK schmitt trigger option	0
	RegSCKSMT	1	SCK schmitt trigger option	0
	RECAudChStNLPCM	0	Read-Only. Same as RegE7[4] for software compatibility	X
E7		7:6		
	RAudDecErrInt	5	RAudDecErrInt Read back	W1C
	RECAudChStNLPCM	4	Read-Only. Audio Channel Status assigned in SPDIF input	X

	ARECAudChStFs	3:0	Read-Only. Audio Channel Status assigned in SPDIF input	X
E8	Reserved	7		0
	Reserved	6		0
		5		
	RegEnExtInt	4	Enable extended interrupt to trigger INT event 0: Disable, 1: Enable	0
		3		
		2		
	RegDDCSMT	1	DDCSCL/DDCSDA Schmitt trigger option	0
	RegCMDSMT	0	PCSCL/PCSDA Schmitt trigger option	0
E9~EB				
EC	RegExtIntMask[7:0]	7		1
		6	Mask video parameter change interrupt	1
		5	Mask HDCP Pj check done interrupt	1
		4	Mask HDCP Ri check done interrupt	1
		3	Mask DDC bus hang interrupt	1
		2	Mask video input FIFO auto-reset interrupt	1
		1	Mask no audio input interrupt	1
		0	Mask audio decode error interrupt	1
ED	Reserved for ExtIntMask			
EE	RegExtIntSts[7:0]	7		-
		6	Video parameter change interrupt (W1C)	-
		5	HDCP Pj check done interrupt (W1C)	-
		4	HDCP Ri check done interrupt (W1C)	-
		3	DDC bus hang interrupt (W1C)	-
		2	Video input FIFO auto-reset interrupt (W1C)	-
		1	No audio input interrupt (W1C)	-
		0	Audio decode error interrupt (W1C)	-
EF	Reserved for ExtIntSts			
F0		7:3		
	RefCECIntSts	2	Read Only. CEC interrupt status	
	RefExtIntSts	1	Read Only. Extended HDMI interrupt status	-
	RefOriIntSts	0	Read Only. Original HDMI interrupt status	-
F0~F2				

1.10. Test Registers

Rx Test Registers				
Reg	Register Name	Bit	Definition	Default
F3		~~7:6~~		~~00~~
	REGDDCDrv[1:0]	5:4		01
	REGPCDrv[1:0]	3:2		10
	Reserved	1		0
	Reserved	0		0
F4	Reserved	7		0
	Reserved	6:4		0
	Reserved	3:2		
		1:0		0
F5 ~ F7				
F8	Reserved	7:0		0

2. Registers in Bank 1

2. 1 Packet Content Registers

N/CTS Packet				
Reg	Name	Bit	Definition	Default
130	REGPktAudCTS[7:0]	7:0		
131	REGPktAudCTS[15:8]	7:0		
132		7:4		
	REGPktAudCTS[19:16]	3:0		
133	REGPktAudN[7:0]	7:0		0x80
134	REGPktAudN[15:8]	7:0		0x18
135	REGPktAudN[19:16]	3:0		0x0
	REGPktAudCTSCnt[3:0]	7:4	Read Only, auto-calculated CTS value.	-
136	REGPktAudCTSCnt[11:4]	7:0	Read Only, auto-calculated CTS value.	--
137	REGPktAudCTSCnt[19:12]	7:0	CTS value of Audio Clock Regeneration Packet	--
Null Packet				
138	REGPktNull0Hdr[7:0]	7:0		
139	REGPktNull1Hdr[7:0]	7:0		
13A	REGPktNull2Hdr[7:0]	7:0		
13B	REGPktNull00PB[7:0]	7:0		
13C~ 155	REGPktNull01PB[7:0]~ REGPktNull26PB[7:0]	7:0	Null Packet Byte01~ Null Packet Byte26	
156	REGPktNull27PB[7:0]	7:0		
157				
AVI Packet				
158	REGPktAVIInfo01PB7	7	Reserved	0
	REGPktAVIInfoY[1:0]	6:5	RGB or YCbCr Indicator 00: RGB 01: YUV422 10: YUV444 11: Reserved	00
	REGPktAVIInfoA	4	Active Format Information Preset 0: No Data 1: Active Format Information valid	0
	REGPktAVIInfoB[1:0]	3:2	Bar Information 00: Bar Data not valid 01: Vertical Bar Info valid 10: Horizontal Bar Info valid 11: Vertical and Horizontal Bar Info valid	00
	REGPktAVIInfoS[1:0]	1:0	Scan Information 00: No Data 01: Composed for Overscanned display 10: Composed for Underscanned display 11: Reserved	00
159	REGPktAVIInfoC[1:0]	7:6	Colorimetry 00: No Data 01: SMPTE170M/ITU601 10: ITU709 11: Extended colorimetry information valid(See REGPktAVIInfoEC[2:0])	00

	REGPktAVIInfoM[1:0]	5:4	Picture Aspect Ratio 00: No Data 01: 4:3 10: 16:9 11: Reserved	00
	REGPktAVIInfoR[3:0]	3:0	Active Format Aspect Ratio 1000: Same as picture aspect ratio 1001: 4:3 1010: 16:9 1011: 14:9 Other values : Reserved	1000
15A	REGPktAVIInfoITC	7	IT Content 0: No Data 1: IT Content	0
	REGPktAVIInfoEC[2:0]	6:4	Extended Colorimetry 000: xvYCC601 001: xvYCC709 Other value: Reserved	000
	REGPktAVIInfoQ[1:0]	3:2	RGB Quantization Range 00: Default, depends on video format 01: Limited Range 10: Full Range 11: Reserved	00
	REGPktAVIInfoSC[1:0]	1:0	Non-Uniform Picture Scaling 00: No non-uniform scaling 01: Picture has been scaled horizontally 10: Picture has been scaled vertically 11: Picture has been scaled horizontally and vertically	00
15B	REGPktAVIInfo04PB7	7	Reserved	0
	REGPktAVIInfoVIC[6:0]	6:0	Video Identification Code. Please reference CEA-861-D Table13 for detailed information.	0000000
15C	REGPktAVIInfoYQ[1:0]	7:6	YCC Quantization Range	00
	REGPktAVIInfoCN[1:0]	5:4	Content Type	00
	REGPktAVIInfoPR[3:0]	3:0	Pixel Repetition Factor Please reference CEA-861-D Table 12 for detailed information.	0000
15D	REGPktAVIInfoSUM[7:0]	7:0	Check Sum of the AVI Information	XX
15E	REGPktAVIInfo06PB[7:0]	7:0	AVI InfoFrame Packet Byte6	XX
15F	REGPktAVIInfo07PB[7:0]	7:0	AVI InfoFrame Packet Byte7	XX
160	REGPktAVIInfo08PB[7:0]	7:0	AVI InfoFrame Packet Byte8	XX
161	REGPktAVIInfo09PB[7:0]	7:0	AVI InfoFrame Packet Byte9	XX
162	REGPktAVIInfo10PB[7:0]	7:0	AVI InfoFrame Packet Byte10	XX
163	REGPktAVIInfo11PB[7:0]	7:0	AVI InfoFrame Packet Byte11	XX
164	REGPktAVIInfo12PB[7:0]	7:0	AVI InfoFrame Packet Byte12	XX
165	REGPktAVIInfo13PB[7:0]	7:0	AVI InfoFrame Packet Byte13	XX
166	REGPktACP00HB[7:0]	7:0	ACP Header Byte0	XX
167	REGPktACP02HB[7:0]	7:0	ACP Header Byte2	XX
Audio InfoFrame Packet				
168	REGPktAudInfoCT[3:0]	7:4	Coding Type. Always 0000	0000
	REGPktAudInfo01PB3	3	Reserved	0
	REGPktAudInfoCC[2:0]	2:0	Channel Number 000: Refer to Stream Header 001: 2 channel	000

			010: 3 channel 011: 4 channel 100: 5 channel 101: 6 channel 110: 7 channel 111: 8 channel	
169	REGPktAudInfo02PBRsvd	7:5	Reserved	000
	REGPktAudInfoSF[2:0]	4:2	Audio Sampling Frequency 000: Refer to stream header 001: 32KHz 010: 44.1KHz 011: 48KHz 100: 88.2KHz 101: 96KHz 110: 176.4KHz 111: 192KHz	00
16A	REGPktAudInfo03PB[7:0]	7:0	Reserved	0x00
16B	REGPktAudInfoCA[7:0]	7:0	Channel/Speaker Allocation. See CEA-861-D Section 6.6.2 for details	0x0
16C	REGPktAudInfoDM	7	Downmix Inhibit. See CEA-861-D Section 6.6.2 for details.	0
	REGPktAudInfoLSV[3:0]	6:3	Level Shift Value(for downmixing). See CEA-861-D Section 6.6.2 for details.	0000
	REGPktAudInfo05PB2	2	Reserved	0
	REGPktAudInfoPBL[1:0]	1:0	LFE Playback level information	00
16D	REGPktAudInfoSUM[7:0]	7:0	Audio InfoFrame Packet Check Sum	XX
ACP InfoFrame Packet				
16E	REGPktACP01HB[7:0]	7:0	Bit2:0→ REGPktACPType[2:0] Content protection type 000: Generic Audio 001: IEC60958-Identified Audio 010: DVD-Audio 011: Super Audio CD 1XX Reserved	XX
16F	REGPktACP00PB[7:0]	7:0	ACP Packet Byte00	XX
170	REGPktACP01PB[7:0]	7:0	ACP Packet Byte01	XX
171	REGPktACP02PB[7:0]	7:0	ACP Packet Byte02	XX
172	REGPktACP03PB[7:0]	7:0	ACP Packet Byte03	XX
173	REGPktACP04PB[7:0]	7:0	ACP Packet Byte04	XX
174	REGPktACP05PB[7:0]	7:0	ACP Packet Byte05	XX
175	REGPktACP06PB[7:0]	7:0	ACP Packet Byte06	XX
176	REGPktACP07PB[7:0]	7:0	ACP Packet Byte07	XX
177	REGPktACP08PB[7:0]	7:0	ACP Packet Byte08	XX
178	REGPktACP09PB[7:0]	7:0	ACP Packet Byte09	XX
179	REGPktACP10PB[7:0]	7:0	ACP Packet Byte10	XX
17A	REGPktACP11PB[7:0]	7:0	ACP Packet Byte11	XX
17B	REGPktACP12PB[7:0]	7:0	ACP Packet Byte12	XX
17C	REGPktACP13PB[7:0]	7:0	ACP Packet Byte13	XX
17D	REGPktACP14PB[7:0]	7:0	ACP Packet Byte14	XX
17E	REGPktACP15PB[7:0]	7:0	ACP Packet Byte15	XX
17F	REGPktACP16PB[7:0]	7:0	ACP Packet Byte 16	XX
Vendor Specific InfoFrame Packet				
180	REGPkt3DInfo04PB[7:0]	7:0		XX
181	REGPkt3DInfo05PB[7:0]	7:0		XX
182	REGPkt3DInfo06PB[7:0]	7:0		XX

183	REGPkt3DInfoSUM[7:0]	7:0		XX
184~189				
MPEG InfoFrame Packet				
18A		7:3		
	REGPktMpgInfoMF[1:0]	2:1	MPEG Frame 00: No Data 01: I Picture 10: B Picture 11: P Picture	XX
	REGPktMpgInfoFR	0	Field Repeat 0: New Field 1: Repeated Field	X
18B	REGPktMpgInfo01PB[7:0]	7:0	MPEG InfoFrame Packet Data01	XX
18C	REGPktMpgInfo02PB[7:0]	7:0	MPEG InfoFrame Packet Data02	XX
18D	REGPktMpgInfo03PB[7:0]	7:0	MPEG InfoFrame Packet Data03	XX
18E	REGPktMpgInfo04PB[7:0]	7:0	MPEG InfoFrame Packet Data04	XX
18F	REGPktMpgInfoSUM[7:0]	7:0	MPEG InfoFrame Packet Check Sum	XX

2.2 Audio Channel Status Registers

Audio Channel Status				
Reg	Name	bit	Definition	Default
190				
191		7		
	REGAudChStD[2:0]	6:4	ICE60958-3 p9 bit[5:3] Additional format information depends on linear PCM audio mode: 5|4|3 ----- 000: 2 audio channels without pre-emphasis. 001: 2 audio channels with 50μs/15μs pre-emphasis. 010: reserved 011: reserved All other combination are reserved and shall not be used until further defined. Read back RECAudChStD when(REGChStSel='1') else REGAudChStD;	000
	REGAudChStC	3	refer to ICE60958-3 p9 bit[2] 0: Software for which copyright is asserted. 1: Software for which no copyright is asserted. Read back RECAudChStC when(REGChStSel='1') else REGAudChStC;	0
	REGAudNLPCM	2	1: for Non-Linear PCM format audio 0: for Linear PCM format audio Read back RECAudNLPCM when(REGChStSel='1') else REGAudNLPCM;	0
	REGAudChStA	1	refer to ICE60958-3 p9 bit[0] use of channel status block Read back RECAudChStA when(REGChStSel='1') else REGAudChStA;	0
	REGAudMono	0	Monochrome bit 1: if there is only one audio source	0
192	REGAudChStCat[7:0]	7:0	Audio category code groups. Refer to IEC60958-3 5.3.2. channel status byte 2 (bit 15-8) Read back RECAudChStCat when(REGChStSel='1') else REGAudChStCat;	
193		7:4		
	REGAudChStSrc[3:0]	3:0	refer to IEC60958-3 p11 bit 16-19 Source number, 0~15, 0 means don't take number into account. Read back RECAudChStSrc when(REGChStSel='1') else REGAudChStSrc;	
194		7:4		

	REGAudChStCH[3:0]	3:0	refer to IEC60958-3 p11 bit 23-20 single and dual channel operating modes are defined in IEC60958-1 Channel number of source 0 L-channel Read back RECAudChStCH when(REGChStSel='1') else REGAudChStCH;	
195~197				
198	REGAudChStCA[3:0]	7:4	refer to IEC60958 p12 bit 29~28 [7:6]: Clock accuracy 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency. [5:4]: Reserved Read back RECAudChStCA when(REGChStSel='1') else REGAudChStCA;	
	REGAudChStFs[3:0]	3:0	Sample frequency indicated in IEC60958-3 p11 bit 24~27. Sample frequency of software indicated 27..24 -------- 0000: 44.1 KHz 1000: 88.2 KHz 1100: 176.4 KHz 0110: 24 Khz 0010: 48Khz 1010: 96Khz 1110: 192KHz 0011: 32KHz 0000: sampling frequency not indicated. 1001: HBR Read back RECAudChStFs when(REGChStSel='1') else REGAudChStFs;	0x0

199	REGAudChStOFs[3:0]	7:4	Sample frequency indicated in IEC60958-3 p11 bit 24~27. Original Sampling Frequency 27..24 --------- 1111: 44.1 KHz 0111: 88.2 KHz 0011: 176.4 KHz 1001: 24 Khz 1101: 48Khz 0101: 96Khz 0001: 192KHz 1100: 32KHz 0000: sampling frequency not indicated. 0110: HBR Read back RECAudChStOFs when(REGChStSel='1') else REGAudChStOFs;	
	REGAudChStWL[3:0]	3:0	Audio sample word length 1101: 21 bits 1011: 24 bit 1001: 23 bit 0101: 22 bit 0011: 20 bit 0001: Word length not indicated 1100: 17 bit 1010: 20 bit 1000: 19 bit 0100: 18 bit 0010: 16 bit 0000: Word length not indicated Read back RECAudChStWL when(REGChStSel='1') else REGAudChStWL;	
19A~ 19F				
1A0				
1A1				
1A2				
1A3~ 1B4				
ACP InfoFrame Packet (General Packet)				
1B5	REGPktACP17PB[7:0]	7:0	ACP Packet Byte 17	XX
1B6	REGPktACP18PB[7:0]	7:0	ACP Packet Byte 18	XX
1B7	REGPktACP19PB[7:0]	7:0	ACP Packet Byte 19	XX
1B8	REGPktACP20PB[7:0]	7:0	ACP Packet Byte 20	XX
1B9	REGPktACP21PB[7:0]	7:0	ACP Packet Byte 21	XX
1BA	REGPktACP22PB[7:0]	7:0	ACP Packet Byte 22	XX
1BB	REGPktACP23PB[7:0]	7:0	ACP Packet Byte 23	XX
1BC	REGPktACP24PB[7:0]	7:0	ACP Packet Byte 24	XX
1BD	REGPktACP25PB[7:0]	7:0	ACP Packet Byte 25	XX
1BE	REGPktACP26PB[7:0]	7:0	ACP Packet Byte 26	XX
1BF	REGPktACP27PB[7:0]	7:0	ACP Packet Byte 27	XX

3. CEC Registers Bank

3.1 CEC Control Registers

CEC Control Registers				
Reg	Name	Bit	Definition	Default
00~05				
06	Reserved	7:6		
	TxFail_Int_Mast	5	0: Interrupt Enable 1: Interrupt Mask	1
	RxDone_Int_Mask	4	0: Interrupt Enable 1: Interrupt Mask	1
	TxDone_Int_Mask	3		1
	RxFail_Int_Mask	2		1
	Rx_Int_Mask	1		1
	Tx_Int_Mask	0		1
07	Reserved	7:0		000
08	Fire_Frame	7	1: Fire CEC command out	0x08
	Reserved	6		
	CEC_OE	5	Force CEC output value	
	CEC_Force	4	Force CEC output regardless of normal function	
	CEC_SMT	3	Schmitt trigger of CEC IO 1: Enable 0: Disable	
	CEC_Rst	2	Reset CEC block 1: Enable 0: Disable	
		1		
	Reg_CECInt_En	0	CEC interrupt enable 1: Enable 0: Disable	
09	DataBit_Sel	7	Select data bit 1: Increase 0.1ms 0: Normal	0x20
	Region_Sel	6	Select region for error bit 1: Whole region 0: Region form state Start to IDLE	
	RxSelf_Sel	5	Initiator received CEC bus data. 1: Disable 0: Enable	
	Reserved	4:3		
	Pulse_Sel	2	Select illegal bit as error bit 1: Enable 0: Disable	
	NACK_En	1	Acknowledge from follower to initiator 1: NACK 0: ACK	
	En100ms_Cnt	0	Used as a reference 100ms time interval for CEC calibration.	
0A	Reserved	7:5		0x00
	ArBit_Sel	4	Select bit time for arbitration lose. 1: 3 bit time 0: 5 bit time	
	Reserved	3:0		
0B	Data_Min	7:0	Minimum data bit time	0x14
0C	Timer_Unit	7:0	CEC timer unit, nominally 100us.	0x59

			This value should be decided from MS_Count.	
0D	CEC_Drv[1:0]	7:6	00: 2.5mA, 01:5mA, 10:7.5mA, 11:10mA	01
	CEC_IOSR	5	CEC IO slew rate control	0
	CEC_IOPU	4	0: Normal, 1: Pull-up	1
		3:0		
0E~ 0F				

3.2 CEC Initiator Registers

10	Tx_Header	7:0	CEC initiator command header	0x00
11	Tx_Opcode	7:0	CEC initiator command opcode	0x00
12	Tx_Operand1	7:0	CEC initiator command operand1	0x00
13	Tx_Operand2	7:0	CEC initiator command operand2	0x00
14	Tx_Operand3	7:0	CEC initiator command operand3	0x00
15	Tx_Operand4	7:0	CEC initiator command operand4	0x00
16	Tx_Operand5	7:0	CEC initiator command operand5	0x00
17	Tx_Operand6	7:0	CEC initiator command operand6	0x00
18	Tx_Operand7	7:0	CEC initiator command operand7	0x00
19	Tx_Operand8	7:0	CEC initiator command operand8	0x00
1A	Tx_Operand9	7:0	CEC initiator command operand9	0x00
1B	Tx_Operand10	7:0	CEC initiator command operand10	0x00
1C	Tx_Operand11	7:0	CEC initiator command operand11	0x00
1D	Tx_Operand12	7:0	CEC initiator command operand12	0x00
1E	Tx_Operand13	7:0	CEC initiator command operand13	0x00
1F	Tx_Operand14	7:0	CEC initiator command operand14	0x00
20	Tx_Operand15	7:0	CEC initiator command operand15	0x00
21	Tx_Operand16	7:0	CEC initiator command operand16	0x00
22	Reserved	7:4		0x00
	Logical_Addr	3:0	CEC target logical address	
23	Reserved	7:5		0x00
	Out_Num	4:0	CEC output byte size in a frame	
24~ 2F				

3.3 CEC Follower Registers

30	Rx_Header	7:0	RO. CEC follower command header	0x00
31	Rx_Opcode	7:0	RO. CEC follower command opcode	0x00
32	Rx_Operand1	7:0	RO. CEC follower command operand1	0x00
33	Rx_Operand2	7:0	RO. CEC follower command operand2	0x00
34	Rx_Operand3	7:0	RO. CEC follower command operand3	0x00
35	Rx_Operand4	7:0	RO. CEC follower command operand4	0x00
36	Rx_Operand5	7:0	RO. CEC follower command operand5	0x00
37	Rx_Operand6	7:0	RO. CEC follower command operand6	0x00
38	Rx_Operand7	7:0	RO. CEC follower command operand7	0x00
39	Rx_Operand8	7:0	RO. CEC follower command operand8	0x00
3A	Rx_Operand9	7:0	RO. CEC follower command operand9	0x00
3B	Rx_Operand10	7:0	RO. CEC follower command operand10	0x00
3C	Rx_Operand11	7:0	RO. CEC follower command operand11	0x00
3D	Rx_Operand12	7:0	RO. CEC follower command operand12	0x00
3E	Rx_Operand13	7:0	RO. CEC follower command operand13	0x00
3F	Rx_Operand14	7:0	RO. CEC follower command operand14	0x00
40	Rx_Operand15	7:0	RO. CEC follower command operand15	0x00
41	Rx_Operand16	7:0	RO. CEC follower command operand16	0x00
42	Reserved	7:5		0x00

	In_Cnt	4:0	RO. CEC follower received bytes.	

3.4 CEC Misc. Registers

43	Reserved	7:5		0x00
	Out_Cnt	4:0	RO. CEC initiator output bytes.	
44	Reserved	7		0x00
	Ready_Fire	6	RO. Bus ready for firing a CEC command.	0x00
	Error_Status	5:4	RO. Error status. 00: No error occurs. 01: Received data period < minimum data bit period. 10: Illegal held-low period. 11: Both	0x00
	Out_Status	3:2	RO. Output status. 00: Received ACK 01: Received NACK 10: Retry, if no ACK, NACK or arbitration lose. 11: Fail	
	Bus_Status	1	RO. Bus status. 0: Busy 1: Free	
	Reserved	0		
45	MS_Count	7:0	RO. MS_Count[7:0]	0x00
46	MS_Count	7:0	RO. MS_Count[15:8]	0x00
47	Reserved	7:4		0x00
	MS_Count	3:0	RO. MS_Count[19:16]	
48	Reserved	7:6		0x00
	CEC_Int	5	CEC interrupt status	
	Reserved	4:0		
49	Reserved	7:0		0x00
4A	Reserved	7:0		0x00
4B	Reserved	7:0		0x00
4C	Reserved	7:6		0x00
	TxFail_Int	5	R: CEC initiator output fail interrupt. W: Write 1 clear this interrupt	
	RxDone_Int	4	R: CEC received finish interrupt. W: Write 1 clear this interrupt	
	TxDone_Int	3	R: CEC output finish interrupt. W: Write 1 clear this interrupt	
	RxFail_Int	2	R: CEC received fail interrupt. W: Write 1 clear this interrupt	
	Rx_Int	1	R: CEC follower received byte interrupt. W: Write 1 clear this interrupt	
	Tx_Int	0	R: CEC initiator output byte interrupt. W: Write 1 clear this interrupt	
4D~ FF				