Chapter 35 MIPI-CSI PHY

35.1 Overview

The MIPI D-PHY is compliant with the MIPI D-PHY interface specification, revision 1.1. The D-PHY can be reused for both master and slave applications. The lane modules are bidirectional with HS-TX, HS-RX, LP-TX, LP-RX, and LP-CD functions.

The D-PHY is targeted for the digital data transmission between a host processor and display drivers or camera interfaces in mobile applications, supporting a maximum effective bit rate of 1.5Gbps per lane. The assembled four-data-lane system enables up to 6Gbps aggregate communication throughputs, delivering the bankwidth needed for high-throughput data transfer.

There were three D-PHY in RK3288, one is for DSI, one is for CSI, another can configure to DSI or CSI.

The MIPI D-PHY supports the following features:

- Attachable PLL clock multiplication unit for master-side functionality
- Flexible input clock reference – 5MHz to 500MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80Mbps to 1.5Gbps in forward direction
- Aggregate throughput up to 6Gbps with four data lanes
- PHY-Protocol Interface (PPI) for clock and data lanes
- Low-power Escape modes and Ultra Low Power state
- 1.8V±10% analog supply operation
- 1.0V±10% digital supply operation

35.2 Block Diagram

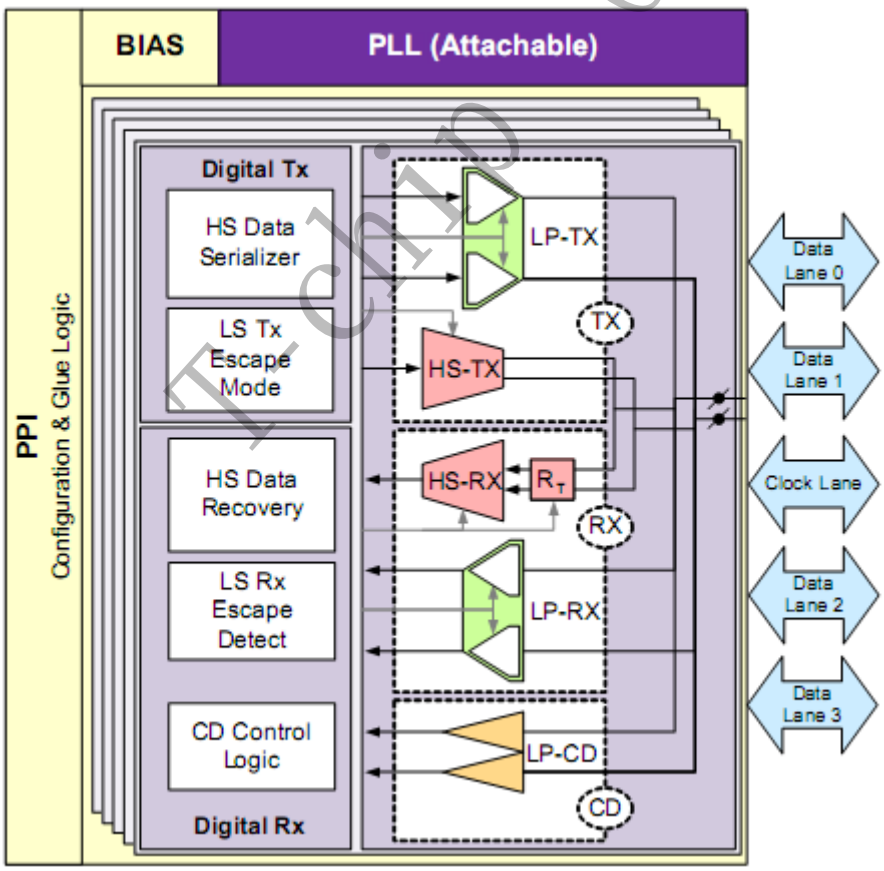


Fig. 35-1 MIPI D-PHY detailed block diagram

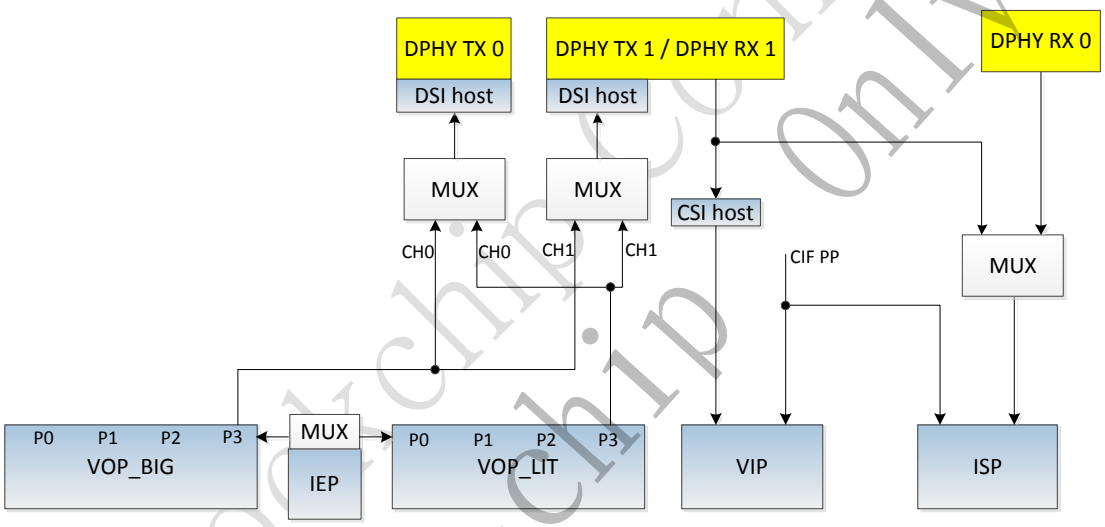
- HS Driver/Receiver
  - Implements high-speed TX and RX functionalities
  - Replicated for each lane
- LP Driver/Receiver
  - Implements the low-power TX and RX functionalities
  - Replicated for each lane
- Contention Detectors
  - Used for contention detector when there is a direction change in the low-power mode
  - Replicated for each lane
- PLL
  - Generates high-speed clocks required in Master Mode
  - Can be attached to D-PHY for Master applications
- Digital Block: Includes all control logic as well as PPI

MIPI CSI2 D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two lines to a complementary part at the other side of the Lane Interconnect.

35.3 Function Description

35.3.1 System Connection

There are three D-PHY in RK3288, their connection are shown as following figure:



D-PHY RX0

D-PHY RX0 is only used for RX, receive the Mipi Camera data then send to ISP. In this mode, you must set grf_con_isp_dphy_sel (bit[1] of GRF_SOC_CON6) to 1'b0.

D-PHY TX0

D-PHY TX0 is only used for TX, send the data from VOP_BIG or VOP_LIT to the Mipi Panel. You can select data from VOP_BIG or VOP_LIT by setting grf_con_dsi0_lcdc_sel (bit[6] of GRF_SOC_CON6)

D-PHY TX1RX1

D-PHY TX1RX1 can configure to for TX or for RX.

The D-PHY can be configured to for TX by setting grf_dphy_tx1rx1_masterslavez = 1'b0, and setting grf_dphy_tx1rx1_basedir = 1'b0, and you can set the grf_con_dsi1_lcdc_sel (bit[9] of GRF_SOC_CON6) to select the data from VOP_BIG or from VOP_LIT.

If you want the D-PHY work as for RX, you must set grf_dphy_tx1rx1_masterslavez = 1'b1, and set grf_dphy_tx1rx1_basedir = 1'b1, then you must select the data from D-PHY RX1 to CSI Host or ISP by setting grf_con_isp_dphy_sel (bit[1] of GRF_SOC_CON6)

The detail register setting is as following table:

Table 35-1 Register Config For D-PHY Mode Select

TX0 + VOP_BIG	**TX0 + VOP_LIT**	**TX1RX1 + VOP_BIG**	**TX1RX1 + VOP_LIT**
bit[6] of GRF_SOC_CON6 = 1'b0	bit[6] of GRF_SOC_CON6 = 1'b1	bit[9] of GRF_SOC_CON6 = 1'b0	bit[9] of GRF_SOC_CON6 = 1'b1
		bit[14] of GRF_SOC_CON6 = 1'b0	bit[14] of GRF_SOC_CON6 = 1'b0
		bit[14] of GRF_SOC_CON14 = 1'b1	bit[14] of GRF_SOC_CON14 = 1'b1
		bit[15] of GRF_SOC_CON14 = 1'b0	bit[15] of GRF_SOC_CON14 = 1'b0
bit[8:7] of GRF_SOC_CON6	bit[8:7] of GRF_SOC_CON6	bit[11:10] of GRF_SOC_CON6	bit[11:10] of GRF_SOC_CON6
bit[11:0] of GRF_SOC_CON8	bit[11:0] of GRF_SOC_CON8	bit[15:0] of GRF_SOC_CON9	bit[15:0] of GRF_SOC_CON9
bit[10:8] of GRF_SOC_CON15	bit[10:8] of GRF_SOC_CON15	bit[12] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14
		bit[7:4] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15
bit[0] of GRF_SOC_CON16	bit[0] of GRF_SOC_CON16	bit[1] of GRF_SOC_CON16	bit[1] of GRF_SOC_CON16
RX0 + ISP	**TX1RX1 + ISP**	**TX1RX1 + CSI_Host + VIP**	
bit[1] of GRF_SOC_CON6 = 1'b0	bit[1] of GRF_SOC_CON6 = 1'b1		
	bit[14] of GRF_SOC_CON6 = 1'b1	bit[14] of GRF_SOC_CON6 = 1'b1	
	bit[13] of GRF_SOC_CON14 = 1'b1	bit[13] of GRF_SOC_CON14 = 1'b0	
	bit[14] of GRF_SOC_CON14 = 1'b0	bit[14] of GRF_SOC_CON14 = 1'b0	
	bit[15] of GRF_SOC_CON14 = 1'b1	bit[15] of GRF_SOC_CON14 = 1'b1	
bit[15:0] of GRF_SOC_CON10	bit[15:0] of GRF_SOC_CON9	bit[15:0] of GRF_SOC_CON9	
bit[10:0] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14	
bit[3:0] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15	

35.3.2 Operating Modes

This section describes the various operating modes of the MIPI D-PHY, the following Figure illustrates the various modes of the MIPI D-PHY during initialization and active operating mode.

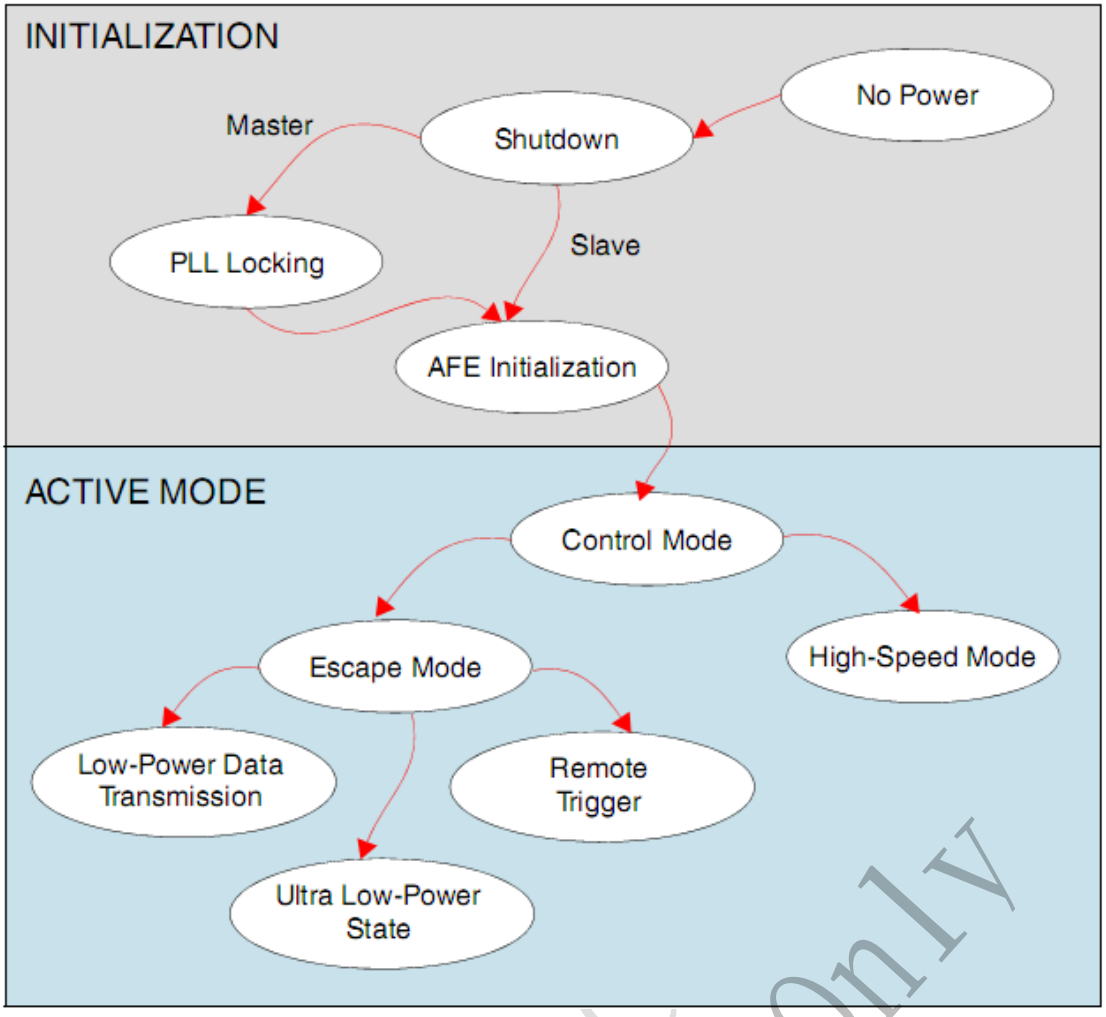


Fig. 35-2 MIPI D-PHY Initialization from Shutdown to Idle Modes

Initialization

- **No Power Mode**

The No Power mode is characterized by the non-existence of any supply voltage applied to MIPI D-PHY . In order to get to the powered modes, proper voltages should be applied sequentially to MIPI D-PHY , this task is usually done by the SoC PMU or eventually by global powering up sequence.

The recommended powering up sequence is that the core voltage (VDD) powers up first and the I/O voltage (AVDD) powers up next. This is not considered as a constraint, but instead a guideline, as it results in the best-case operating scenario, where power-down currents are kept to a minimum.

For complex SoCs, it is likely that core voltage islands exist for different main blocks/macros, while the I/O voltage is always present. This means that VDD may power up after the I/O voltage and not follow the previous guideline. This is not considered a problem because MIPI D-PHY supports power collapsing, which ensures valid logical levels across power domains even when one of the supplies is not present at a given time.

The digital core voltage (VDD) and I/O analog voltage (AVDD) domains are isolated by the use of level shifter cells. No additional leakage is expected when there is a lack of VDD and/or AVDD.

- **Shutdown Mode**

This mode is the lowest power consumption mode, where all analog blocks are disabled, and digital logic is reset. The current consumption is given by the analog stand-by current and the

digital logic leakage current. It is entered asynchronously when RSTZ and SHUTDOWNZ are in low state. It should be ensured that the TESTCLR signal is asserted by default, as it acts as an active high reset to the control block responsible for the configuration values preset.

In this mode, the differential lines of DATAN/DATAP and CLKN/CLKP are high impedance (Hi-Z).

Depending on the MIPI D-PHY usage, some additional steps can be performed. By default, MIPI D-PHY is configured to work only on the lower operation range of 80-110 Mbps. If higher bit rate operation is required, you should set the register hsfreqrange (HS RX Control of Lane 0) with the proper code. If MIPI D-PHY is expected to work always at the same bit rate, this additional step can be performed while in Shutdown mode as the control interface is independent of the rest of MIPI D-PHY. Conversely, if the MIPI D-PHY is expected to change the bit rate after initialization, hsfreqrange should be updated while in Idle mode. For more information on these options, see "Active Modes".

In addition, when working in Master mode, the PLL must be configured to select the proper input frequency and the desired output frequency, which determines the bit rate on the transmission path. For more information, see "PLL Requirements".

When RSTZ and SHUTDOWNZ are set to logic high level, MIPI D-PHY leaves this state and starts an initialization procedure.

- **PLL Locking Mode and AFE Initialization**

The MIPI D-PHY consists of four data lanes, but applications can use four or lesser number data lanes. In such cases, you are granted access to individual enabling signals (ENABLE_N) that control which lanes should be used and evolve through all the necessary initialization steps. It is assumed that such configurations are static or at least are stable prior to leaving the Shutdown mode.

After the reset signals (RSTZ and SHUTDOWNZ) are released, the MIPI D-PHY begins an initialization sequence that allows its correct operation. Sequence of the release of signals is not critical but it is recommended that SHUTDOWNZ precedes RSTZ. It is also assumed that the CFG_CLK signal is available and stable by that time.

If there are no test or configuration operations to be performed, the TESTCLR signal can be kept at logic high level. Otherwise, the TESTCLR must be de-asserted to bring the control logic out of reset and allow for the necessary configuration steps through the control interface.

The D-PHY specification has many timing intervals which have to be followed to ensure proper operation. The fact that those timing intervals often have both a relative Unit Interval (UI) and absolute timing components, makes it difficult to meet the maximum and minimum values across the complete data rate range (80 Mbps-1.5 Gbps) by just using default settings. To cope with this, MIPI D-PHY implements a set of frequency ranges that needs to be configured prior to starting normal operation. Those ranges, when in Master operation, also define the operating bit rate, assuming REFCLK is equal to 27MHz. If the desired bit rate or REFCLK frequencies are different, directly configure the PLL as described in "PLL Requirements". All these steps come under the category of configurations that need to be performed through the control interface with TESTCLR de-asserted.

The following Table lists the frequency ranges.

Table 35-2 Frequency Ranges

Range (Mbps)	hsfreqrange[5:0]	Default Bit Rate (Mbps)
80-90 (default)	000000	81
90-100	010000	90
100-110	100000	108

110-130	000001	126
130-140	010001	135
140-150	100001	144
150-170	000010	162
170-180	010010	180
180-200	100010	198
200-220	000011	216
220-240	010011	234
240-250	100011	243
250-270	000100	270
270-300	010100	297
300-330	000101	324
330-360	010101	360
360-400	100101	396
400-450	000110	450
450-500	010110	486
500-550	000111	540
550-600	010111	594
600-650	001000	648
650-700	011000	684
700-750	001001	738
750-800	011001	783
800-850	101001	846
850-900	111001	900
900-950	001010	945
950-1000	011010	999
1000-1050	101010	1044
1050-1100	111010	1080
1100-1150	001011	1134
1150-1200	011011	1188
1200-1250	101011	1242
1250-1300	111011	1296

1300-1350	001100	1350
1350-1400	011100	1386
1400-1450	101100	1440
1450-1500	111100	1494

The hsfreqrange field is accessible through control code 0x44 (“HS RX Control of Lane 0”) when TESTDIN[7] = 0 and TESTDIN[0] = 0. The hsfreqrange[5:0] field is programmed with the contents of TESTDIN[6:1] at every rising edge of TESTCLK.

If the MIPI D-PHY is configured to work as a Master (MASTERSLAVEZ=1'b1), the PLL becomes active and MIPI D-PHY goes through the PLL Locking mode, in which the MIPI D-PHY waits for the PLL to acquire lock, indicated by the LOCK output going high. A valid REFCLK (FREFCLK) should be provided.

Following the PLL lock, the rest of the AFE is initialized leading to the enabling of the low-power drivers. After completing these transitory states, the lines go to the Stop state (LP = 11) and the TX achieves active mode.

In the case of a Slave configuration (MASTERSLAVEZ = 1'b0), PLL is inactive, therefore only the rest of AFE initialization takes place.

The initialization sequence determines that bandgap and biasing blocks are enabled first. After the related voltage and current references get settled, a second step is triggered where the internal calibrations are performed, and this can include internal resistors, receivers offset compensation, and so on.

When this second step is complete, the control is passed to the lanes, which handle the power management for LP/HS requests, enabling or disabling the corresponding drivers and receivers.

All initialization steps are performed once the STOPSTATEDATA_N and STOPSTATECLK outputs get asserted.

Initialization period (TINIT) is a protocol dependent parameter with a minimum 100 µs defined by the specification. The MIPI D-PHY does not set any limit to the initialization period, meaning it drives a Stop state (LP-11) immediately after the AFE initialization and PLL lock when in Master mode, or alternatively starts decoding the LP commands after the AFE initialization in Slave mode. It is up to the controller or the upper layers to ensure the proper initialization times through the correct handling of MIPI D-PHY control signals. This time must conform to D-PHY specification and obey the minimum specified 100 µs value.

Following Figure shows a possible power-up sequence for a Slave application when the default setting is 80-110 Mbps operation.

If the desired operation mode is different from the default one, additional configuration steps can be performed during the T2+T3 time window.

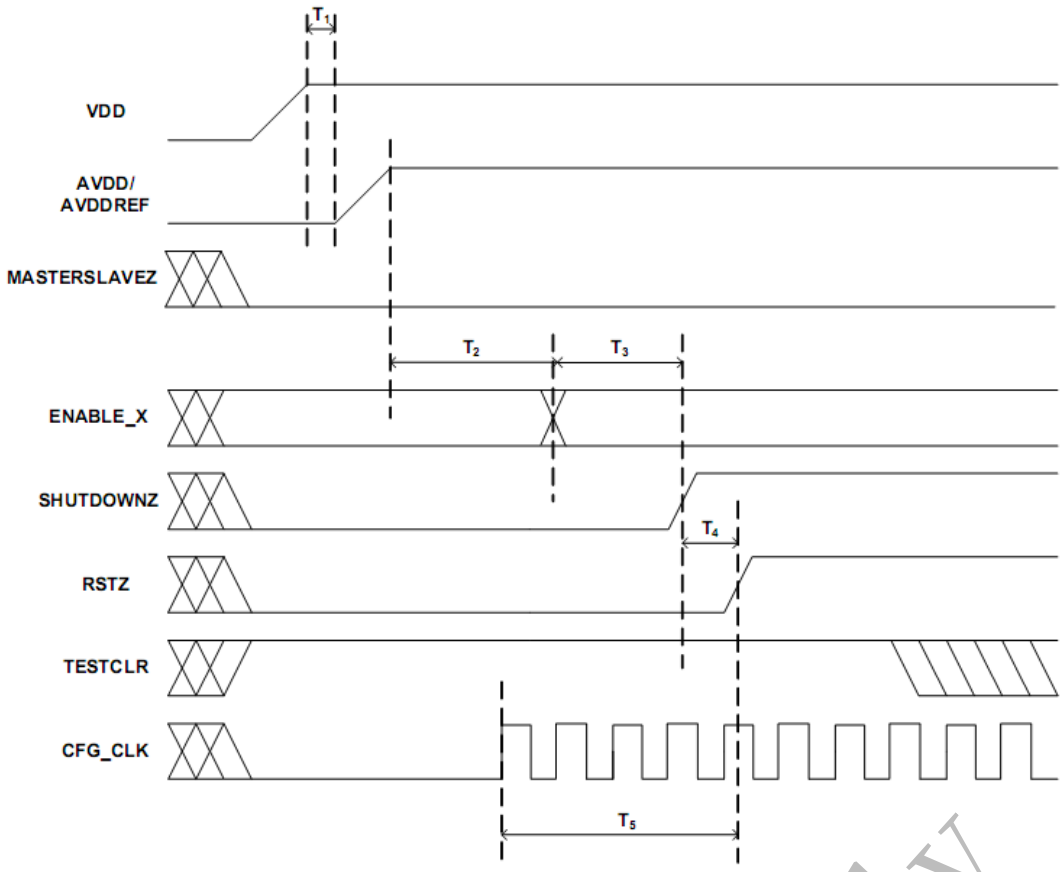


Fig. 35-3 Power-Up Sequence for Slave Operation

Table 35-3 Power-Up Sequence Timings

Parameter	Symbol	Minimum	Typical	Units
Delay from stable VDD to AVDD/AVDDREF start	T1	0	1	us
Delay from stable AVDD/AVDDREF to ENABLE_X definition	T2	0		ns
Delay for assertion of SHUTDOWNZ after ENABLE_X definition	T3	5		ns
Delay from SHUTDOWNZ assertion to RSTZ assertion	T4	5		ns
Time for CFG_CLK setting before the assertion of RSTZ	T5	1		CFG_CLK

Active Modes

- **Idle Mode**

Idle mode is the default operating mode. After the initialization is completed (analog calibrations and PLL locking for Master configurations), the MIPI D-PHY remains in this default mode until some request is placed. The request is placed either by the protocol layer for TX, or directly through the sequence of low-power signals in the lanes in case of RX. While in control mode, the transmitter side sets the LP-11 state in the lines - this is called the Stop state. The receiver side remains in control mode while receiving LP-11 in the lines. Any request must start from and end in Stop state. Following a request, a lane can leave control mode for either high-speed data transfer mode, Escape mode, or Ultra Low Power state.

- **High-Speed Data Transfer Mode**

Once the initialization sequence is completed, the MIPI D-PHY remains in control mode, which is the default operating mode, until some request appears. High-speed is one of the possible requests at this point. High-speed data transfer occurs in bursts. Only during these bursts the lane is in high-speed mode. A high-speed burst must start from and return to a Stop state (control mode). A high-speed burst allows for the transmission of payload data by the data lanes. Inherent to such data transmission is the existence of a valid DDR clock in the clock lane.

High-speed data bursts are independent for each lane, which means that each data lane can start and end a high-speed transmission independently of the state of the remaining data lanes.

A burst contains the low-power initialization sequence, the high-speed data payload, and also the end of transmission sequence.

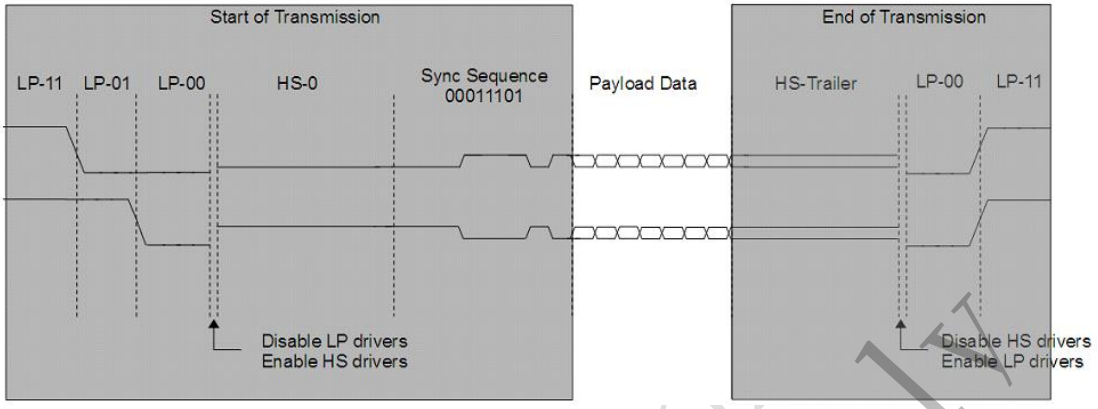


Fig. 35-4 HS Data Transfer Sequence

From the transmitter side, high-speed mode is entered when the corresponding TXREQUESTHS input is set high (assuming that MIPI D-PHY is in Stop state). This request is processed in a slightly different way for clock and data lanes. For a clock lane, the high-speed request is followed by the transmission of a low-power sequence that represents this request for the receiver side (a lane high-speed request). Only after generating this sequence the low-power driver is disabled, and the high-speed driver enabled. After the time necessary to settle, the transmission of the high-speed DDR clock starts. For a data lane, the high-speed request also starts with a lane high-speed request, and in addition, extend the payload data with a leader and a trailer sequence that allow for the receiver synchronization. The transmission of such sequence requires the existence of a valid high-speed clock signal in the clock lane.

When the high-speed request input is disabled, each lane leaves the high-speed data transmission mode. It is important that a clock lane must be in high-speed mode during the complete high-speed data transmission state of all the lanes. The clock lane must enter the high-speed mode before a high-speed data transmission begins and it must not leave this state before all the lanes finish their respective high-speed data transmission bursts. The operation sequence when leaving the high-speed mode is also slightly different for data and clock lanes. For a clock lane, the high-speed transmission always ends with a HS-0 state, followed by the disabling of the high-speed driver, and enabling of low-power driver. As for a data lane, the transmission ends with the differential state opposite to the last bit transmitted, followed by the disabling of the high-speed driver, and enabling of the low-power driver.

The receiver side enters the high-speed mode following the sequence of low-power states in the lines: LP-11, LP-01, and LP-00. This sequence is seen as a high-speed mode request, and toggles the enabling of the high-speed receivers. The synchronization is then achieved through the identification of the leader sequence in the received differential high-speed data. Once the synchronization is achieved, the MIPI D-PHY outputs the received bytes trough the protocol layer, until a Stop state (LP-11) is detected in the lane.

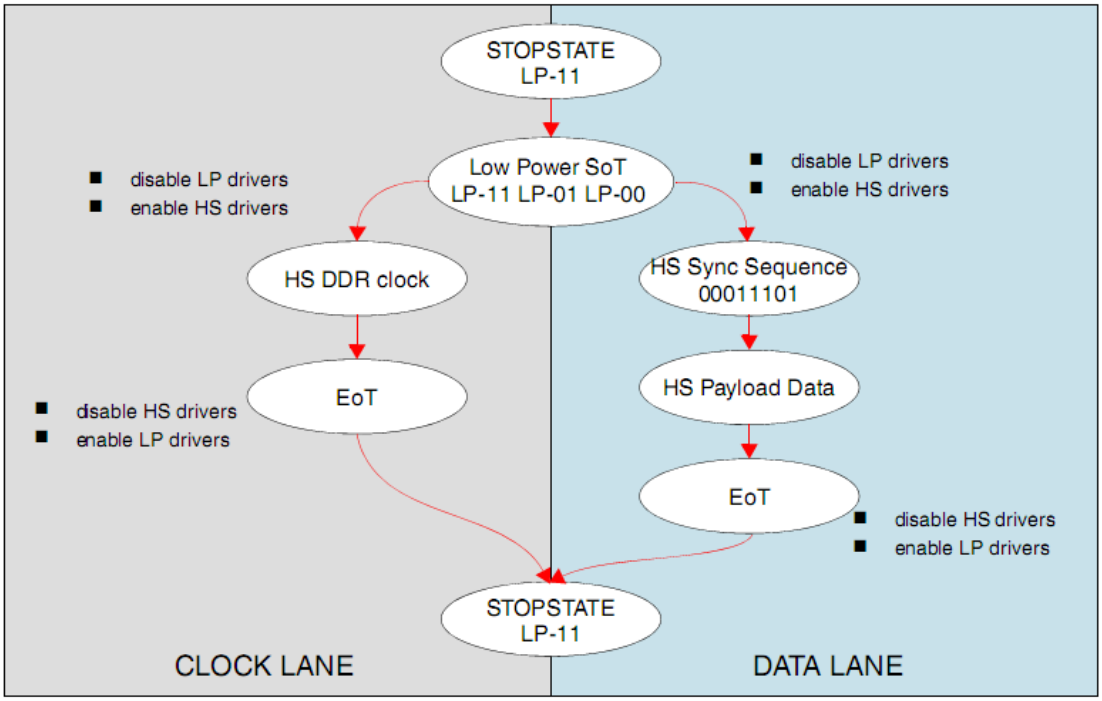


Fig. 35-5 HS Data Transfer State Diagram

The current implementation does not feature EoT processing which should be done at the controller level. This affects the behavior of the RXActiveHs and RXValidHS signals as illustrated in "Timing Diagrams".

- **Escape Mode**

Escape mode is a special mode of operation that uses the data lanes to communicate asynchronously using the low-power states at low-speed. The MIPI D-PHY supports this mode in both directions. A Data Lane enters the Escape mode through an Escape mode entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00), if an LP-11 is detected before reaching LP-00 state, the entry is aborted and the receiver returns to the Stop state. Once the sequence is correctly completed, the transmitter sends an 8-bit command to indicate a requested action. The following Table shows the Escape mode supported actions. If the entry command is not valid, it is ignored, ERRESC error flag goes high, and the receiver waits until the transmitter returns to the Stop state. The MIPI D-PHY applies Spaced-One-Hot encoding (a Mark state is interleaved with a Space state) on commands and data.

Each symbol consists of the following two parts:

■ One-Hot phase

■ Space state

To transmit one bit, a Mark-1 should be sent followed by the Space state. In the case of a zero bit, a Mark-0 should be sent followed by Space state.

Table 35-4 Possible Escape Mode Sequences for Data Lanes

Escape Mode Action	Entry Command Pattern	Command Type
Low-Power Data Transmission	8'b11100001	mode
Ultra-Lower Power State	8'b00011110	mode
Reset Trigger	8'b01100010	trigger
Unknown-3	8'b01011101	trigger

Unknown-4	8’b00100001	trigger
Unknown-5	8’b10100000	trigger

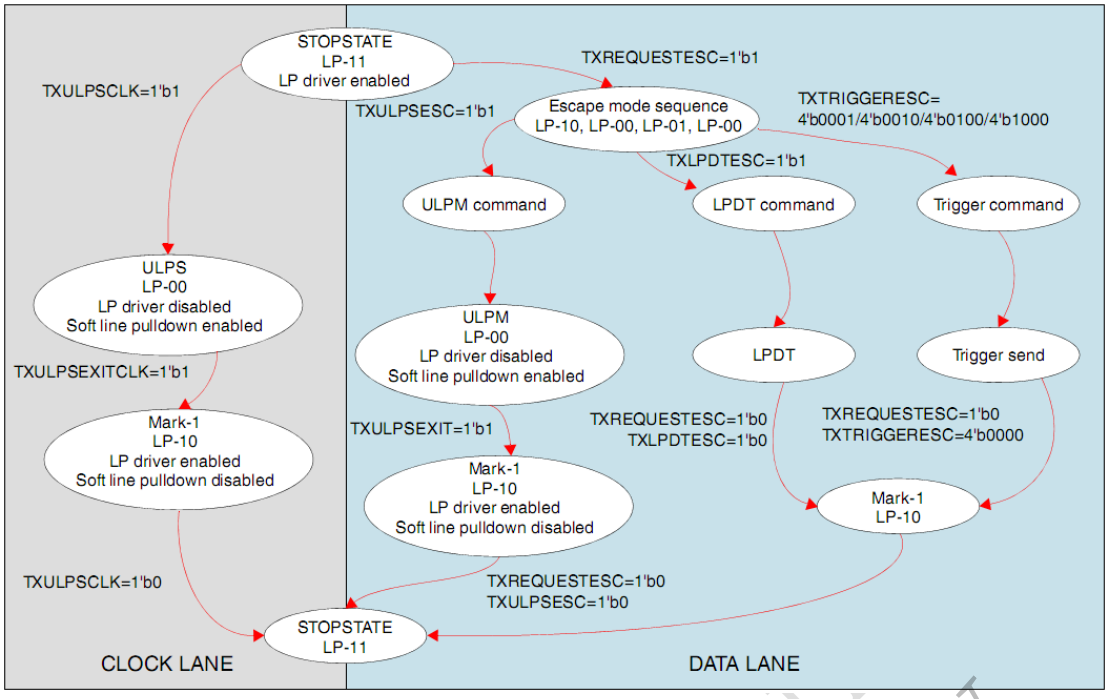


Fig. 35-6 Escape Mode Sequences State Diagram

35.4 Register Description

35.4.1 Registers Summary

Ref 9.6 Control/Test Codes of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

35.4.2 Detail Register Description

Ref 9.6 Control/Test Codes of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

35.5 Application Notes

35.5.1 PLL Requirements

Ref 6 PLL Requirements of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

35.5.2 Calibration Requirements

Ref 7 Calibration Requirements of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

35.5.3 Electrical and Timing Information

The following Tables provides the electrical and timing characteristics of MIPI D-PHY, the following conditions are applicable unless otherwise noted:

- Vdd (core) = 1.0V
- Vdd (I/O) = 1.8V
- $Ta^{o} = T_{min}$ to T_{max}

Table 35-5 DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input DC Specifications – Apply to CLKP/N and DATAP/N Inputs						
V_I	Input signal voltage range		-50		1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \leqslant V_I \leqslant V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode				uA
V_{GNDSH}	Ground shift		-50		50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level		-0.15		1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $V_{OH(absmax)}$				20	ns
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω $\leqslant R_L \leqslant$ 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω $\leqslant R_L \leqslant$ 125 Ω			14	mV
V_{CMTX}	Steady-state commond-mode output voltage	80 Ω $\leqslant R_L \leqslant$ 125 Ω	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 Ω $\leqslant R_L \leqslant$ 125 Ω			5	mV
V_{OHHS}	HS output high voltage	80 Ω $\leqslant R_L \leqslant$ 125 Ω			360	mV
Z_{OS}	Single-ended output impedance		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch				10	%
LP Line Drivers DC Specifications						
V_{OL}	Ouput Low-level SE voltage		-50		50	mV
V_{OH}	Ouput high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance		110			Ω
$\Delta Z_{OLP(01,10)}$	Single-ended ouput impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(00,11)}$	Single-ended ouput impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						

V_{IDTH}	Differential input high voltage threshold				70	mV
V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		880			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold				200	mV
V_{IHF}	Input high fault threshold		450			mV

35.5.4 Switching Characteristics

This section provides the various specifications for the switching characteristics of MIPI D-PHY

Table 35-6 Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Configuration Clock Specifications						
F_{CFG_CLK}	CFG_CLK frequency		17		27	MHz
DC_{CFG_CLK}	CFG_CLK duty cycle		40	50	60	%
HS Line Drivers AC Specifications						
-	Maximum Serial Data rate (forward direction)	On DATAP/N outputs. 80 Ω ⩽ R_L ⩽ 125 Ω	80		1500	Mbps
F_{DDRCLK}	DDR CLK frequency	On CLKP/N outputs	40		750	MHz
P_{DDRCLK}	DDR CLK period	80 Ω ⩽ R_L ⩽ 125 Ω	1.3		25	ns
UI_{INST}	UI instantaneous				12.5	ns[a]
ΔUI	UI variation		-10%		10%	UI[b]

			-5%		5%	UI[c]
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH}/P_{DDRCLK}$		50		%
t_{CPH}	DDR CLK high time			1		UI
t_{CPL}	DDR CLK low time			1		UI
-	DDR CLK/DATA Jittler[d]			75		ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI[e]
			-0.20		0.20	UI[f]
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI[g]
			0.20			UI[h]
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI[g]
			0.20			UI[h]
t_r	Differential output signal rise time	20% to 80%, R_L=50Ω			0.30	UI[i]
					0.35	UI[j]
			100			ps[k]
t_f	Differential output signal fall time	20% to 80%, R_L=50Ω			0.30	UI[i]
					0.35	UI[j]
			100			ps[k]
$\Delta V_{CMTX(HF)}$	Common level variation above 450MHz	80 Ω ≤ R_L ≤ 125 Ω			15	mVrms
$\Delta V_{CMTX(LF)}$	Common level variation between 50MHz and 450MHz	80 Ω ≤ R_L ≤ 125 Ω			25	mVp

Table 35-7 AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70pF			25	ns
t_{reot}		30% to 85%, C_L<70pF			35	ns
$\partial V/\partial t_{SR}$	Signal slew rate[l]	15% to 85%, C_L<70pF			150	mV/ns

C_L	Load capacitance		0		70	pF[m]
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50MHz and 450MHz		-50		50	mVpp
C_{CM}	Common mode termination				60	pF[n]
LP Line Receiver AC Specifications						
e^{SPIKE}	Input pulse rejection				300	V.ps
T_{MIN}	Minimum pulse response		20			ns
V_{INT}	Pk-to-Pk interference voltage				300	mVpp
f_{INT}	Interference frequency		450			MHz
Model Parameters Used for Driver Load Switching Performance Evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance				1	pF
C_{PIN}	Equivalent Signal Ended Package + PCB capacitance				2	pF
L_S	Euqivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

Notes:

a. This value corresponds to a minimum Mbps data rate.

b. When UI ⩾ 1ns, within a single burst.

c. When UI < 1ns, within a single burst.

d. Jitter specification with clean clock at REFCLK input.

*e. Total silicon and package skew delay budget of 0.3*UIINST when D-PHY is supporting maximum data rate = 1 Gbps.*

f. Total silicon and package skew delay budget of 0.4 UIINST when D-PHY is supporting maximum data rate > 1 Gbps.*

g. Total setup and hold window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1 Gbps.*

h. Total setup and hold window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1 Gbps.*

i. Applicable when operating at HS bit rates ⩽ 1 Gbps (UI ⩾ 1 ns).

j. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

k. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ⩽ 1 Gbps (UI ⩾ 1 ns), should not use

values below 150 ps.

l. Measured as average across any 50 mV of the output signal transition.

m. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

n. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.