Chapter 34 eDP TX Controller

34.1 Overview

This eDP TX IP is compliant with DisplayPort standard 1.2a and eDP 1.3. DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and consumer electronics (CE) industries. It consolidates the internal and external connection methods to reduce device complexity and cost, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

This DisplayPort 1.2 specification defines a scalable digital display interface with optional content protection capability for broad application within PC and CE devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a notebook PC for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of box-to-box applications for DisplayPort include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

It supports following features:

- Compliant with DisplayPortTM Specification, Version 1.2.
- Compliant with eDPTM Specification, Version 1.3.
- HDCP v1.3 amendment for DisplayPortTM Revision 1.0.
- Main link containing 4 physical lanes of 2.7/1.62 Gbps/lane
- TX PHY lanes, control pins and hot-plug pins are shared by the DisplayPort Source
- Bi-directional auxiliary link with up to 1Mbps speed.
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format.
- Video and audio slave mode
- Support PSR
- I2S audio interface
- 2,4,6,8-ch PCM - IEC60958 compliant
- S/PDIF audio interface
- Encoded bit stream (Dolby Digital, or DTS) – IEC61937 compliant
- APB slave bus interface
- Hot plug and unplug detection and link status monitor.
- Support VESA DMT and CVT timing standards.
- Fully support EIA/CEA-861Dvideo timing and Info Frame structure.
- Supports reading of the display EDID whenever the display is connected to power, even an AC-trickle power.
- Up to 0.5% down-spreading support at high-speed link.
- Supports DDC/CI and MCCS command transmission when the monitor includes a display controller.
- Flexible output channel mapping and polarity setting.
- PRBS or programmable transmitter pattern for main link quality test.
- Integrated HDCP encryption engine for transmitting protected audio and video content
- SPSRAM interface to read external encrypted HDCP key
- 24 Mhz crystal clock input.

- Built-in video and audio BIST patterns.
- 28nm LP CMOS process with Core voltage 0.9V (min)/ 1.0V (typ)/ 1.08V (max) @ global corner.

34.2 Block Diagram

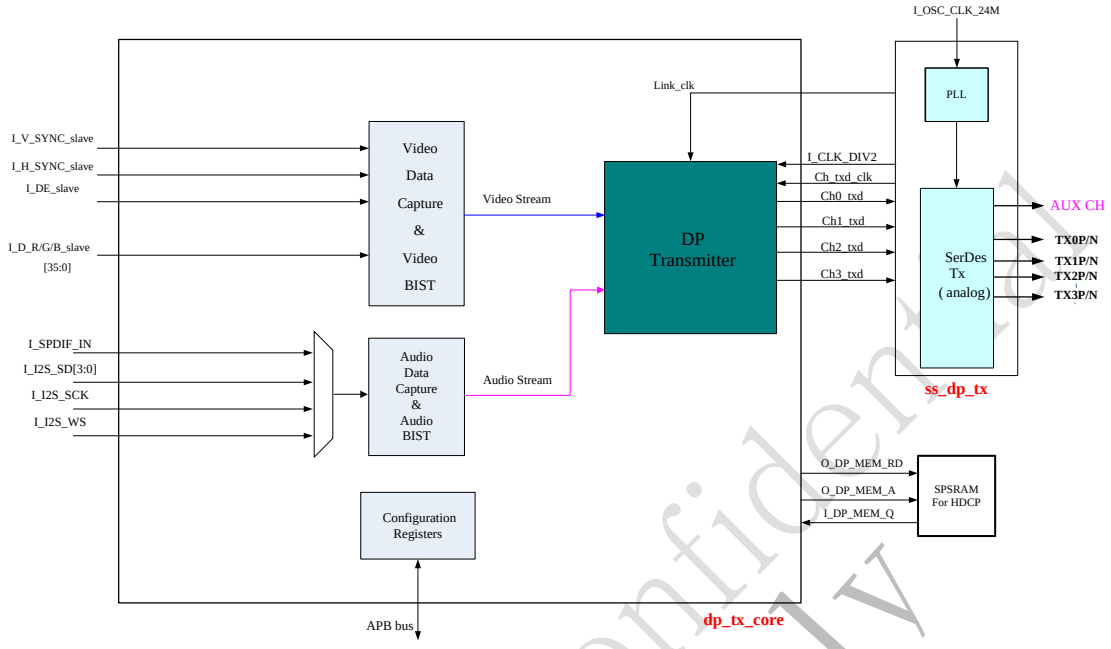

Fig. 34-1 eDP TX controller Block Diagram

Fig.1-1 shows the block diagram of eDP TX controller in top level. The video data and clock are sent directly from the VOP0 or VOP1.

The audio input has 2 interfaces, SPDIF and I2S.

The video data capture & video BIST block is separated as video_capture and display_bist module. The audio data capture & audio BIST block is separated as audio_capture and audio_bist. The block before SerDes is DP_TX main module. Following Table shows the brief function description of each sub-module.

Table 34-1 Brief function description of each module in top level

Module Name in Top Level	Brief Module Function Description
video_capture	Capture block of video data.
display_bist	Generation of arbitrary video format with three types of video data. The output of display_bist module will input to video_capture module directly if display BIST mode is active.
audio_capture	Capture block of audio data.
audio_bist	Generation of the audio BIST pattern.
dp_tx	DisplayPort transmitter block.
apb_slave_top	APB slave Bus interface

34.3 Function Description

34.3.1 eDP in SoC

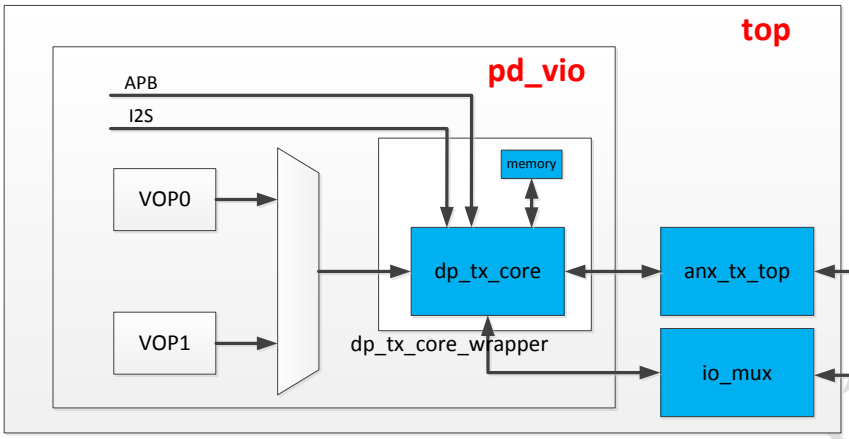

Fig. 34-2 eDP in SoC

There is a 512x8bits memory used to store the HDCP keys in the eDP controller. When GRF_SOC_CON8[13] (grf_edp_mem_ctrl_sel) = 1'b0, the memory is controlled by APB bus. When GRF_SOC_CON8[13] (grf_edp_mem_ctrl_sel) = 1'b1, the memory is controlled by eDP controller.

Please refer to "eDP TX IP Rockchip Datasheet.docx" for detail information.

34.4 Register Description

Please refer to "eDP TX IP Rockchip Datasheet.docx" for detail information.

34.5 Interface Description

34.5.1 Video Input Source

In RK3288, the eDP TX video source comes from vop0 or vop1.

- GRF_SOC_CON6[5] == 1'b0, video source from vop0.
- GRF_SOC_CON6[5] == 1'b1, video source from vop1.

34.5.2 Audio Input Source

In RK3288, the eDP TX audio source can come from I2S_8CH and SPDIF, and the SPDIF source comes from SPDIF_2CH or SPDIF_8CH.

- GRF_SOC_CON2[1] == 1'b0, SPDIF source from SPDIF_8CH.
- GRF_SOC_CON2[1] == 1'b1, SPDIF source from SPDIF_2CH

34.5.3 Hot plug

There is a hot plug input signal to eDP TX. This signal is muxed with GPIO7_B[3], and is enabled by "GPIO7B_IOMUX[7:6] = 2'b10".

34.6 Application Notes

Please refer to "eDP TX IP Rockchip Datasheet.docx" for detail information.