Chapter 33 LVDS

33.1 Overview

LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Using a differential signal reduces the system's susceptibility to noise and EMI emissions. In addition, using a differential signal can deliver high speeds. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications.

LVDS supports following features:

- Comply with the TIA/EIA-644-A LVDS standard
- Combine LVTTL IO, support LVDS/LVTTL data output
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 30/24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, every channel include 4 data lanes and 1 clock lane
- Support MSB mode and LSB mode data transfer
- Support APB slave bus interface
- Support low power mode

33.2 Block Diagram

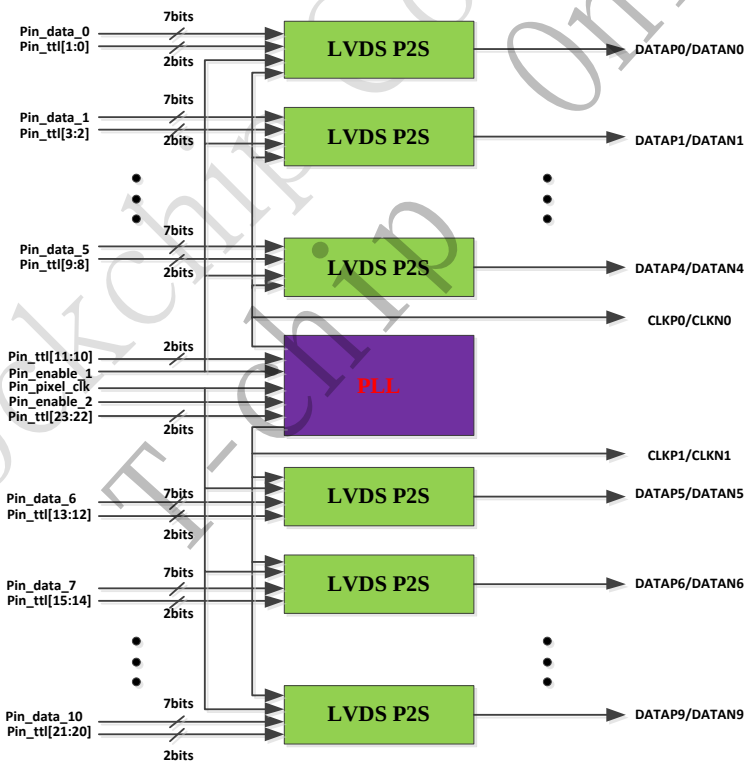

Fig. 33-1 LVDS Block Diagram

Fig.1-1 shows the brief block diagram of the innosilicon LVDS/TTL PHY, which includes ten LVDS P2S modules and one PLL module.

PLL is responsible for multiplying the pin_pixel_clk by 7, which generates a 7X clock used to deserialize the parallel data.

LVDS P2S module implements the parallel to serial function and transmits the TTL data directly.

33.3 Function Description

33.3.1 Transmitter with Two 35:5 Data Channels

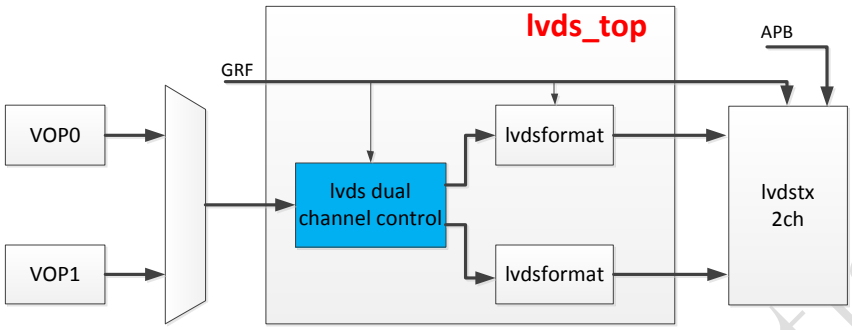

Fig. 33-2 LVDS in SoC

There are two transfer channels in LVDS, every channel include 4 data lanes and 1 clock lane. LVDS can work at single channel mode or double channel mode.

The LVDS output data timing is showed as the following figure,

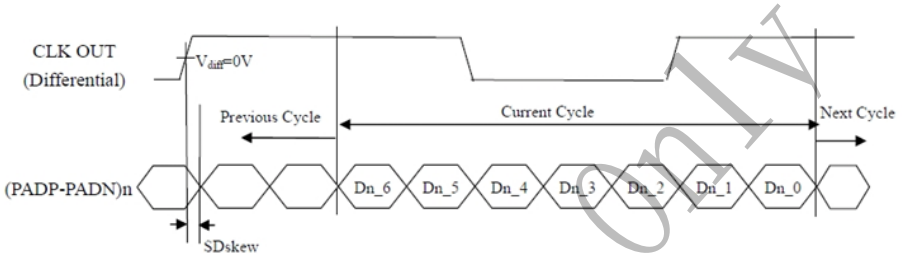

Fig. 33-3 LVDS output data timing

33.3.2 LVDS Format

Lvdsformat converts VOP RGB interface to LVDS format data. The lvdsformat support RGB 10/8/6bits color data input. There are two lvdsformat modules in the lvds_top.

When LVDS works at double channel mode, both the lvdsformat modules are necessary. One is for odd cycle RGB data format convert, and the other is for even cycle RGB data format convert. The frequency of LVDS output clock is half of the dclk.

When LVDS works at single channel mode, only one lvdsformat module is necessary. User can configure GRF register to select which lvdsformat converts the VOP RGB data. The frequency of LVDS output clock is equal to the dclk.

Table 33-1 is the MSB mapping relationship between the input data and output data of lvdsformat module (single channel mode). The LSB mapping relationship is opposite to MSB.

Table 33-1 MSB mapping relationship (single channel mode)

lvds-format id	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
			format-1	format-2	format-1	format-2	format-3	
lvds-format *	DATA0	DATA0[0]	R0	R4	R0	R2	R2	R0
		DATA0[1]	R1	R5	R1	R3	R3	R1

		DATA0[2]	R2	R6	R2	R4	R4	R2
		DATA0[3]	R3	R7	R3	R5	R5	R3
		DATA0[4]	R4	R8	R4	R6	R6	R4
		DATA0[5]	R5	R9	R5	R7	R7	R5
		DATA0[6]	G0	G4	G0	G2	G2	G0
	DATA1	DATA1[0]	G1	G5	G1	G3	G3	G1
		DATA1[1]	G2	G6	G2	G4	G4	G2
		DATA1[2]	G3	G7	G3	G5	G5	G3
		DATA1[3]	G4	G8	G4	G6	G6	G4
		DATA1[4]	G5	G9	G5	G7	G7	G5
		DATA1[5]	B0	B4	B0	B2	B2	B0
		DATA1[6]	B1	B5	B1	B3	B3	B1
	DATA2	DATA2[0]	B2	B6	B2	B4	B4	B2
		DATA2[1]	B3	B7	B3	B5	B5	B3
		DATA2[2]	B4	B8	B4	B6	B6	B4
		DATA2[3]	B5	B9	B5	B7	B7	B5
		DATA2[4]	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
		DATA2[5]	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
	DATA3	DATA3[0]	R6	R2	R6	R0	GND	GND
		DATA3[1]	R7	R3	R7	R1	GND	GND
		DATA3[2]	G6	G2	G6	G0	GND	GND
		DATA3[3]	G7	G3	G7	G1	GND	GND
		DATA3[4]	B6	B2	B6	B0	GND	GND
		DATA3[5]	B7	B3	B7	B1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
	DATA4	DATA4[0]	R8	R0	GND	GND	GND	GND
		DATA4[1]	R9	R1	GND	GND	GND	GND
		DATA4[2]	G8	G0	GND	GND	GND	GND
		DATA4[3]	G9	G1	GND	GND	GND	GND
		DATA4[4]	B8	B0	GND	GND	GND	GND
		DATA4[5]	B9	B1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND
	CLKOUT	CLKOUT	DCLK	DCLK	DCLK	DCLK	DCLK	DCLK

Table 33-2 is the MSB mapping relationship between the input data and output data of lvdsformat module (double channel mode). The LSB mapping relationship is opposite to MSB.

Table 33-2 MSB mapping relationship (double channel mode)

lvds-format id	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
			format-1	format-2	format-1	format-2	format-3	
lvds-format 0	DATA0	DATA0[0]	OR0	OR4	OR0	OR2	OR2	OR0
		DATA0[1]	OR1	OR5	OR1	OR3	OR3	OR1
		DATA0[2]	OR2	OR6	OR2	OR4	OR4	OR2

		DATA0[3]	OR3	OR7	OR3	OR5	OR5	OR3
		DATA0[4]	OR4	OR8	OR4	OR6	OR6	OR4
		DATA0[5]	OR5	OR9	OR5	OR7	OR7	OR5
		DATA0[6]	OG0	OG4	OG0	OG2	OG2	OG0
	DATA1	DATA1[0]	OG1	OG5	OG1	OG3	OG3	OG1
		DATA1[1]	OG2	OG6	OG2	OG4	OG4	OG2
		DATA1[2]	OG3	OG7	OG3	OG5	OG5	OG3
		DATA1[3]	OG4	OG8	OG4	OG6	OG6	OG4
		DATA1[4]	OG5	OG9	OG5	OG7	OG7	OG5
		DATA1[5]	OB0	OB4	OB0	OB2	OB2	OB0
		DATA1[6]	OB1	OB5	OB1	OB3	OB3	OB1
	DATA2	DATA2[0]	OB2	OB6	OB2	OB4	OB4	OB2
		DATA2[1]	OB3	OB7	OB3	OB5	OB5	OB3
		DATA2[2]	OB4	OB8	OB4	OB6	OB6	OB4
		DATA2[3]	OB5	OB9	OB5	OB7	OB7	OB5
		DATA2[4]	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
		DATA2[5]	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
	DATA3	DATA3[0]	OR6	OR2	OR6	OR0	GND	GND
		DATA3[1]	OR7	OR3	OR7	OR1	GND	GND
		DATA3[2]	OG6	OG2	OG6	OG0	GND	GND
		DATA3[3]	OG7	OG3	OG7	OG1	GND	GND
		DATA3[4]	OB6	OB2	OB6	OB0	GND	GND
		DATA3[5]	OB7	OB3	OB7	OB1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
	DATA4	DATA4[0]	OR8	OR0	GND	GND	GND	GND
		DATA4[1]	OR9	OR1	GND	GND	GND	GND
		DATA4[2]	OG8	OG0	GND	GND	GND	GND
		DATA4[3]	OG9	OG1	GND	GND	GND	GND
		DATA4[4]	OB8	OB0	GND	GND	GND	GND
		DATA4[5]	OB9	OB1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND
	CLKOUT	CLKOUT	DCLK/2	DCLK/2	DCLK/2	DCLK/2	DCLK/2	DCLK/2
lvds-format 1	DATA0	DATA0[0]	ER0	ER4	ER0	ER2	ER2	ER0
		DATA0[1]	ER1	ER5	ER1	ER3	ER3	ER1
		DATA0[2]	ER2	ER6	ER2	ER4	ER4	ER2
		DATA0[3]	ER3	ER7	ER3	ER5	ER5	ER3
		DATA0[4]	ER4	ER8	ER4	ER6	ER6	ER4
		DATA0[5]	ER5	ER9	ER5	ER7	ER7	ER5
		DATA0[6]	EG0	EG4	EG0	EG2	EG2	EG0
	DATA1	DATA1[0]	EG1	EG5	EG1	EG3	EG3	EG1
		DATA1[1]	EG2	EG6	EG2	EG4	EG4	EG2
		DATA1[2]	EG3	EG7	EG3	EG5	EG5	EG3
		DATA1[3]	EG4	EG8	EG4	EG6	EG6	EG4
		DATA1[4]	EG5	EG9	EG5	EG7	EG7	EG5

		DATA1[5]	EB0	EB4	EB0	EB2	EB2	EB0
		DATA1[6]	EB1	EB5	EB1	EB3	EB3	EB1
	DATA2	DATA2[0]	EB2	EB6	EB2	EB4	EB4	EB2
		DATA2[1]	EB3	EB7	EB3	EB5	EB5	EB3
		DATA2[2]	EB4	EB8	EB4	EB6	EB6	EB4
		DATA2[3]	EB5	EB9	EB5	EB7	EB7	EB5
		DATA2[4]	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
		DATA2[5]	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
	DATA3	DATA3[0]	ER6	ER2	ER6	ER0	GND	GND
		DATA3[1]	ER7	ER3	ER7	ER1	GND	GND
		DATA3[2]	EG6	EG2	EG6	EG0	GND	GND
		DATA3[3]	EG7	EG3	EG7	EG1	GND	GND
		DATA3[4]	EB6	EB2	EB6	EB0	GND	GND
		DATA3[5]	EB7	EB3	EB7	EB1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
	DATA4	DATA4[0]	ER8	ER0	GND	GND	GND	GND
		DATA4[1]	ER9	ER1	GND	GND	GND	GND
		DATA4[2]	EG8	EG0	GND	GND	GND	GND
		DATA4[3]	EG9	EG1	GND	GND	GND	GND
		DATA4[4]	EB8	EB0	GND	GND	GND	GND
		DATA4[5]	EB9	EB1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND

33.3.3 GRF Relative Register Description

GRF_SOC_CON6[3] (grf_con_lvds_lcdc_sel):

- 1'b0: lvds video source from vop0;
- 1'b1: lvds video source from vop1;

GRF_SOC_CON7[2:0] (grf_lvds_con_select):

- 3'b000: select RGB8 bits format-1;
- 3'b001: select RGB8 bits format-2;
- 3'b010: select RGB8 bits format-3;
- 3'b011: select RGB6 bits format;
- 3'b100: select RGB10 bits format-1;
- 3'b101: select RGB10 bits format-2;

GRF_SOC_CON7[3] (grf_lvds_con_msbsel):

- 1'b0: LSB for lvdsformat;
- 1'b1: MSB for lvds format;

GRF_SOC_CON7[4] (grf_lvds_con_chasel):

- 1'b0: single channel mode;
- 1'b1: double channel mode;

GRF_SOC_CON7[5] (grf_lvds_con_startsel):

- 1'b0: when lvds works at single channel mode, select lvdsformat 0 for RGB data convert;
- 1'b1: when lvds works at single channel mode, select lvdsformat 1 for RGB data convert;

GRF_SOC_CON7[6] (grf_lvds_con_ttl_en):

- 1'b0: disable lvds ttl mode;
- 1'b1: enable lvds ttl mode;

GRF_SOC_CON7[7] (grf_lvds_con_startphase):

- 1'b0: dclk_div2 start phase reset to 0 at beginning of hs;
- 1'b1: dclk_div2 start phase reset to 1 at beginning of hs;

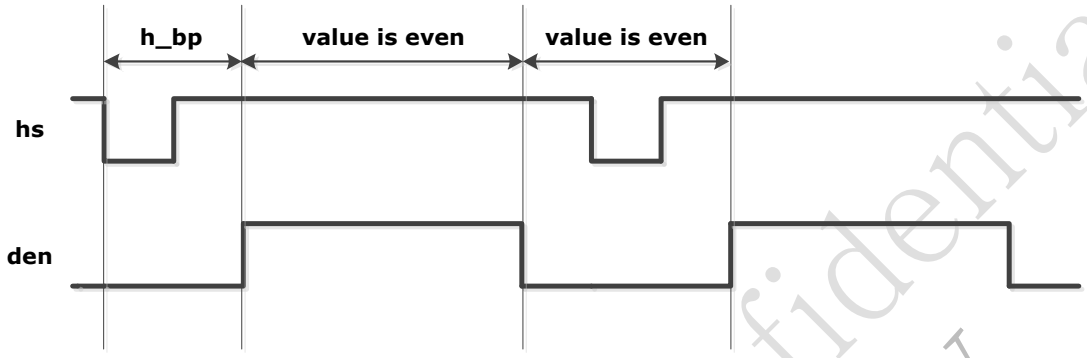

Fig. 33-4 LVDS h_bp timing diagram

when h_bp is odd, grf_lvds_con_startphase need be configured to 1'b1;

when h_bp is even, grf_lvds_con_startphase need be configured to 1'b0;

GRF_SOC_CON7[8] (grf_lvds_con_clkinv):

- 1'b0: not invert the clock to LVDS from lvds_top;
- 1'b1: invert the clock to LVDS from lvds_top;

GRF_SOC_CON7[9] (grf_lvds_con_hs_polarity):

- 1'b0: hsync polarity low active;
- 1'b1: hsync polarity high active;

GRF_SOC_CON7[10] (grf_lvds_con_den_polarity):

- 1'b0: den polarity high active;
- 1'b1: den polarity low active;

GRF_SOC_CON7[11] (grf_lvds_con_enable_1):

- 1'b0: LVDS channel 1 disable;
- 1'b1: LVDS channel 1 enable;

GRF_SOC_CON7[12] (grf_lvds_con_enable_2):

- 1'b0: LVDS channel 2 disable;
- 1'b1: LVDS channel 2 enable;

GRF_SOC_CON7[15] (grf_lvds_pwrdwn):

- 1'b0: LVDS not power down;

- 1’b1: LVDS power down;

33.4 Register Description

This section describes the control/status registers of the design.

33.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
LVDS_channel0_reg00	0x0000	W	0x000000bf	LVDS register
LVDS_channel0_reg01	0x0004	W	0x0000003f	LVDS register
LVDS_channel0_reg02	0x0008	W	0x0000007e	LVDS register
LVDS_channel0_reg03	0x000c	W	0x00000046	LVDS register
LVDS_channel0_reg04	0x0010	W	0x00000000	LVDS register
LVDS_channel0_reg05	0x0014	W	0x00000000	LVDS register
LVDS_config_reg0c	0x0030	W	0x00000000	LVDS register
LVDS_channel0_reg0d	0x0034	W	0x0000000a	LVDS register
LVDS_channel0_reg20	0x0080	W	0x00000045	LVDS register
LVDS_config_reg21	0x0084	W	0x00000000	LVDS register
LVDS_channel1_reg40	0x0100	W	0x000000bf	LVDS register
LVDS_channel1_reg41	0x0104	W	0x0000003f	LVDS register
LVDS_channel1_reg42	0x0108	W	0x0000007e	LVDS register
LVDS_channel1_reg43	0x010c	W	0x00000046	LVDS register
LVDS_channel1_reg44	0x0110	W	0x00000000	LVDS register
LVDS_channel1_reg45	0x0114	W	0x00000000	LVDS register
LVDS_channel1_reg4d	0x0134	W	0x0000000a	LVDS register
LVDS_channel1_reg60	0x0180	W	0x00000045	LVDS register

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

33.4.2 Detail Register Description

LVDS_channel0_reg00
Address: Operational Base + offset (0x0000)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	lvds_mode_en 1'b1: enable lvds mode; 1'b0: disable lvds mode;
6	RW	0x0	ttl_mode_en 1'b1: enable ttl mode; 1'b0: disable ttl mode;
5	RW	0x1	lane_en_ck 1'b1: enable lane_ck; 1'b0: disable lane_ck;
4	RW	0x1	lane_en_4 1'b1: enable lane_4; 1'b0: disable lane_4;
3	RW	0x1	lane_en_3 1'b1: enable lane_3; 1'b0: disable lane_3;
2	RW	0x1	lane_en_2 1'b1: enable lane_2; 1'b0: disable lane_2;
1	RW	0x1	lane_en_1 1'b1: enable lane_1; 1'b0: disable lane_1;
0	RW	0x1	lane_en_0 1'b1: enable lane_0; 1'b0: disable lane_0;

LVDS_channel0_reg01
Address: Operational Base + offset (0x0004)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	biasen_ck 1'b1: enable lane_ck bias; 1'b0: disable lane_ck bias;
4	RW	0x1	biasen_4 1'b1: enable lane_4 bias; 1'b0: disable lane_4 bias;
3	RW	0x1	biasen_3 1'b1: enable lane_3 bias; 1'b0: disable lane_3 bias;

Bit	Attr	Reset Value	Description
2	RW	0x1	biasen_2 1'b1: enable lane_2 bias; 1'b0: disable lane_2 bias;
1	RW	0x1	biasen_1 1'b1: enable lane_1 bias; 1'b0: disable lane_1 bias;
0	RW	0x1	biasen_0 1'b1: enable lane_0 bias; 1'b0: disable lane_0 bias;

LVDS_channel0_reg02
Address: Operational Base + offset (0x0008)
LVDS register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	lane_lvds_en_ck 1'b1: enable lane_ck lvds mode; 1'b0: disable lane_ck lvds mode;
5	RW	0x1	lane_lvds_en_4 1'b1: enable lane_4 lvds mode; 1'b0: disable lane_4 lvds mode;
4	RW	0x1	lane_lvds_en_3 1'b1: enable lane_3 lvds mode; 1'b0: disable lane_3 lvds mode;
3	RW	0x1	lane_lvds_en_2 1'b1: enable lane_2 lvds mode; 1'b0: disable lane_2 lvds mode;
2	RW	0x1	lane_lvds_en_1 1'b1: enable lane_1 lvds mode; 1'b0: disable lane_1 lvds mode;
1	RW	0x1	lane_lvds_en_0 1'b1: enable lane_0 lvds mode; 1'b0: disable lane_0 lvds mode;
0	RW	0x0	pll_fbdiv_8 pll_fbdiv[8];

LVDS_channel0_reg03
Address: Operational Base + offset (0x000c)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x46	pll_fbdiv_7_to_0 pll_fbdiv[7:0];

LVDS_channel0_reg04
Address: Operational Base + offset (0x0010)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_en_ck 1'b1: enable lane_ck ttl mode; 1'b0: disable lane_ck ttl mode;
4	RW	0x0	lane_ttl_en_4 1'b1: enable lane_4 ttl mode; 1'b0: disable lane_4 ttl mode;
3	RW	0x0	lane_ttl_en_3 1'b1: enable lane_3 ttl mode; 1'b0: disable lane_3 ttl mode;
2	RW	0x0	lane_ttl_en_2 1'b1: enable lane_2 ttl mode; 1'b0: disable lane_2 ttl mode;
1	RW	0x0	lane_ttl_en_1 1'b1: enable lane_1 ttl mode; 1'b0: disable lane_1 ttl mode;
0	RW	0x0	lane_ttl_en_0 1'b1: enable lane_0 ttl mode; 1'b0: disable lane_0 ttl mode;

LVDS_channel0_reg05
Address: Operational Base + offset (0x0014)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_ctr_ck 1'b1: enable lane_ck ttl data transmission; 1'b0: disable lane_ck ttl data transmission;
4	RW	0x0	lane_ttl_ctr_4 1'b1: enable lane_4 ttl data transmission; 1'b0: disable lane_4 ttl data transmission;
3	RW	0x0	lane_ttl_ctr_3 1'b1: enable lane_3 ttl data transmission; 1'b0: disable lane_3 ttl data transmission;
2	RW	0x0	lane_ttl_ctr_2 1'b1: enable lane_2 ttl data transmission; 1'b0: disable lane_2 ttl data transmission;
1	RW	0x0	lane_ttl_ctr_1 1'b1: enable lane_1 ttl data transmission; 1'b0: disable lane_1 ttl data transmission;
0	RW	0x0	lane_ttl_ctr_0 1'b1: enable lane_0 ttl data transmission; 1'b0: disable lane_0 ttl data transmission;

LVDS_config_reg0c
Address: Operational Base + offset (0x0030)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	enable_pll 8'h00: enable pll;

LVDS_channel0_reg0d
Address: Operational Base + offset (0x0034)
LVDS register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0a	pll_prediv_4_to_0 pll_prediv[4:0];

LVDS_channel0_reg20
Address: Operational Base + offset (0x0080)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x45	msb_lsb_sel 8'h45: MSB; 8'h44: LSB;

LVDS_config_reg21
Address: Operational Base + offset (0x0084)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	enable_tx 8'h00: disable tx; 8'h92: enable tx;

LVDS_channel1_reg40
Address: Operational Base + offset (0x0100)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	lvds_mode_en 1'b1: enable lvds mode; 1'b0: disable lvds mode;

Bit	Attr	Reset Value	Description
6	RW	0x0	ttl_mode_en 1'b1: enable ttl mode; 1'b0: disable ttl mode;
5	RW	0x1	lane_en_ck 1'b1: enable lane_ck; 1'b0: disable lane_ck;
4	RW	0x1	lane_en_4 1'b1: enable lane_4; 1'b0: disable lane_4;
3	RW	0x1	lane_en_3 1'b1: enable lane_3; 1'b0: disable lane_3;
2	RW	0x1	lane_en_2 1'b1: enable lane_2; 1'b0: disable lane_2;
1	RW	0x1	lane_en_1 1'b1: enable lane_1; 1'b0: disable lane_1;
0	RW	0x1	lane_en_0 1'b1: enable lane_0; 1'b0: disable lane_0;

LVDS_channel1_reg41
Address: Operational Base + offset (0x0104)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	biasen_ck 1'b1: enable lane_ck bias; 1'b0: disable lane_ck bias;
4	RW	0x1	biasen_4 1'b1: enable lane_4 bias; 1'b0: disable lane_4 bias;
3	RW	0x1	biasen_3 1'b1: enable lane_3 bias; 1'b0: disable lane_3 bias;
2	RW	0x1	biasen_2 1'b1: enable lane_2 bias; 1'b0: disable lane_2 bias;
1	RW	0x1	biasen_1 1'b1: enable lane_1 bias; 1'b0: disable lane_1 bias;
0	RW	0x1	biasen_0 1'b1: enable lane_0 bias; 1'b0: disable lane_0 bias;

LVDS_channel1_reg42
Address: Operational Base + offset (0x0108)
LVDS register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	lane_lvds_en_ck 1'b1: enable lane_ck lvds mode; 1'b0: disable lane_ck lvds mode;
5	RW	0x1	lane_lvds_en_4 1'b1: enable lane_4 lvds mode; 1'b0: disable lane_4 lvds mode;
4	RW	0x1	lane_lvds_en_3 1'b1: enable lane_3 lvds mode; 1'b0: disable lane_3 lvds mode;
3	RW	0x1	lane_lvds_en_2 1'b1: enable lane_2 lvds mode; 1'b0: disable lane_2 lvds mode;
2	RW	0x1	lane_lvds_en_1 1'b1: enable lane_1 lvds mode; 1'b0: disable lane_1 lvds mode;
1	RW	0x1	lane_lvds_en_0 1'b1: enable lane_0 lvds mode; 1'b0: disable lane_0 lvds mode;
0	RW	0x0	pll_fbdiv_8 pll_fbdiv[8];

LVDS_channel1_reg43
Address: Operational Base + offset (0x010c)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x46	pll_fbdiv_7_to_0 pll_fbdiv[7:0];

LVDS_channel1_reg44
Address: Operational Base + offset (0x0110)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_en_ck 1'b1: enable lane_ck ttl mode; 1'b0: disable lane_ck ttl mode;
4	RW	0x0	lane_ttl_en_4 1'b1: enable lane_4 ttl mode; 1'b0: disable lane_4 ttl mode;

Bit	Attr	Reset Value	Description
3	RW	0x0	lane_ttl_en_3 1'b1: enable lane_3 ttl mode; 1'b0: disable lane_3 ttl mode;
2	RW	0x0	lane_ttl_en_2 1'b1: enable lane_2 ttl mode; 1'b0: disable lane_2 ttl mode;
1	RW	0x0	lane_ttl_en_1 1'b1: enable lane_1 ttl mode; 1'b0: disable lane_1 ttl mode;
0	RW	0x0	lane_ttl_en_0 1'b1: enable lane_0 ttl mode; 1'b0: disable lane_0 ttl mode;

LVDS_channel1_reg45
Address: Operational Base + offset (0x0114)
LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_ctr_ck 1'b1: enable lane_ck ttl data transmission; 1'b0: disable lane_ck ttl data transmission;
4	RW	0x0	lane_ttl_ctr_4 1'b1: enable lane_4 ttl data transmission; 1'b0: disable lane_4 ttl data transmission;
3	RW	0x0	lane_ttl_ctr_3 1'b1: enable lane_3 ttl data transmission; 1'b0: disable lane_3 ttl data transmission;
2	RW	0x0	lane_ttl_ctr_2 1'b1: enable lane_2 ttl data transmission; 1'b0: disable lane_2 ttl data transmission;
1	RW	0x0	lane_ttl_ctr_1 1'b1: enable lane_1 ttl data transmission; 1'b0: disable lane_1 ttl data transmission;
0	RW	0x0	lane_ttl_ctr_0 1'b1: enable lane_0 ttl data transmission; 1'b0: disable lane_0 ttl data transmission;

LVDS_channel1_reg4d
Address: Operational Base + offset (0x0134)
LVDS register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0a	pll_prediv_4_to_0 pll_prediv[4:0];

LVDS_channel1_reg60
Address: Operational Base + offset (0x0180)
LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x45	msb_lsb_sel 8'h45: MSB; 8'h44: LSB;

33.5 Interface Description

In RK3288, the LVDS video source comes from vop0 or vop1.

- GRF_SOC_CON6[3] == 1'b0, video source from vop0.
- GRF_SOC_CON6[3] == 1'b1, video source from vop1.

33.6 Application Notes

Following is the operation flow which describes how the software configures the registers to start lvds data transmission.

- Select the video source by GRF register;
- Select single channel mode or double channel mode by GRF register;
- Select data transfer format by GRF register;
- Enable lvds pll by LVDS registers;
- Enable lvds transfer by LVDS registers;