Chapter 32 HDMI TX

32.1 Overview

HDMI TX is fully compliant with HDMI 1.4a and 2.0a specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMI TX consists of one HMDI transmitter controller and one HMDI transmitter PHY.

It supports following features:

- Video formats:
  - All CEA-861-E video formats up to 1080p at 60 Hz and 720p/1080i at 120 Hz
  - Optional HDMI 1.4b video formats
  - HDMI 2.0 video formats, All CEA-861-F video formats
- Colorimetry, 24/30-bit RGB 4:4:4
- Pixel clock from 13.5 MHz up to 600 MHz
- Up to 192 kHz IEC60958 audio sampling rate
- Flexible synchronous enable per clock domain to set functional power down modes
- AMBA APB 3.0 register access
- I2C DDC, EDID block read mode
- SCDC I2C DDC access
- TMDS Scrambler to enable support for 2160p@60Hz with RGB 4:4:4
- Integrated CEC hardware engine

32.2 Block Diagram

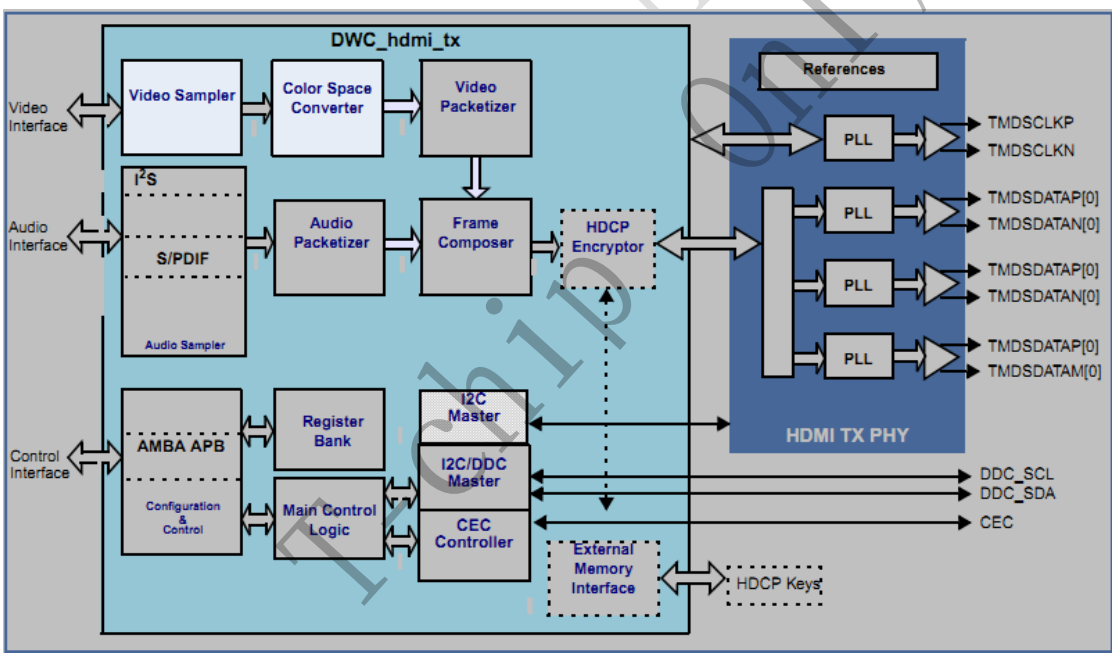

Fig. 32-1 HDMI TX Block Diagram

32.3 Function Description

32.3.1 Video Data Processing

The video processing contain video format timings, pixel encodings(RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

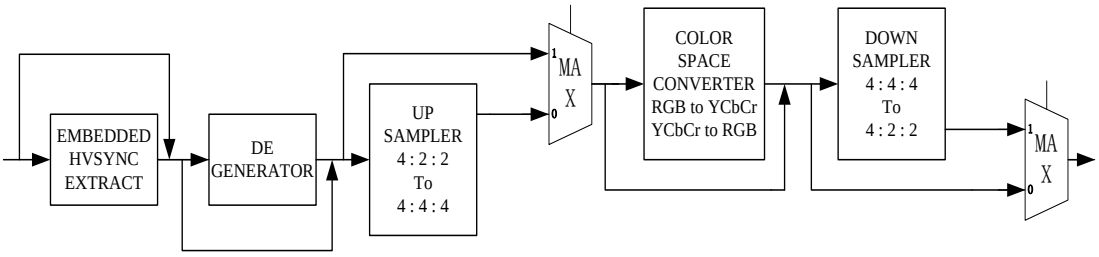

Fig. 32-2 HDMI Video Data Processing

The input video pixels can be encoded in either RGB, YCBCR 4:4:4 or YCBCR 4:2:2 formats by Color Space Conversion block.

The input Video data can have a pixel size of 24, 30bits. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

The following interface timing diagram outlines the Video interface signal format. 24 bit data (we also support 36 bit data for deep color) in RGB can be captured by the rising edge of VCLK with 1ns setup time and 1ns hold time requirements. Control signals such DE and VSync/HSync/FSync going with the same timing relationship.

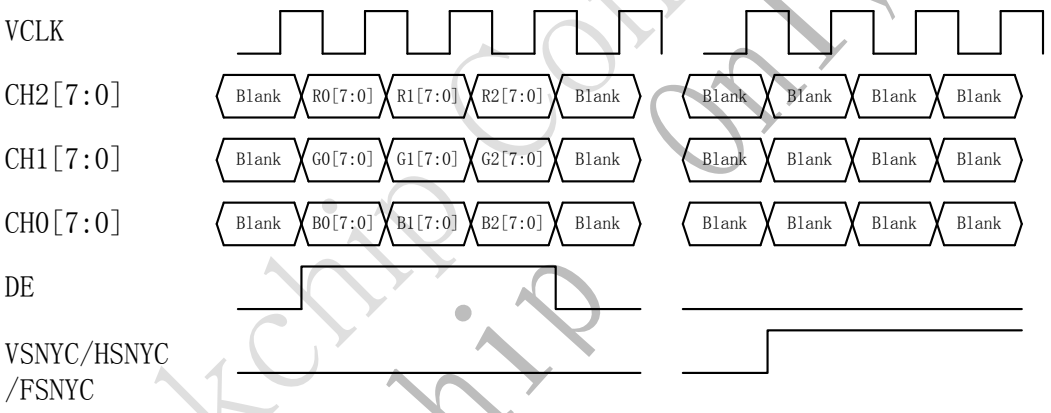

Fig. 32-3 HDMI Video Processing Timing

1. Video Data Capture Logic

HDMI TX support input video data related format table is listed below.

Table 32-1 HDMI Supported Input Video Formats

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
RGB	4:4:4	Separate	8	24
RGB	4:4:4	Separate	10	30
RGB	4:4:4	Separate	12	36
YCbCr	4:4:4	Separate	8	24
YCbCr	4:4:4	Separate	10	30
YCbCr	4:4:4	Separate	12	36
YCbCr	4:2:2	Separate	8	16
YCbCr	4:2:2	Separate	10	20

YCbCr	4:2:2	Separate	12	24
YCbCr	4:4:4	Embedded	8	24
YCbCr	4:4:4	Embedded	10	30
YCbCr	4:4:4	Embedded	12	36
YCbCr	4:2:2	Embedded	8	16
YCbCr	4:2:2	Embedded	10	20
YCbCr	4:2:2	Embedded	12	24

2. Embedded Sync Extraction Module

The module is used to extract Vsync and Hsync signals from input video data stream such as ITU656 format. With setting the relative registers, this functional module can extract correct video sync signals for later process block using.

3. Data Enable (DE) Generator

HDMI Transmitter has DE signal generator by incoming HSYNCs, VSYNCs and Video clock. External DE is optional and selected by appropriate register settings. This feature is particularly useful when interfacing to MPEG decoders that do not provide a specific DE output signal.

4. Color Space Conversion

HDMI Transmitter Color space conversion (CSC) is available to interface for several MPEG decoders like with YCbCr-only outputs, and to provide full DVI backwards compatibility.

The function of this module is to perform color space conversion functionality as listed below.

(1). Convert RGB input Video data to YCbCr Video data.

(2). Convert YCbCr input Video data to RGB Video data.

(3). upsample for YCbCr 4:2:2 to YCbCr 4:4:4

(4). downsample for YCbCr 4:4:4 to YCbCr 4:2:2

32.3.2 Audio Data Processing

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks

The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.

The scheme of audio processing as shown in the figure below:

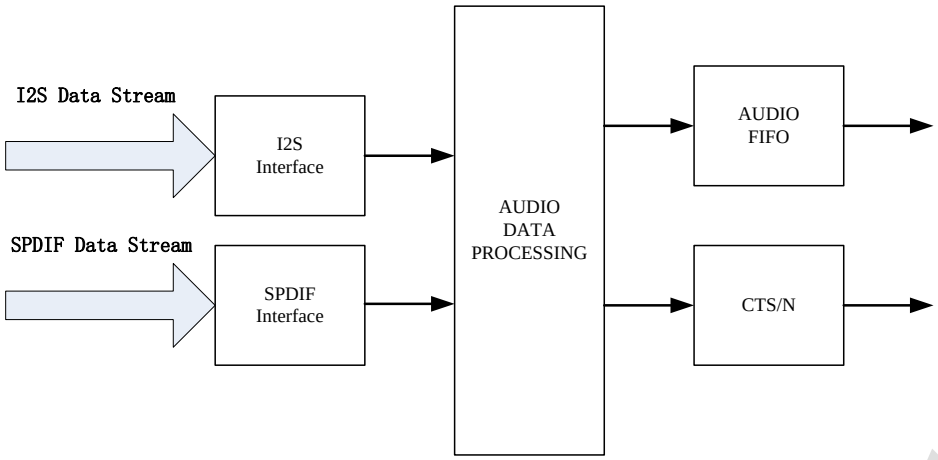

Fig. 32-4 HDMI Audio Data Processing Diagram

1.I2S

The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table 32-2 HDMI TX I2S 2 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 32-3 HDMI TX I2S 8 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.SPDIF

The function of this module is to implement SPDIF audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. SPDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. SPDIF input supports audio sampling rates from 32 to 192 KHz. The following shows the SPDIF audio formats that are supported for each of the video formats

Table 32-4 HDMI SPDIF Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

3.Audio Sample Clock Capture and Regeneration

Audio data being carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sink then re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be.

$$128 \cdot fS = fTMDS\_clock \cdot N / CTS.$$

The scheme of the Audio Sample Clock Capture and Regeneration as shown below:

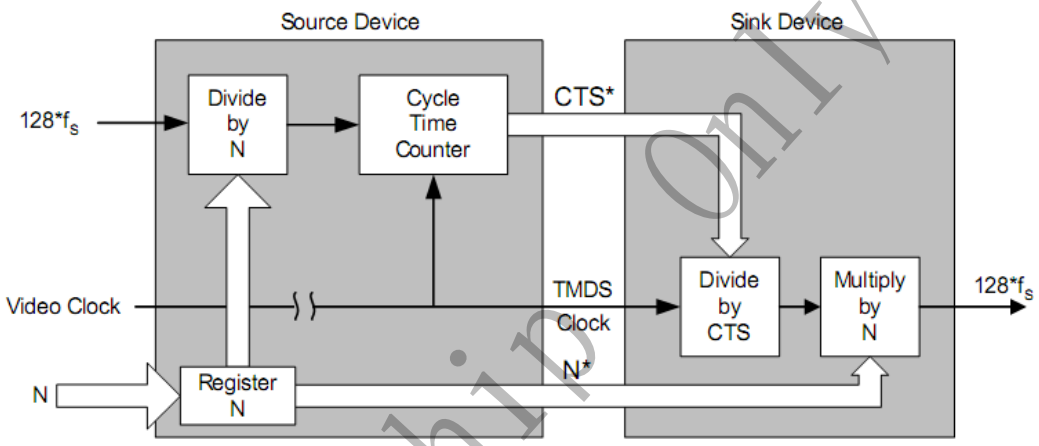

Fig. 32-5 HDMI Audio Clock Regeneration Model

Because there is no audio clock carried through the HDMI link,only the TMDS clock is used.Software sets the CTS/N with a value taken form the below table,which shows the CTS and N value for the supported standard.All other TMDS clocks are not supported;The TMDS clocks divided or multiplied by 1,001 coefficients are not supportd.

Table 32-5 HDMI CTS and N table

	TMDS Clock (MHz)													
	25.2		27		54		74.25		148.5		297		597	
Fs (kHZ)	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS
32	4096	25200	4096	27000	4096	54000	4096	74250	4096	148500	3072	222750	3072	445500
44.1	6272	28000	6272	30000	6272	60000	6272	82500	6272	165000	4704	247500	9408	990000
48	6144	25200	6144	27000	6144	54000	6144	74250	6144	148500	5120	247500	6144	495000
88.2	12544	28000	12544	30000	12544	60000	12544	82500	12544	165000	9408	247500	18816	990000
96	12288	25200	12288	27000	12288	54000	12288	74250	12288	148500	10240	247500	12288	495000
176.4	25088	28000	25088	30000	25088	60000	25088	82500	25088	165000	18816	247500	37632	990000
192	24576	25200	24576	27000	24576	54000	24576	74250	24576	148500	20480	247500	24576	4950000

32.3.3 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HMDI Transmitter Controller has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

32.3.4 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

32.3.5 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

32.3.6 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

32.3.7 TMDS encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data.

HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

32.3.8 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

32.4 Register Description

The address offset of the HDMI TX is 0xff980000,it contains 16 address section.The offset of the table of Register Summary must multiple with 4 when software configure it。Like the Interrupt registers，its base address is 0x0100.If we want to configure it, its real address is 0xff980000+0x0100*4.

We can configure the HDMI PHY register through the internal I2C interface. The internal I2C register interface map with the address which from 0x3020. We just to configure the register which can trigger one i2c write or i2c read. For example, we configure the PLL through these register.

32.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
Identification Registers	0x0000	B		Identification releated registers
Interrupt registers	0x0100	B		Interrupt releated registers
Video Sampler registers	0x0200	B		Video Sampler registers
Video Packetizer registers	0x0800	B		Video Packetizer registers
Frame Composer Registers	0x1000	B		Frame Composer Registers
HDMI Source PHY Registers	0x3000	B		HDMI Source PHY Registers
I2C Master PHY Registers	0x3020	B		I2C Master PHY Registers
Audio Sampler Registers	0x3100	B		Audio Sampler Registers
Main Controller Registers	0x4000	B		Main Controller Registers
Color Space Converter Registers	0x4100	B		Color Space Converter Registers
HDCP Encryption Engine Registers	0x5000	B		HDCP Encryption Engine Registers
HDCP BKSV Registers	0x7800	B		HDCP BKSV Registers
HDCP AN Registers	0x7805	B		HDCP AN Registers
Encrypted DPK Embedded Storage Registers	0x780E	B		Encrypted DPK Embedded Storage Registers
CEC Engine Registers	0x7D00	B		CEC Engine Registers
I2C Master Registers	0x7E00	B		I2C Master Registers for E-DDC/SCDC

For the detail register description,please see the doc：DWC_hdmi_tx_databook.pdf and dwc_hdmi_tx_ew_6gbps-gf28slp18_databook_rockchip.pdf

32.5 Interface Description

32.5.1 Video Input Source

In RK3288, the HDMI TX video source comes from VOP_BIG and VOP_LIT.

32.5.2 Audio Input Source

In RK3288, the HDMI TX audio source comes from I2S_8CH or SPDIF_2CH.

32.6 Application Notes

This chapter describes how to bring up HDMI transmitter in your system. As shown few examples below, these introduce the basically HDMI transmitter application, likes, the Hot Plug Detect, EDID read back, multiple audio format input and different video resolution displaying.

You can easily configure these functions with proper registers value setting by HDMI TX APB BUS.

32.6.1 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Just do the step, reset the HDMI TX.

32.6.2 Hot Plug Detection

Hot Plug Detect is a special feature for HDMI transmitter spying the state on the HDMI port.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The following is a step by step instruction for detecting the hot plug in and out.

Hot Plug in Steps:

Step1: Write 1'b1 in the phy_conf0.enhpdrxsense bit field register..

Step2: Plug HDMI receiver in.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the phy_stat0.HPD bit field register. If HPD=0,the Hot Plug signal is low(no Sink(Receiver) detected). If HPD=1,the Hot Plug signal is high(Sink(Receiver) detected).

Hot Plug out Steps:

Step1: HDMI transmitter at working state.

Step2: Plug HDMI receiver out.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the phy_stat0.HPD bit field register. If HPD=0,the Hot Plug signal is low(no Sink(Receiver) detected). If HPD=1,the Hot Plug signal is high(Sink(Receiver) detected).

32.6.3 Reading EDID

Read EDID is a function that can make the HDMI transmitter to read the HDMI receiver's Extended Display Identification Data (EDID) in order to discover the HDMI receiver's configuration and capabilities. HDMI transmitter can choose the appropriate audio and video format for playing and displaying by the HDMI receiver through the use of the EDID. Besides, HDMI transmitter support the reading Enhanced Extended Display Identification Data (E-EDID) if HDMI receiver have this enhanced structure.

The following describes how to read E-EDID through HDMI transmitter. The total E-EDID is 512bytes data, which is divided into 2 segments. Each segment has 256bytes data. The Read E-EDID function is only read 64bytes data from HDMI receiver at each time. So, you must read 8 times that can read total 512bytes data back.

The related registers offset is 0x7E00.

Normal read E-EDID 512bytes Steps:

Step1: Set I2C slave address.
Write i2cm_slave.slaveaddr[6:0] bit field register.
Step2: Set I2C register address.
Write i2cm_slave.address[7:0] bit field register.
Step3: Activate Sequential Real operation.
Write "1" in the i2cm_operation.rd8 bit field register.
Step4: Wait for interruption
Wait for ii2cmasterdone interrupt in the ih_i2cm_stat0 register
Step5: Read data result
Read data of registers i2cm_read_buff0[7:0] to i2cm_read_buff7[7:0]

Read E-EDID extended sequential read operation Steps:

Step1: Set I2C slave address.
Write i2cm_slave.slaveaddr[6:0] bit field register.
Step2: Set I2C segment address.
Write the i2cm_segaddr.seg_addr bit field register.
Step3: Set I2C segment pointer.
Write i2cm_segptr.segptr bit field register.
Step4: Activate Read operation.
Write "1"in the i2cm_operation.rd8_ext bit field register.
Step5: Wait for interruption.
Wait for ii2cmasterdone interrupt in the ih_i2cm_stat0 register
Step6: Read data result.
Read data of registers i2cm_read_buff0[7:0] to i2cm_read_buff7[7:0].

32.6.4 Audio input configuration

HDMI transmitter audio support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 48K.

The following describes how to configure audio input format. The related register offset is from 0x3100.

Configure Audio Input Format with I2S Steps:

Step1: Select I2S input.
Write "1" in the aud_conf0.i2s_select bit field register.
Step2: Enable I2S inputs:
Write "1" in the aud_conf0.i2s_in_en[3:0] bit field register.
Step3: Set I2S Mode [Standard | Right-justified | Left-justified | Burst1 | Burst2]:
Write the aud_conf1.i2s_mode[2:0] bit field register.
Step4: Set I2S data width [16 bits up to 24 bits]:
Write the aud_conf1.i2s_width[4:0] bit field.

Configure Audio Input Format with SPDIF Steps:

Step1: Select SPDIF input.
Write "0" in the aud_conf0.i2s_select bit field register.
Step2: Set S/PDIF Linear-PCM or Non-Linear PCM audio samples:
Write the aud_spdif1.setnlpcm bit field register.
Step3: Set SPDIF data width [16 bits up to 24 bits]:
Write the aud_spdif1.spdif_width[4:0] bit field.

Configure Audio Parameters Steps:

Step1: Set Audio input frequency clock FS ratio factor [128 Fs | 256 Fs |512 Fs]:
Write the aud_inputclkfs.lfsfactor bit field register.
Step2: Set Audio fixed N factor for Audio Clock Regeneration. This factor depends on the audio sampling rate and video mode.
Write the aud_n1.audN, aud_n2.audN, and aud_n3.audN bit field registers.
Step3: Set Audio CTS factor for Audio Clock Regeneration. This factor can be generated automatically or manually.
For Automatic CTS generation
Write "0" on the bit field "CTS_manual", Register 0x3205: AUD_CTS3
For Manual CTS setting
Write "1" in the aud_cts3.CTS_manual register bit field.
Write the aud_cts1.audCTS, aud_cts2.audCTS, aud_cts3.audCTS bit field registers.
Step4: Enable Audio sampler block:
Write "0" in the mc_clkdis.audclk_disable bit field register.

32.6.5 Video input configuration

HDMI transmitter support RGB/YCbCr 24/30bit video input with different resolution. The default video format is RGB24bit input at resolution of 1080P@60. The following describes

how to configure video input format into RGB24bit input at resolution of 480P@60, 720P@60 or 1080P@60.

HDMI pin_vclk cannot get invert.

Video input requirement:

24bit RGB 4:4:4 Source.
Resolution is 480P@60, 720P@60 or 1080P@60.

Configure Video Input Format Steps:

Step1: To select the Video Mapping input mode (RGB444, YCC444, YCC422).
Write the video code in the tx_invid0.video_mapping bit field register.
Step2: Set video timing information configuration:
Write the fc_invidconf.vsync_in_polarity register.
Write the fc_invidconf.hsync_in_polarity register.
Write the fc_invidconf.de_in_polarity register.
Write the fc_invidconf.r_v_blank_in_osc register.
Write the fc_invidconf.in_I_P register.
H active pixels
- Write the fc_inhactiv1.H_in_activ register.
- Write the fc_inhactiv0.H_in_activ register.

V active pixels
- Write the fc_invactiv1.V_in_activ register.
- Write the fc_invactiv0.V_in_activ register.

H blanking pixels
Write the fc_inhblank0.H_in_blank register.
V blanking pixels
Write the fc_invblank.V_in_blank register.
HSync offset
Write the fc_hsyncindelay0.H_in_delay register.
VSync offset
Write the fc_vsyncindelay0.V_in_delay register.
HSync pulse width
Write the fc_hsyncinwidth0.H_in_width register.
VSync pulse width
Write the fc_vsyncinwidth0.V_in_width register.
Step3: Select DVI or HDMI mode:
Write "0" for DVI in the fc_invidconf.DVI_modez bit field register.
Write "1" for HDMI in the fc_invidconf.DVI_modez bit field register.

The detail configuration for AVI information, please refer to the HDMI specification (8.2.1) and CEA-861-D (6.3).

32.6.6 HDMI MPLL CONFIGURE

HDMI transmitter have a PLL for generate the TMDS clock. Configuring the PLL related parameter use the i2c master interface.

Configure HDMI PLL Step:

Step1: Place the PHY in configuration mode by writing 8'h32 to the phy_conf0 register.
Step2: Reset the PHY by writing 0x01 in the mc_phyrstz register.
Step3: Write the desired color depth and the pixel repetition in the vp_pr_cd register.
Step4: After a PHY-dependent time, it is required to lift the reset by writing 0x00 to the mc_phyrstz register.
Step5: Set the PHY slave address by writing 0x69 in the phy_i2cm_slave register.
Step6: According to dwc_hdmi_tx_ew_6gbps-gf28slp18_databook_rockchip.pdf, (Appendix B:MPLL Configuration)you are required to look up the configuration for your intended video mode and write those values to the PHY I2C interface. The baseline flow to write to the
PHY through the I2C interface is as follows:
i. Write the register address in the phy_i2cm_address register.
ii. Write data in the phy_i2cm_datao_1 (MSB, [15:8]) and phy_i2cm_datao_0 (LSB, [7:0]) registers.
iii. Initialize the write operation by writing 8'h10 in the phy_i2cm_operation register.
iv. Wait for a done interruption from the I2C master.
Step7: After all of the required PHY I2C registers have been configured, you now need to place the PHY in power-on mode by setting the txpwron bit in the PHY_CONF0 register, writing 8'h2a to the phy_conf0 register.
The mc_phyrstz register controls the PHY reset.
Step8: At the end of the PHY configuration, it is recommended to check if the PHY PLL is locked.
Read the phy_stat0.tx_phy_lock bit field register.
If tx_phy_lock = 0, the PLL is not locked.
If tx_phy_lock = 1, the PLL is locked.

32.6.7 CEC OPERATION

The CEC line is used for high-level user control of HDMI-connected devices.The HDMI TX contain CEC TX operations and CEC RX operations.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The register offset is from 0x7D00.

Configure The CEC Step:

Step1: Write the CEC logical address to cec_addr_l,cec_addr_h register
Step2: Write the size of the frame in bytes which are available in the transmitter data buffer to cec_tx_cnt register
Step3: Write the desired CEC data(including header and data blocks) to cec_tx_data0 to cec_tx_data15
Step4: Write 1 to cec_ctrl.send register, to start the cec transmit.

32.6.8 HDCP OPERATION

HDCP is designed to protect the transmission of Audiovisual Content between an HDCP Transmitter and an HDCP Receiver. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

The following is a step by step instruction for HDCP operation.

HDCP Access KSV Memory Step:

Step1: Request access to KSV memory through setting a_ksvmemctrl.KSVMEMrequest to 1'b1 and pool a_ksvmemctrl.KSVMEMaccess until this value is 1'b1 (access granted).

Step2: Read VH', M0, Bstatus, and the KSV FIFO.

The data is stored in the revocation memory, as provided in the "Address Mapping for Maximum Memory Allocation" table in the hdmi_databook.

HDCP Key Write Step: