Chapter 28 RGA2

28.1 Overview

RGA is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending and image blur/sharpness.

28.1.1 Features

- **Data format**
  - Input data: ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
  - Output data: ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio，from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT:
  - A+B=B only BitBLT, not support scale/rotate mode
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
- **Raster operation**
  - ROP2/ROP3/ROP4
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

28.2 Block Diagram

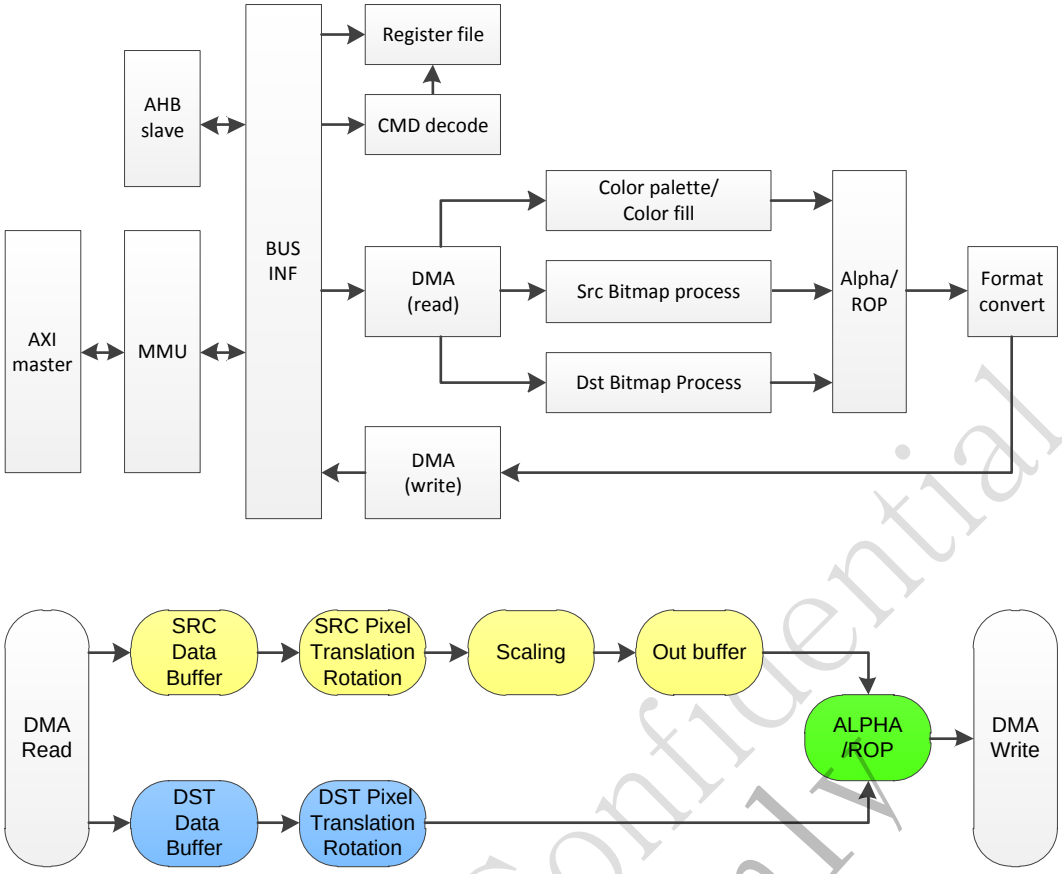


Fig. 28-1 RGA2 Block Diagram

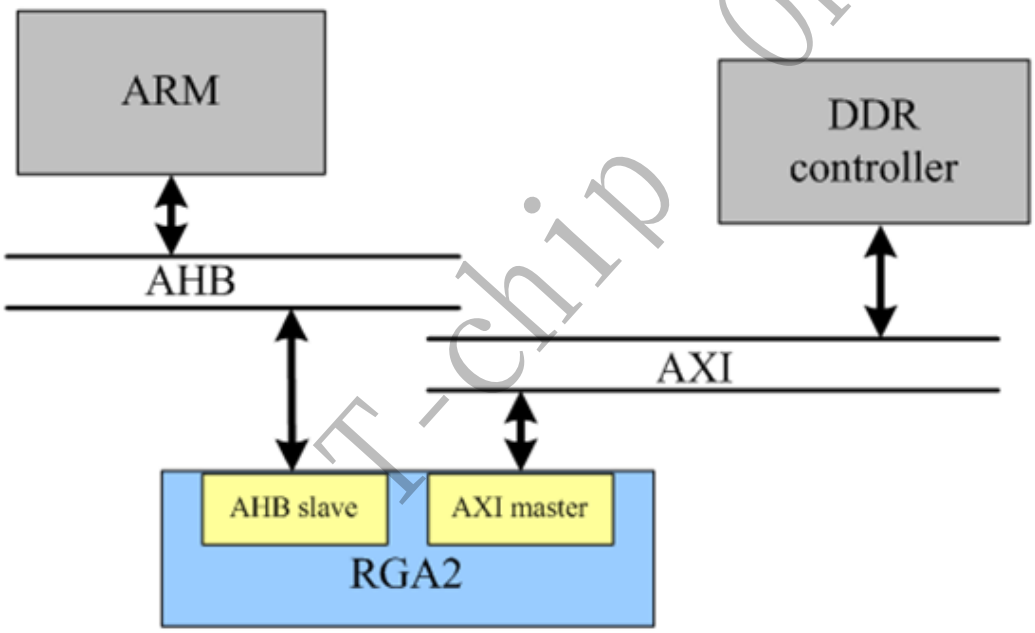


Fig. 28-2 RGA2 in SOC

28.3 Function Description

28.3.1 Data Format

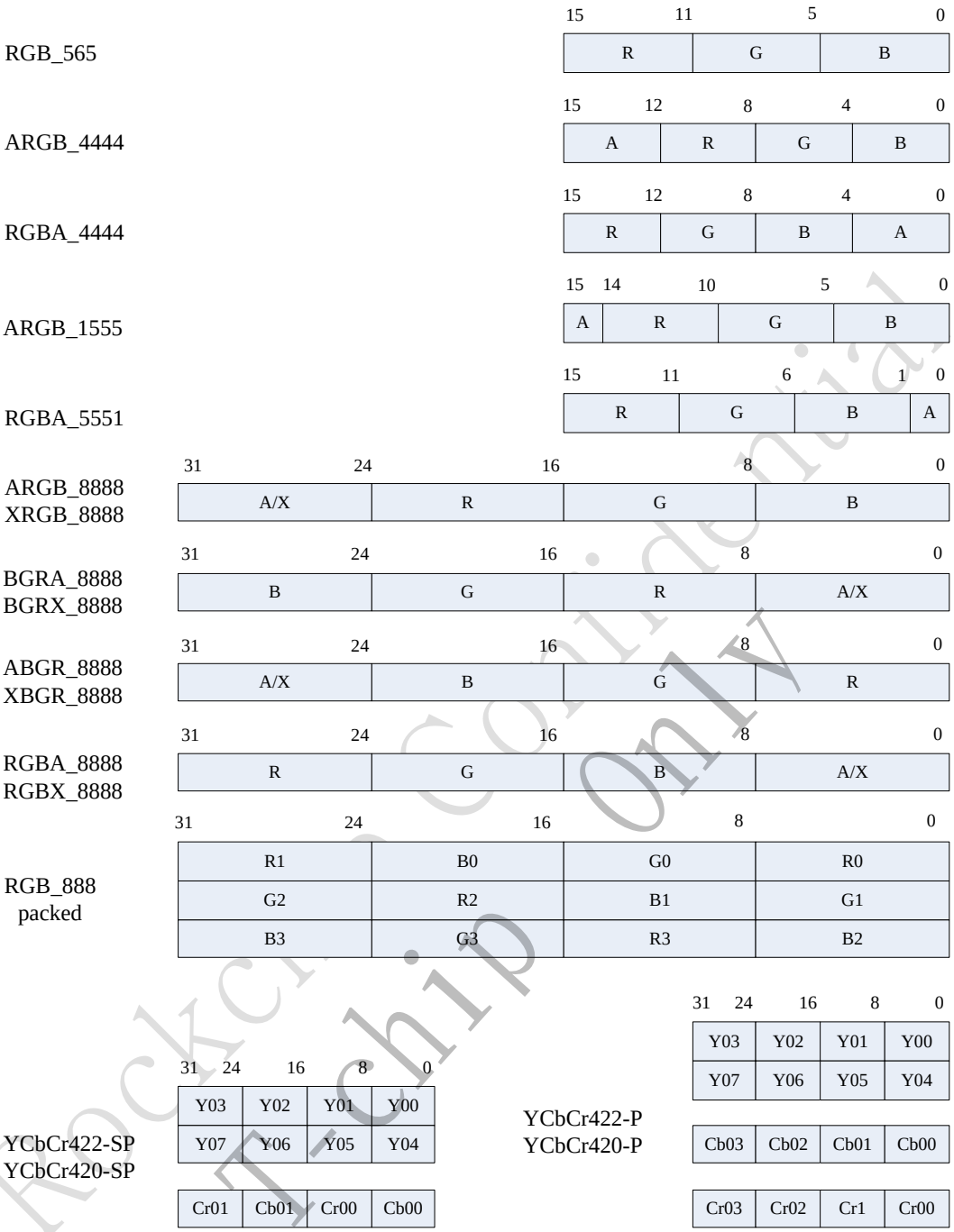


Fig. 28-3 RGA Input Data Format

All input datas (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

28.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

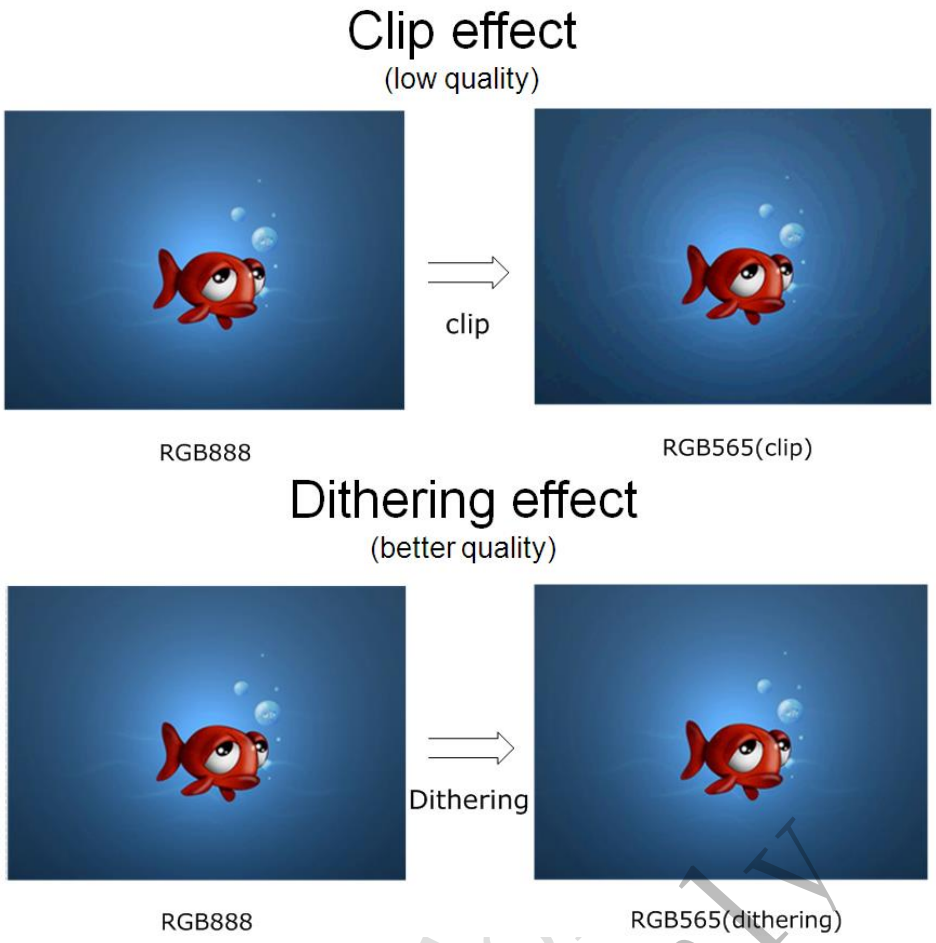
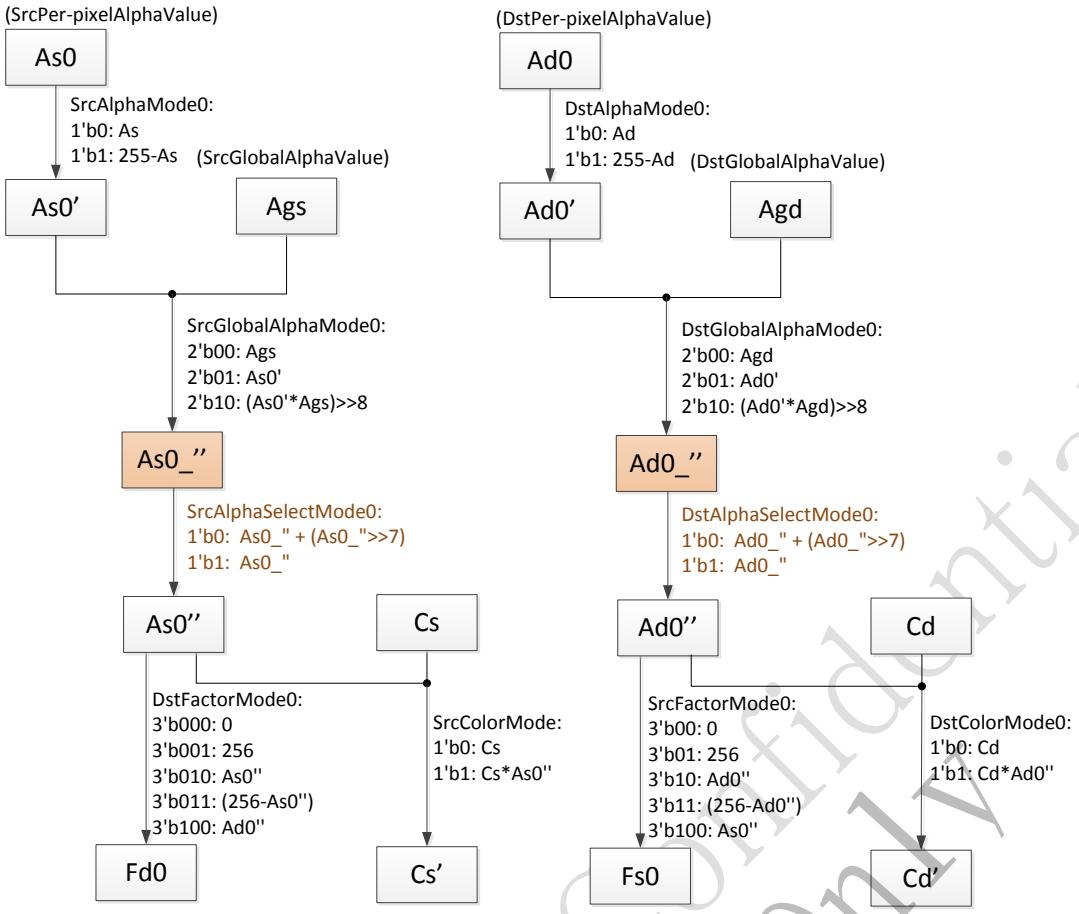


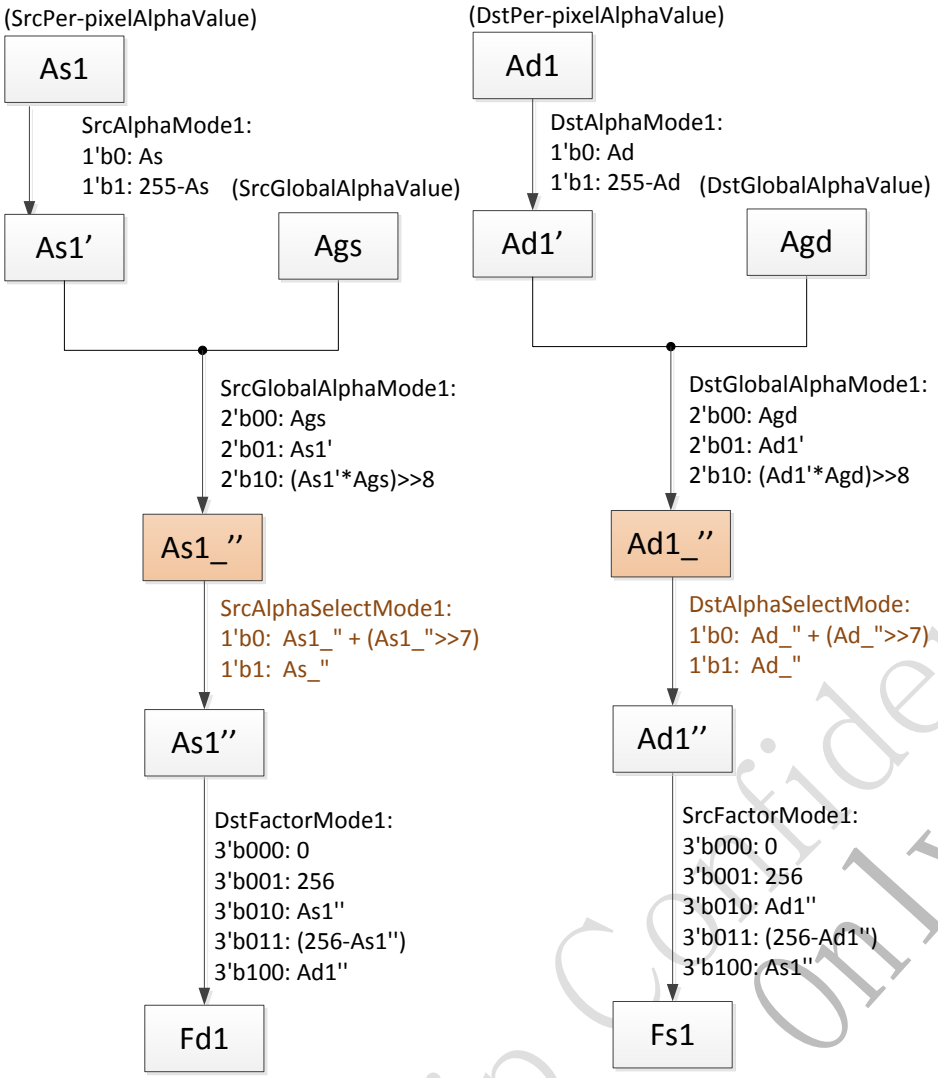
Fig. 28-4 RGA Dither effect

28.3.3 Alpha mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

28.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

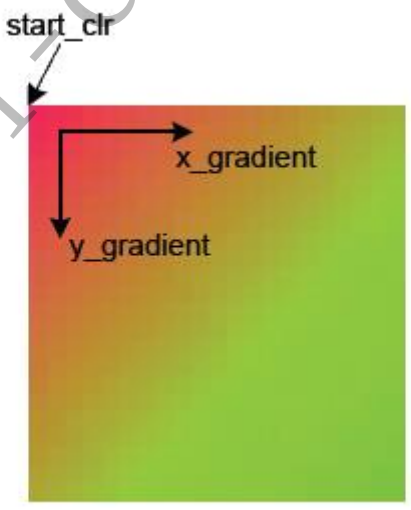


Fig. 28-5 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different coordinary.

```
A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;
```

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

28.3.5 Raster Operation (ROP)

Raster operation (ROP) is a Boolean operation between operands, which involve AND, OR, XOR, and NOT operations. For ROP2, operands are P (select pan) and D (Destination bitmap). For ROP3, operands are P (pattern), S (source bitmap) and D (Destination bitmap). For ROP4, operands are P (pattern), S (source bitmap), D (Destination bitmap) and MASK.

Table 28-1 RGA ROP Boolean operations

Operator	Meaning
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

28.3.6 Scaling

The scaling operation is the imageresizing processing of source image. Scaling is done base on ARGB8888 format.

There are three sampling modes: scale down (Average); scale up(Bi-cubic);

28.4 Register description

28.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
RGA2_RGA_SYS_CTRL	0x0000	W	0x00000004	RGA system control register
RGA2_RGA_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_RGA_CMD_BASE	0x0008	W	0x12345678	RGA command codes base address register
RGA2_RGA_STATUS	0x000c	W	0x00000000	RGA status register
RGA2_RGA_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_RGA_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_RGA_MMU_CMD_BASE	0x0018	W	0x00000000	Register0000 Abstract

Name	Offset	Size	Reset Value	Description
RGA2_RGA_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_RGA_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_RGA_SRC_BASE0	0x0108	W	0x00000000	source image Y/RGB base address
RGA2_RGA_SRC_BASE1	0x010c	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_RGA_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_RGA_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_RGA_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number
RGA2_RGA_SRC_ACT_INFO	0x011c	W	0x00000000	RGA source image active width/height register
RGA2_RGA_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_RGA_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_RGA_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_RGA_SRC_FG_COLOR	0x012c	W	0x00000000	RGA source image foreground color
RGA2_RGA_CP_GR_A	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_RGA_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_RGA_CP_GR_B	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_RGA_SRC_TR_COLOR1	0x0134	W	0x00000000	Register0000 Abstract
RGA2_RGA_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_RGA_DST_BASE0	0x013c	W	0x00000000	RGA destination image base address 0 register
RGA2_RGA_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_RGA_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_RGA_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register

Name	Offset	Size	Reset Value	Description
RGA2_RGA_DST_ACT_INFO	0x014c	W	0x00000000	RGA destination image active width/height register
RGA2_RGA_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_RGA_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Abstract
RGA2_RGA_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_RGA_PAT_CON	0x015c	W	0x00000000	Pattern size/offset register
RGA2_RGA_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_RGA_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register
RGA2_RGA_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_RGA_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_RGA_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_RGA_MMU_CTRL1	0x016c	W	0x00000000	RGA MMU control register 1
RGA2_RGA_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_RGA_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_RGA_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_RGA_MMU_ELS_BASE	0x017c	W	0x00000000	RGA ELSE MMU TLB base address

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

28.4.2 Detail Register Description

RGA2_RGA_SYS_CTRL

Address: Operational Base + offset (0x0000)

RGA system control register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	sw_auto_rst it would auto-resetn after one frame finish. 0: disable 1: enable

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 0：disable 1：enable
1	WO	0x0	sw_cmd_mode RGA command mode 0：slave mode 1：master mode
0	WO	0x0	sw_cmd_op_st_p RGA operation start bit Only used in passive (slave) control mode

RGA2_RGA_CMD_CTRL
Address: Operational Base + offset (0x0004)
RGA command control register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total cmd number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total cmd number would reset to RGA_INCR_CMD_NUM.

RGA2_RGA_CMD_BASE
Address: Operational Base + offset (0x0008)
RGA command codes base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x12345678	sw_cmd_base RGA command codes base address

RGA2_RGA_STATUS
Address: Operational Base + offset (0x000c)
RGA status register

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RW	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 0: idle 1: working

RGA2_RGA_INT
Address: Operational Base + offset (0x0010)
RGA interrupt register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag

Bit	Attr	Reset Value	Description
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

RGA2_RGA_MMU_CTRL0
Address: Operational Base + offset (0x0014)
RGA MMU control 0 register

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved
10:9	RW	0x0	sw_els_ch_priority
8:7	RW	0x0	sw_dst_ch_priority
6:5	RW	0x0	sw_src1_ch_priority
4:3	RW	0x0	sw_src_ch_priority
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 0: disable 1: enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 0: 4KB page 1: 64KB page

RGA2_RGA_MMU_CMD_BASE
Address: Operational Base + offset (0x0018)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_RGA_MODE_CTRL
Address: Operational Base + offset (0x0100)
RGA mode control register

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 0:clip 1:not-clip

Bit	Attr	Reset Value	Description
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key 0: disable 1: enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 0: solid color 1: pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 0: SRC + DST => DST 1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 000: Bitblt 001: Color palette 010: Rectangle fill 011: Update palette LUT/pattern ram

RGA2_RGA_SRC_INFO
Address: Operational Base + offset (0x0104)
RGA source information register

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:24	RW	0x0	sw_bic_coe_sel SRC bicubic scaling coefficient select 00: CATROM 01: MITCHELL 10: HERMITE 11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 0:disable 1:enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit

Bit	Attr	Reset Value	Description
18	RW	0x0	sw_src_trans_mode Source transparency mode 0: normal stencil test (color key) 1: inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 00：no scaling 01: down-scaling 10: up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 00：no scaling 01: down-scaling 10: up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 00: no mirror 01: x mirror 10: y mirror 11: x mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 00: 0 degree 01: 90 degree 10: 180 degree 11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 00: BT.601-range0 01: BT.601-range1 10: BT.709-range0 11: BT.709-range1
7	RW	0x0	sw_cp_endian Source Color palette endian swap 0: big endian 1: little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 0: ABGR 1: BGRA

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 0: BGR 1: RGB
3:0	RW	0x0	sw_src_fmt Source bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P 1100: 1BPP (color palette) 1101: 2BPP (color palette) 1110: 4BPP (color palette) 1111: 8BPP (color palette)

RGA2_RGA_SRC_BASE0
Address: Operational Base + offset (0x0108)
source image Y/RGB base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 source image Y/RGB base address

RGA2_RGA_SRC_BASE1
Address: Operational Base + offset (0x010c)
RGA source image Cb/Cbr base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 source image Cb base address (YUV422/420-P) source image Cb/Cr base address (YU,V422/420-SP)

RGA2_RGA_SRC_BASE2
Address: Operational Base + offset (0x0110)
RGA source image Cr base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_src_base2 source image Cr base address (YUV422/420-P)

RGA2_RGA_SRC_BASE3
Address: Operational Base + offset (0x0114)
RGA source image 1 base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base3 source image 1 RGB base address (source bitblt mode1)

RGA2_RGA_SRC_VIR_INFO
Address: Operational Base + offset (0x0118)
RGA source image virtual stride / RGA source image tile number

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride mask image virtual stride (words)
15	RW	0x0	Reserved
14:0	RW	0x0000	sw_src_act_width source image active width count from 1

RGA2_RGA_SRC_ACT_INFO
Address: Operational Base + offset (0x011c)
RGA source image active width/height register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2
28:16	RW	0x0000	sw_src_act_height source image active height
15:13	RW	0x0	Reserved1
12:0	RW	0x0000	sw_src_act_width source image active width

RGA2_RGA_SRC_X_FACTOR
Address: Operational Base + offset (0x0120)
RGA source image horizontal scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =(DST_ACT_WIDTH/SRC_ACT_WIDTH) * 65536

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(SRC_ACT_WIDTH/DST_ACT_WIDTH) * 65536

RGA2_RGA_SRC_Y_FACTOR
Address: Operational Base + offset (0x0124)
RGA source image vertical scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor (DST_ACT_HEIGHT/SRC_ACT_HEIGHT) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor (SRC_ACT_HEIGHT/DST_ACT_HEIGHT) * 65536

RGA2_RGA_SRC_BG_COLOR
Address: Operational Base + offset (0x0128)
RGA source image background color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_RGA_SRC_FG_COLOR
Address: Operational Base + offset (0x012c)
RGA source image foreground color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_RGA_CP_GR_A
Address: Operational Base + offset (0x0130)
RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_RGA_SRC_TR_COLOR0
Address: Operational Base + offset (0x0130)
RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin source image transparency color R min value

RGA2_RGA_CP_GR_B
Address: Operational Base + offset (0x0134)
RGA source image transparency color max value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_RGA_SRC_TR_COLOR1
Address: Operational Base + offset (0x0134)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax source image transparency color R max value

RGA2_RGA_DST_INFO
Address: Operational Base + offset (0x0138)
RGA destination format register

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved
18	RW	0x0	sw_dst_csc_clip BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip

Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_dst_csc_mode DST bitmap RGB2YUV conversion mode 00: Bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 00: 888 to 666 01: 888 to 565 10: 888 to 555 11: 888 to 444
13	RW	0x0	sw_dither_down DST dither down enable 0:disable 1:enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 0:disable 1:enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 0: ABGR 1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 0: BGR 1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 000: ABGR888 001: XBGR888 010: BGR packed 100: RGB565 101: ARGB1555 110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 0: ABGR 1: BGRA

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 0: BGR 1: RGB
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P

RGA2_RGA_DST_BASE0
Address: Operational Base + offset (0x013c)
RGA destination image base address 0 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 destination image Y/RGB base address

RGA2_RGA_DST_BASE1
Address: Operational Base + offset (0x0140)
RGA destination image base address 1 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 destination image Cb/CbCr base address

RGA2_RGA_DST_BASE2
Address: Operational Base + offset (0x0144)
RGA destination image base address 2 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 destination image Cr base address

RGA2_RGA_DST_VIR_INFO
Address: Operational Base + offset (0x0148)
RGA destination image virtual width/height register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2
30:16	RW	0x000	sw_src1_vir_stride source image 1 virtual stride (words)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	Reserved1
14:0	RW	0x000	sw_dst_vir_stride destination image virtual stride(words)

RGA2_RGA_DST_ACT_INFO
Address: Operational Base + offset (0x014c)
RGA destination image active width/height register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_RGA_ALPHA_CTRL0
Address: Operational Base + offset (0x0150)
Alpha control register 0

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 0: big endian 1: little endian
19:12	RW	0x00	sw_dst_global_alpha global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha global alpha value of SRC(Ags) fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 00: ROP 2 01: ROP 3 10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 0: alpha 1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 0: disable 1: enable

RGA2_RGA_ALPHA_CTRL1
Address: Operational Base + offset (0x0154)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 0: As 1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 0: Ad 1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1_'') 00: Ags 01: As1' 10: (As1'*Ags)>>8 11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1_'') 00: Agd 01: Ad1' 10: (Ad1'*Agd)>>8 11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1'') 0: As1''= As1_''+ (As1_''>>7) 1: As1''= As1 _''
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1'') 0: Ad1''= Ad1_'' + (Ad1_''>>7) 1: Ad1''= Ad1_''
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 000: 0 001: 256 010: Ad1'' 011: 256-Ad1'' 100: As1''

Bit	Attr	Reset Value	Description
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 000: 0 001: 256 010: As1'' 011: 256-As1'' 100: Ad1''
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0') 0: As 1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0') 0: Ad 1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_'') 00: Ags 01: As0' 10: (As0'*Ags)>>8 11: reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_'') 00: Agd 01: Ad0' 10: (Ad0'*Agd)>>8 11: reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0'') 0: As0''= As0_''+ (As0_''>>7) 1: As0''= As0 _''
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0'') 0: Ad0''= Ad0_'' + (Ad0_''>>7) 1: Ad0''= Ad0_''

Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 000: 0 001: 256 010: Ad0'' 011: 256-Ad0'' 100: As0''
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 000: 0 001: 256 010: As0'' 011: 256-As0'' 100: Ad0''
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 0: Cs 1: Cs * As0''
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 0: Cd 1: Cd * Ad0''

RGA2_RGA_FADING_CTRL
Address: Operational Base + offset (0x0158)
Fading control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_RGA_PAT_CON
Address: Operational Base + offset (0x015c)
Pattern size/offset register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset

Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_RGA_CP_GR_G
Address: Operational Base + offset (0x0160)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_RGA_ROP_CON0
Address: Operational Base + offset (0x0160)
ROP code 0 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24:0	RW	0x0000000	sw_rop3_code0 Rop3 code 0 control bits

RGA2_RGA_CP_GR_R
Address: Operational Base + offset (0x0164)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_RGA_ROP_CON1
Address: Operational Base + offset (0x0164)
ROP code 1 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24:0	RW	0x0000000	sw_rop3_code1 Rop3 code 1 control bits

RGA2_RGA_MASK_BASE
Address: Operational Base + offset (0x0168)
RGA mask base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base mask base address in ROP4 mode LUT/ pattern load base address

RGA2_RGA_MMU_CTRL1
Address: Operational Base + offset (0x016c)
RGA MMU control register 1

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 0: disable 1: enable
11	RW	0x0	sw_dst_mmu_prefetch_dir 0:forward 1:backward
10	RW	0x0	sw_dst_mmu_prefetch_en 0:disable 1:enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 0: disable 1: enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 0:forward 1:backward
6	RW	0x0	sw_src1_mmu_prefetch_en 0:disable 1:enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 0: disable 1: enable
3	RW	0x0	sw_src_mmu_prefetch_dir 0:forward 1:backward

Bit	Attr	Reset Value	Description
2	RW	0x0	sw_src_mmu_prefetch_en 0:disable 1:enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 0: disable 1: enable

RGA2_RGA_MMU_SRC_BASE
Address: Operational Base + offset (0x0170)
RGA source MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

RGA2_RGA_MMU_SRC1_BASE
Address: Operational Base + offset (0x0174)
RGA source1 MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

RGA2_RGA_MMU_DST_BASE
Address: Operational Base + offset (0x0178)
RGA destination MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

RGA2_RGA_MMU_ELS_BASE
Address: Operational Base + offset (0x017c)
RGA ELSE MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

28.5 Programming Guide

28.5.1 Register Partition

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

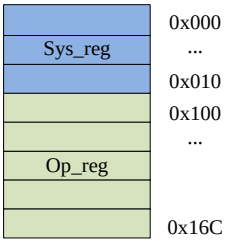


Fig. 28-6 HDMI TX Software Main Sequence Diagram

28.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[1] to '1'. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing '1' to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write '1' to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1)

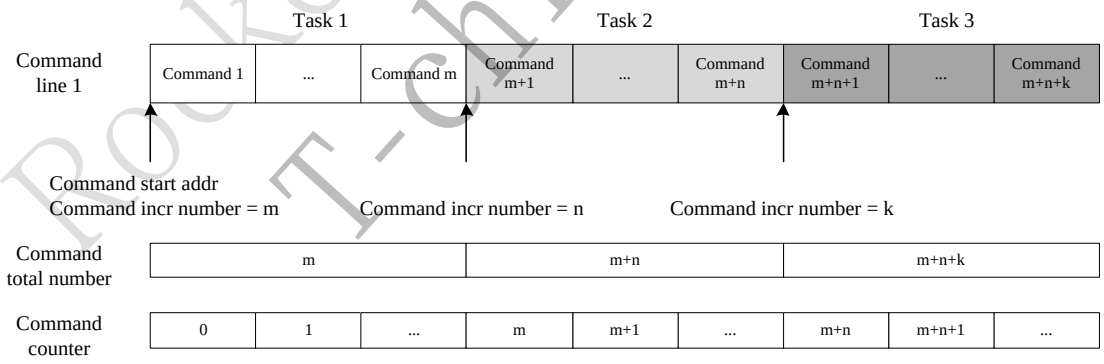


Fig. 28-7 RGA command line and command counter

28.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the current_cmd_int command by command to

generate a interrupt at the end point of target command operation.

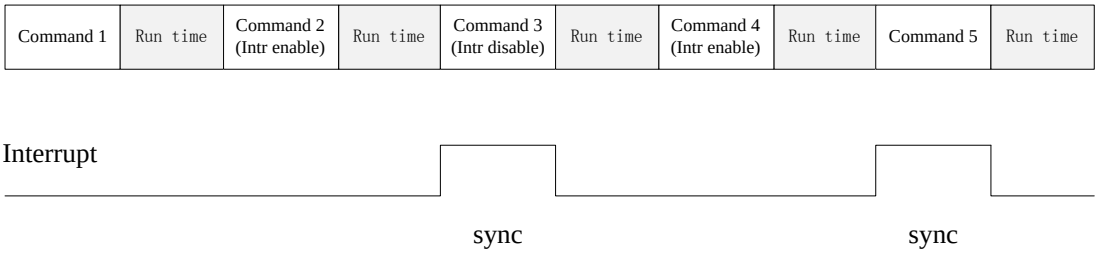


Fig. 28-8 RGA command sync generation