Chapter 19 High-Speed ADC Interface (HS-ADC)

19.1 Overview

HS-ADC Interface Unit is an interface unit for connecting the TS interface and GPS ADC interface to AMBA AHB bus. It fetches the bus data received by the TS interface and GPS ADC interface and stores them to internal asynchronous FIFO after the ADC clock is active. The HS-ADC Interface Unit generates the DMA request signal when data length of the asynchronous FIFO over the almost full level or almost empty level.
HS-ADC supports the following features:

Support Transport-Stream(TS) Interface with 8bits data bus
Support GPS interface with 2bits or 4bits data bus
Support combined interrupt output, source including: full interrupt, empty interrupt
Support DMA transfer mode through generating DMA request from the event of almost full or almost empty, etc.
Support two channel mode: single channel and dual channel
Support the most significant bit negation or not
Support sign bit extension
Support two storage mode: input data are stored to high 8bit or 10bit and stored to low 8bit or 10bit of 16bit when pushed into FIFO.
Support an asynchronous build-in FIFO with 128x64 size

19.2 Block Diagram

The HS-ADC diagram is as follows.

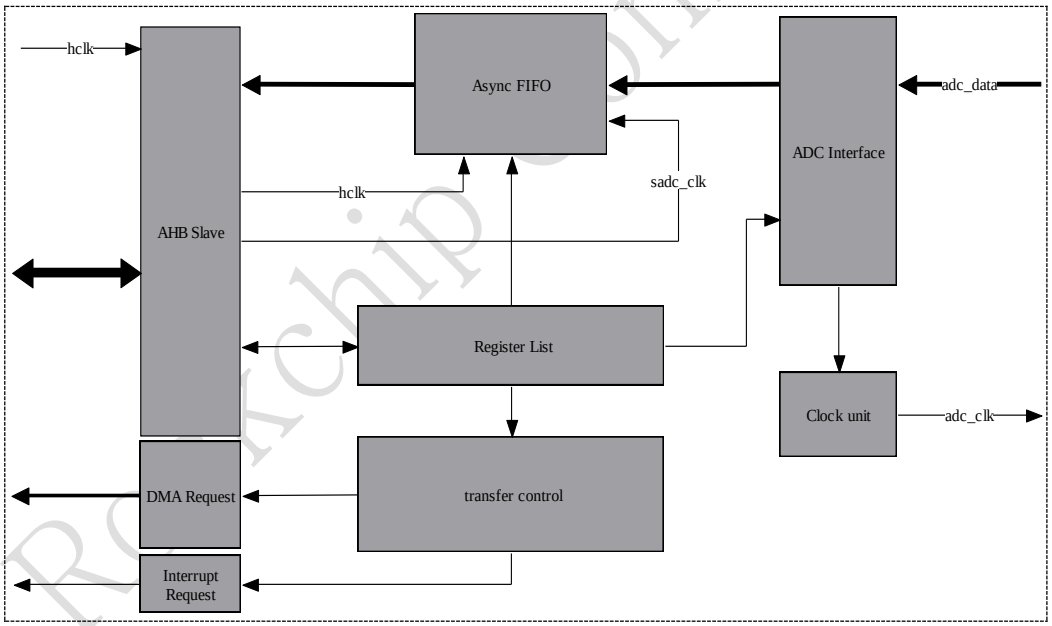

Fig. 19-1 HS-ADC Architecture

19.3 Function Description

This module can be configured for two interfaces: GPS interface, TS interface.

19.3.1 GPS interface

When this module is used as GPS interface, user should configure GRF register to select 2bits or 4bitsGPS data input and gps_clk as GPS clock input from pad.
Also, user should configure CRU_CLKSEL22_CON[5:4] to select gps_clk as HS-ADC controller working clock source.

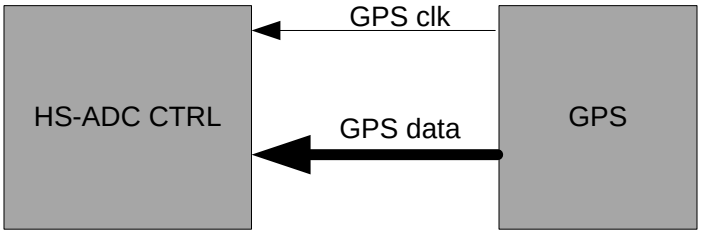

Fig. 19-2 GPS Application Diagram

19.3.2 TS interface

When this module is used as TS interface, user should configure GRF register to select 8bit TS data, ts_sync, ts_valid and ts_fail input and gps_clk input as TS clock input from pad.
Also, user should configure CRU_CLKSEL22_CON[5:4] to select gps_clk from pad as TS clock input.

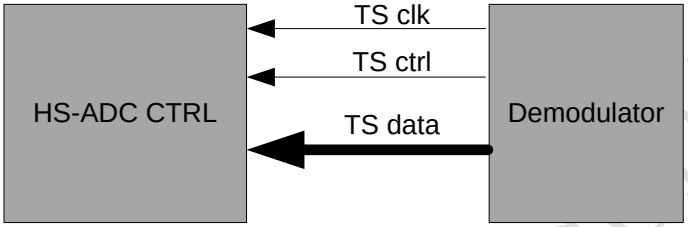

Fig. 19-3 TS Application Diagram

19.4 Register Description

19.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
HSADC_CTRL	0x0000	W	0x00000000	Control register
HSADC_IER	0x0004	W	0x00000000	Interrupt control register
HSADC_ISR	0x0008	W	0x00000000	Interrupt status register
HSADC_TS_FAIL	0x000c	W	0x00000000	ts fail register
HSADC_CGCTL	0x0010	W	0x00000000	HSADC clock gating control
HSADC_DATA	0x0020	W	0x00000000	The data register of hsadc controller

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

19.4.2 Detail Register Description

HSADC_CTRL
Address: Operational Base + offset (0x0000)
Control register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	almost_full_level Define almost full trigger level 0x0~"0xf" - configure valid range (Notes: 1 level indicate 4 entries data in the async FIFO. and this configure range mapping to 64 - 124 entries data in the async FIFO.)
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	almost_empty_level Define almost empty trigger level 0x0~"0xf" - configure valid range (Notes: 1 level indicate 4 entries data in the async FIFO. and this configure range mapping to 0 - 60 entries data in the async FIFO.)
15	RW	0x0	gps_auto_gate_en GPS interface auto clock gating enable 1'b1: auto clock gating 1'b0: not auto clock gating
14	RW	0x0	ts_auto_gate_en TS interface auto clock gating enable 1'b1: auto clock gating 1'b0: not auto clock gating
13:12	RO	0x0	reserved
11	RW	0x0	gpsw GPS interface data width select 1'b0: 2bit data mode 1'b1: 4bit data mode
10	RW	0x0	ts_sync_en TS sync interface enable Field0000 Description
9	RW	0x0	ts_valid_en TS valid interface enable Enable ts interface "ts_valid" signal as data valid indicator 1'b0: disable 1'b1: enable
8	RW	0x0	ts_gps_sel MPEG-TS and GPS input select 1'b0: GPS is selected 1'b1: MPEG-TS is selected
7:6	RO	0x0	reserved
5	RW	0x0	dma_req_mode DMA request mode select 1'b1: almost full generate DMA request signal (Notes: this mode generate DMA request signal from almost full condition and cancel DMA request signal from almost empty condition. so you need configure two level by almost full level and almost empty level) 1'b0: almost empty generate DMA request signal (Notes: this mode generate DMA request signal from almost empty condition and that only once DMA request.)

Bit	Attr	Reset Value	Description
4:1	RO	0x0	reserved
0	RW	0x0	adc_en HS-ADC Interface Unit Enable Bit 1'b1: enable (Notes: will return 1 when the hardware started transfer) 1'b0: disable (Notes: other bit can be modify only the hardware return 0)

HSADC_IER
Address: Operational Base + offset (0x0004)
Interrupt control register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	int_empty_en Interrupt en/disable bit for the empty interrupt flag of async FIFO 1'b1: enable 1'b0: disable
0	RW	0x0	int_full_en Interrupt en/disable bit for the full interrupt flag of async FIFO 1'b1: enable 1'b0: disable

HSADC_ISR
Address: Operational Base + offset (0x0008)
Interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	int_empty_stat_ind Async FIFO empty interrupt flag 1'b1(R): This bit will be set to "1" when Async FIFO empty status and that only to read operation. 1'b0(W): Write "0" to bit for clear the interrupt flag and that only to wrtie operation.
0	RW	0x0	int_full_stat_ind Async FIFO full interrupt flag 1'b1(R): This bit will be set to "1" when Async FIFO full status and that only to read operation. 1'b0(W): Write "0" to bit for clear the interrupt flag and that only to wrtie operation.

HSADC_TS_FAIL
Address: Operational Base + offset (0x000c)
ts fail register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	ts_fail_ahb TS stream fail indicator this signal only valid when select TS stream input(mpts=1) 1'b0: TS stream decode successfully 1'b1: TS stream decode fail

HSADC_CGCTL
Address: Operational Base + offset (0x0010)
HSADC Clock Gating control

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	cycle_cfg clock gated cycles configuration when configure cg_enable to 1 and cycle_cfg to non-zero value,HSADC clock will be gated for cycle_cfg cycles ,then clock recover.
0	RW	0x0	cg_enable clock gating enable control 1'b0: clock gating disable 1'b1: clock gating enable

HSADC_DATA
Address: Operational Base + offset (0x0020)
Data register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DATA

19.5 Interface Description

19.5.1 TS mode

Table 19-1 IOMUX configuration in TS mode

Module Pin	IO	Pad Name	IOMUX Setting
hsadc_data0	I	IO_CIFdata2_HOSTdin0_HSADCdata0_DVPgpio2a0	GPIO2A_IOMUX[1:0]= 2'b11
hsadc_data1	I	IO_CIFdata3_HOSTdin1_HSADCdata1_DVPgpio2a1	GPIO2A_IOMUX[3:2]= 2'b11
hsadc_data2	I	IO_CIFdata4_HOSTdin2_HSADCdata2_DVPgpio2a2	GPIO2A_IOMUX[5:4]= 2'b11

Module Pin	IO	Pad Name	IOMUX Setting
hsadc_data3	I	IO_CIFdata5_HOSTdin3_HSADCdata3_DVPgpio2a3	GPIO2A_IOMUX[7:6]= 2'b11
hsadc_data4	I	IO_CIFdata6_HOSTckinp_HSADCdata4_DVPgpio2a4	GPIO2A_IOMUX[9:8]= 2'b11
hsadc_data5	I	IO_CIFdata7_HOSTckinn_HSADCdata5_DVPgpio2a5	GPIO2A_IOMUX[11:10]= 2'b11
hsadc_data6	I	IO_CIFdata8_HOSTdin4_HSADCdata6_DVPgpio2a6	GPIO2A_IOMUX[13:12]= 2'b11
hsadc_data7	I	IO_CIFdata9_HOSTdin5_HSADCdata7_DVPgpio2a7	GPIO2A_IOMUX[15:14]= 2'b11
hsadc_valid	I	IO_CIFhref_HOSTdin7_HSADCTSvalid_DVPgpio2b1	GPIO2B_IOMUX[3:2]= 2'b11
hsadc_sync	I	IO_CIFvsync_HOSTdin6_HSADCTSsync_DVPgpio2b0	GPIO2B_IOMUX[1:0]= 2'b11
hsadc_err	I	IO_CIFclkout_HOSTwkreq_HSADCTSfail_DVPgpio2b3	GPIO2B_IOMUX[7:6]= 2'b01
gps_clk	I	IO_CIFclkin_HOSTwkack_GPSclk_HSADCclkout_DVPgpio2b2	GPIO2B_IOMUX[5:4]= 2'b11
gpst1_clk	I	IO_UART3GPSctsn_GPSrfclk_GPST1clk_GPIO30gpio7b1	GPIO7B_IOMUX[3:2]= 2'b11

19.5.2 GPS mode

Table 19-2 IOMUX configuration in GPS mode

Module Pin	IO	Pad Name	IOMUX Setting
gps_clk	I	IO_CIFclkin_HOSTwkack_GPSclk_HSADCclkout_DVPgpio2b2	GPIO2B_IOMUX[5:4]= 2'b11
gpst1_clk	I	IO_UART3GPSctsn_GPSrfclk_GPST1clk_GPIO30gpio7b1	GPIO7B_IOMUX[3:2]= 2'b11
hsadc_data0	I	IO_CIFdata2_HOSTdin0_HSADCdata0_DVPgpio2a0	GPIO2A_IOMUX[1:0]= 2'b11
hsadc_data1	I	IO_CIFdata3_HOSTdin1_HSADCdata1_DVPgpio2a1	GPIO2A_IOMUX[3:2]= 2'b11
hsadc_data2	I	IO_CIFdata4_HOSTdin2_HSADCdata2_DVPgpio2a2	GPIO2A_IOMUX[5:4]= 2'b11
hsadc_data3	I	IO_CIFdata5_HOSTdin3_HSADCdata3_DVPgpio2a3	GPIO2A_IOMUX[7:6]= 2'b11

19.6 Application Notes

The following sections will describe the operation of DMA requests and DMA transfers.

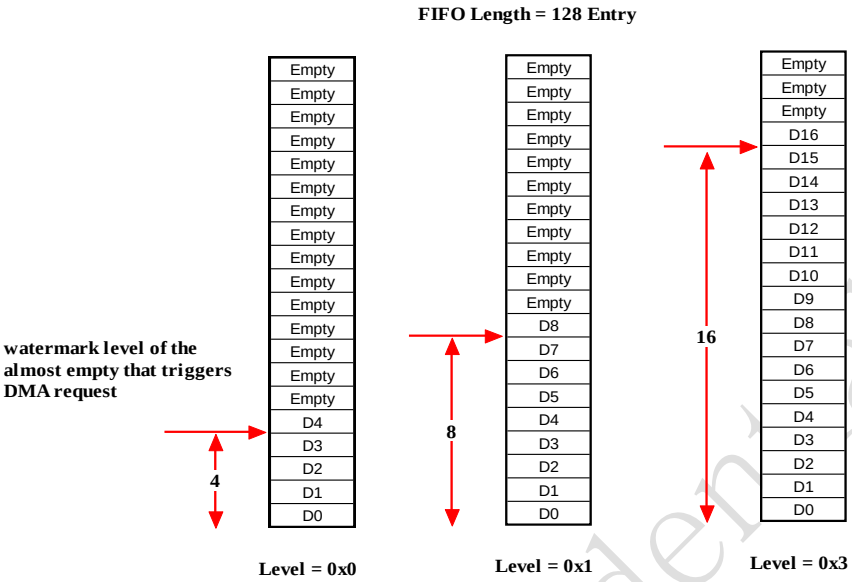

Fig. 19-4 Almost empty triggers a DMA request by DMA request mode

The DMA request signal will be generated from a watermark level trigger when data stored to FIFO over the watermark level of almost empty, where the watermark level can be configured through HSADC_CTRL[19:16] by software. This DMA request mode doesn't care the watermark level of almost full. The sample for watermark level configuration is shown in figure above.

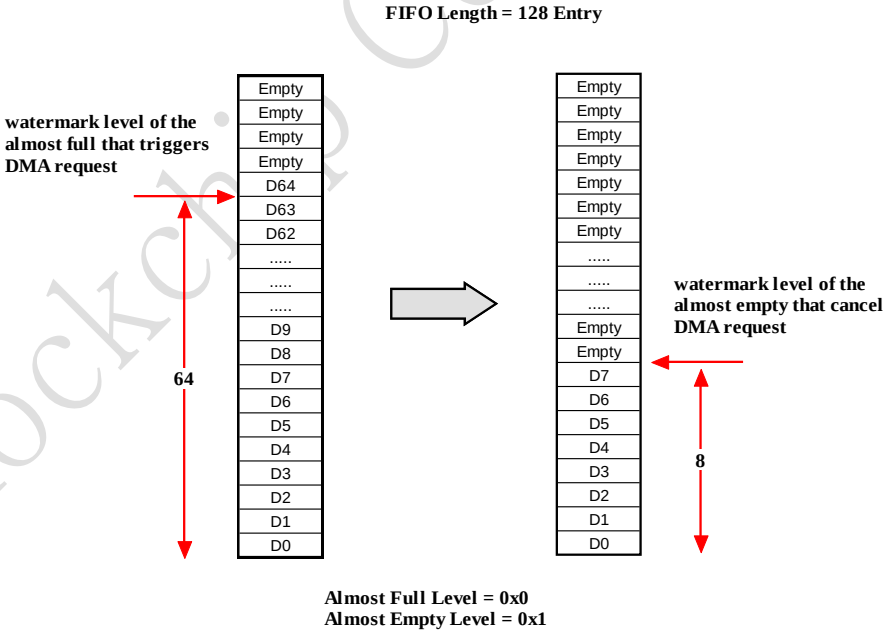

Fig. 19-5 Almost full triggers a DMA request by DMA request mode

The DMA request signal will be generated from a watermark level trigger when data stored to FIFO over the watermark level of almost full. It continues to generate request signal when the number of data in FIFO greater than watermark level of almost empty. This DMA request mode needs configure two watermark levels: watermark level of almost empty at the HSADC_CTRL[19:16] and watermark level of almost full at the HSADC_CTRL[27:24]. The sample for watermark level configuration is shown in figure above. When controller works in TS mode, the interface signal ts_sync should always be used.