Chapter 12 Generic Interrupt Controller (GIC)

12.1 Overview

The generic interrupt controller (GIC400) in this device has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A17.

It supports the following features:

- Supports 160 hardware interrupt inputs
- Masking of any interrupts
- Prioritization of interrupts
- Distribution of the interrupts to the target Cortex-A17 processor(s)
- Generation of interrupts by software
- Supports Security Extensions

12.2 Block Diagram

The generic interrupt controller comprises with:

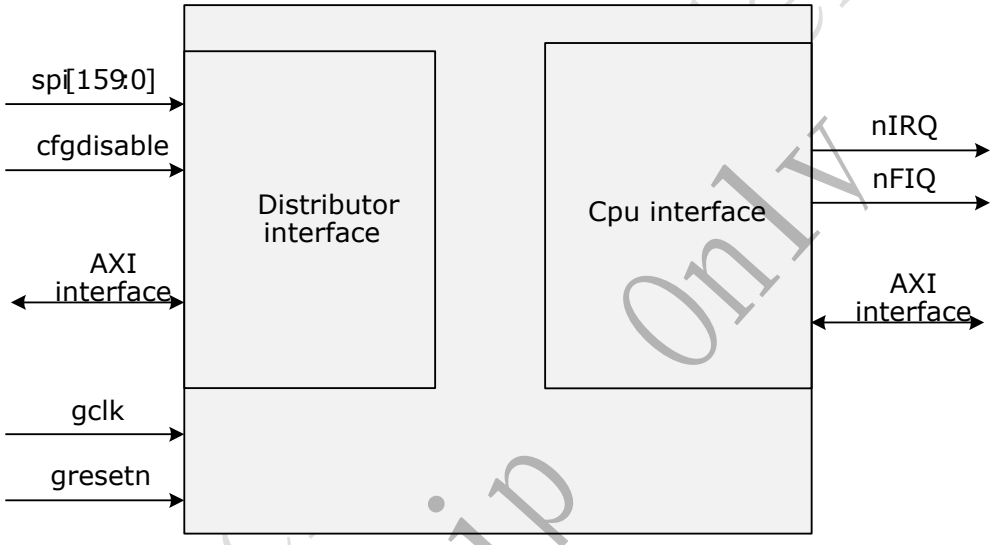

Fig. 12-1 Block Diagram

12.3 Function Description

Please refer to the document IHI0048B_gic_architecture_specification.pdf for the cpu detail description.