Chapter 1 Introduction

RK3288 is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A17 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3288 supports almost full-format H.264 decoder by 2160p@24fps, H.265 decoder by 2160p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3288 completely compatible with OpenGL ES1.1/2.0/3.0, OpenCL 1.1 and DirectX 11. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3288 has high-performance dual channel external memory interface(DDR3/DDR3L /LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications..

1.1 Features

1.1.1 MicroProcessor

- Quad-core ARM Cortex-A17 MPCore processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFP v3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the four CPUs
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 1MB unified L2 Cache
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Six separate power domains for every core to support internal power switch and externally turn on/off based on different application scenario
  - PD_A17_0: 1st Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_1: 2nd Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_2: 3rd Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_A17_3: 4th Cortex-A17 + Neon + FPU + L1 I/D Cache
  - PD_SCU: SCU + L2 Cache controller, and including PD_A17_0, PD_A17_1, PD_A17_2, PD_A17_3, debug logic
- One isolated voltage domain to support DVFS
- Maximum frequency can be up to 1GHz@1.0V

1.1.2 Memory Organization

- Internal on-chip memory
  - 20KB BootRom
  - 100KB internal SRAM for security and non-security access, detailed size is programmable

- External off-chip memory①
  - Dual channel DDR3-1066/DDR3L-1066, each channel 16/32bits data widths, 2 ranks, totally 4GB(max) address space, maximum address space for one rank of channel 0 is also 4GB.
  - Dual channel LPDDR2-1066, each channel 32bits data width, 2 ranks, totally 8GB(max) address space, maximum address space for one rank of channel 0 is also 4GB.
  - Dual channel LPDDR3-1066, each channel 32bits data width, 2 ranks, totally 8GB(max) address space, maximum address space for one rank of channel 0 is also 4GB.
  - Dual channel async Nand Flash(include LBA Nand), 8bits data width, 4 banks, 60bits ECC
  - Single channel async Nand Flash(include LBA Nand), 16bits data width, 4 banks, 60bits ECC
  - Dual channel sync ONFI/toggle Nand Flash , 8bits data width, 4 banks, 60bits ECC

1.1.3 Internal Memory

- Internal BootRom
  - Size : 20KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - 8bits toggle Nand Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 100KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB, … up to 96KB by 4KB step

1.1.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR2/LPDDR3)
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
  - Data rates up to 1333Mbps(66777MHz) for DDR3/DDR3L
  - Data rates up to 1066Mbps(533MHz) for LPDDR2/LPDDR3
  - Support 2 channel, each channel 16 or 32bits data widths
  - Support up to 2 ranks (chip selects) for each channel, totally 8GB(max) address space, maximum address space for one rank of channel 0 is also 4GB, which is software-configurable.
  - 16bits/32bits data width is software programmable
  - 7 host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2/LPDDR3 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals , make SDRAM still in self-refresh state to prevent data missing.

- Nand Flash Interface
  - Support dual channel async nand flash, each channel 8bits, up to 4 banks
  - Support dual channel sync DDR nand flash, each channel 8bits, up to 4 banks
  - Support LBA nand flash in async or sync mode
  - Up to 60bits hardware ECC
  - For DDR nand flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
  - For async nand flash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded special DMA interface to do data transfer
  - Also support data transfer together with general PERI_DMAC in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.5 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3288
  - One oscillator with 24MHz clock input and 5 embedded PLLs
  - Up to 2.2GHz clock output for all PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 4 separate voltage domains
  - 12 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 8 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility

- Support capture mode
- Support continuous mode or one-shot mode
- Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with four 64-bits AXI masters, one 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with three 128-bits AXI master, four 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master with point-to-point AXI-lite architecture and 32-bits APB slave
    - VCODEC interconnect also with two 64-bits AXI master and two 32-bits AHB slave, they are point-to-point AXI-lite architecture
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 112 SPI interrupt sources input from different components inside RK3288
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separatelyfor each Cortex-A17, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , BUS_DMAC is for bus system, PERI_DMAC is for peripheral system
  - BUS_DMAC features:
    - 6 channels totally

- 6 hardware request from peripherals
- 2 interrupt output
- Dual APB slave interface for register config, designated as secure and non-secure
- Support trustzone technology and programmable secure state for each DMA channel

- PERI_DMAC features:
  - 7 channels totally
  - 9 hardware request from peripherals
  - 2 interrupt output
  - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK3288
    - Cortex-A17, support security and non-security mode, switch by software
    - BUS_DMAC, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A17 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)
  - Embedded encryption and decryption engine
    - Support AES-128/192/256 with ECB, CBC, OFB, CTR, CBC-MAC, CMAC, XCBC-MAC, XTS and CCM modes
    - Supports the DES (ECB and CBC modes) and TDES (EDE and DED) algorithms
    - Supports SHA-1, SHA-256 and SHA-512 modes, as well as HMAC
    - Support all mathematical operations required to implement the PKA supported cryptosystems between 128 bits and 3136 bits in size (in steps of 32 bits)
    - Support random bits generator from the ring oscillator
    - Control the AIB interface to the OTP memory and providing an interface for the CPU to access to the non-confidential trusted data
    - Set the device's security lifecycle state according to the values of various flag words in the OTP memory
    - Provide an firmware interface for secure boot, secure debug
    - Provide a security processor sub-system based on an internal 32-bit CPU
  - Support security boot
  - Support security debug

1.1.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, AVS, VC-1, RV, VP6/VP8, Sorenson Spark, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 5.2 : 2160p@24fps (3840x2160)③
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 2160p@24fps (3840x2160)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - Sorenson Spark : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - RV8/RV9/RV10 : 1080p@60fps (1920x1088)
  - VP6/VP8 : 2160p@24fps (3840x2160)
  - AVS : 1080p@60fps (1920x1088)
  - MVC : 2160p@24fps (3840x2160)

- For AVS, 4:4:4 sampling not supported
- For H.264, image cropping not supported
- For MPEG-4, GMC(global motion compensation) not supported
- For VC-1, upscaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080[③]
  - Bit rate supported is from 10Kbps to 20Mbps

1.1.7 HEVC Decoder

- Main/Main10 HEVC/H.265 decoderof 4k@60FPS
- Support up to 4096x2304 resolution
- Support up to 100Mbps bit rate
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.1.8 JPEG CODEC

- JPEG decoder
  - Input JPEG file：YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image：YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[④] is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image：
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file：JFIF file format 1.02 or Non-progressive JPEG

- Encoder image size up to 8192x8192(64million pixels) from 96x32
- Maximum data rate④ up to 90million pixels per second
- Embedded memory management unit(MMU)

1.1.9 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside RK3288, not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization
  - Work in combined mode with HD video encoder inside RK3288 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image Post-Processor (embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory
  - Input data format:
    - Any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Output data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
  - Input image size:
    - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
    - Stand-alone mode: width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
    - Step size is 16 pixels
  - Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
  - Support image up-scaling:
    - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Maximum output width is 3x input width
    - Maximum output height is 3x input height
  - Support image down-scaling:
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Unlimited down-scaling ratio

- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha + YUV444, big endian channel order with AYUV8888
  - 8bit alpha + 24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Enhancement-Processor (IEP)
  - Image format
    - Input data: XRGB/RGB565/YUV420/YUV422
    - Output data: ARGB/RGB565/YUV420/YUV422
    - The format ARGB/XRGB/RGB565/YUV support swap
    - Support YUV semi-planar/planar
    - Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
    - Support RGB dither up/down conversion
    - Support YUV up/down sampling conversion
    - Max source image resolution: 8192x8192
    - Max scaled image resolution: 4096x4096
  - Enhancement
    - Gamma adjustment with programmable mapping table
    - Hue/Saturation/Brightness/Contrast enhancement
    - Color enhancement with programmable coefficient
    - Detail enhancement with filter matrix up to 9x9
    - Edge enhancement with filter matrix up to 9x9
    - Programmable difference table for detail enhancement
    - Programmable distance table for detail and edge enhancement
  - Noise reduction
    - Compression noise reduction with filter matrix up to 9x9
    - Programmable difference table for compression noise reduction
    - Programmable distance table for compression noise reduction
    - Spatial sampling noise reduction
    - Temporal sampling noise reduction
    - Optional coefficient for sampling noise reduction
  - Scaling
    - Horizontal down-scaling with vertical down-scaling
    - Horizontal down-scaling with vertical up-scaling
    - Horizontal up-scaling with vertical down-scaling
    - Horizontal up-scaling with vertical up-scaling
    - Arbitrary non-integer scaling ratio, from 1/16 to 16
  - Deinterlace
    - Input 4 fields, output 2 frames mode
    - Input 4 fields, output 1 frames mode
    - Input 2 fields, output 1 frames mode
    - Programmable motion detection coefficient
    - Programmable high frequency factor
    - Programmable edge interpolation parameter
    - Source width up to 1920
  - Interface
    - Programmable direct path to VOP

- Embedded memory management unit(MMU)

1.1.10 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1/2.0/3.0, OpenCL 1.1, DirectX 11 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 256KB size
  - Image quality using double-precision FP64, and anti-aliasing

- 2D Graphics Engine :
  - BitBlit with Stretch Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4
  - Alpha blending modes including global alpha, per pixel alpha, porter-duff and fading
  - 8K x 8K input and 2K x 2K output raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Blending, scaling and rotation are supported in one pass for Bitbilt
  - Source format:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
    - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.1.11 Video IN/OUT

- Camera Interface(interface only)
  - Support up to 5M pixels
  - 8bits BT656(PAL/NTSC) interface
  - 16bits BT601 DDR interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Camera Interface and Image Processer(Interface and Image Processing)
  - Maximum input resolution of 14M(4416x3312) pixels
  - Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
  - Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
  - support of semiplanar NV21 color storage format

- support of independent image cropping on main and self path
- ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
- 12 bit camera interface
- 12 bit resolution per color component internally
- YCbCr 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable
- quantization and Huffman tables
- Windowing and frame synchronization
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Continuous resize support
- Color processing (contrast, saturation, brightness, hue, offset, range)
- Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
- Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
- Read port provided to read back a picture from system memory
- Simultaneous picture read back, resizing and storing through self path while main
- path captures the camera picture
- Black level compensation
- Four channel Lens shade correction (Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction

- Display Interface
  - Embedded two channel display interfaces: VOP_BIG and VOP_LIT.
  - Parallel Display interface
    - Parallel RGB LCD Interface:
      - 30-bit(RGB101010),24-bit(RGB888),18-bit(RGB666), 15-bit(RGB565)
    - Serial RGB LCD Interface(optional):
      - 2x12-bit, 3x8-bit(RGB delta support), 3x8-bit+dummy
    - MCU LCD interface(optional):
      - i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
    - TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i)
    - DDR output interface:
      - parallel RGB and 2x12-bit serial RGB
      - Single or dual clock out
    - dither down:
      - allegro, FRC
      - gamma after dither
    - Max output resolution: 3840x2160 (for VOP_BIG), 2560x1600 (for VOP_LIT)
    - Scaning timing 8192x4096
  - Display process

- Background layer:
  - programmable 24-bit color
- Win0 (Video0) layer:
  - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
  - Support virtual display
  - 1/8 to 8 scaling-down and scaling-up engine:
    - Scale up using bicubic or bilinear;
    - Scale down using bilinear or average;
    - 4 Bicubic tables : precise,spline,catrom,mitchell;
    - coord 8bit, coe 8bit signed
  - x-mirror,y-mirror
- Win1 (Video1) layer:
  - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
  - Support virtual display
  - 1/8 to 8 scaling-down and scaling-up engine
    - Scale up using bicubic or bilinear;
    - Scale down using bilinear otraverage;
    - 4 Bicubic tables : precise,spline,catrom,mitchell;
    - coord 8bit, coe 8bit signed
  - x-mirror,y-mirror
- Win2 (UI 0) layer:
  - RGB888, ARGB888, RGB565, 1/2/4/8bpp
  - Support virtual display
  - 4 display regions
  - x-mirror,y-mirror
- Win3 (UI 1) layer:
  - RGB888, ARGB888, RGB565, 1/2/4/8bpp
  - Support virtual display
  - 4 display regions
  - x-mirror,y-mirror
- Hardware cursor:
  - RGB888, ARGB888, RGB565, 1/2/4/8bpp
  - Support two size: 32x32,64x64,or 128x128
- Overlay:
  - Win0/Win1/Win2/Win3 256 level alpha blending (support pre-multiplied alpha)
  - Win0/Win1/Win2/Win3 overlay position exchangeable
  - Win0/Win1/Win2/Win3 Transparency color key
  - Win0/Win1/Win2/Win3 global/per-pixel alpha
  - HWC 256 level alpha blending
  - HWC global/per-pixel alpha

- Others
  - 3 x 256 x 8 bits display LUTs
  - YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709/BT2020)and RGB2YcbCr
  - Support BCSH function
  - Support CABC function
  - QoS request signals
  - Gather transfer (Max 8)
  - Y/UV scheduler
  - Addr alignment
  - Support IEP direct path(win0/1/2/3)
  - Embedded memory management unit(MMU)
  - Support MIPI flow control

1.1.12 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:

  - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
  - Up to 10-bit Deep Color modes
  - Up to 18 Gbps aggregate bandwidth
  - 13.5–600 MHz input reference clock
  - HPD input analog comparator
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- Support HDCP 1.4

1.1.13 LVDS

- Comply with the TIA/EIA-644-A LVDS standard
- Combine LVTTL IO, support LVDS/LVTTL data output
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 30/24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, every channel include 5 data lanes and 1 clock lane

1.1.14 MIPI PHY

- Embedded 3 MIPI PHY, MIPI 0 only for TX, MIPI 1 for TX and RX, MIPI 2 only for RX
- Support 4 data lane, providing up to 6Gbps data rate
- Support 1080p @ 60fps output
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction

1.1.15 eDP PHY

- Support 4Kx2K @ 30fps
- Compliant with eDP TM Specification, version 1.1
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane(HBR2/HBR/RBR)
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format
- Encoded bit stream (Dolby Digital, or DTS) – IEC61937 compliant
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861D video timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Support DDC/CI and MCCS command transmission when the monitor includes a display controller.
- Supports Panel Self Refresh(PSR)

1.1.16 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

1.1.17 Connectivity

- SDIO interface
  - Embedded 2 SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface

- TS interface
  - Supports two TS input channels and one TS output channel.
  - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
  - Supports serial and parallel output mode with PCR adjustment, and lsb-msb or msb-lsb bit ordering can be chosen in the serial output mode.
  - Supports 2 TS sources: demodulators and local memory.
  - Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
    - 64 PID filters.
    - TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps
    - 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
    - 4/8 PCR extraction channels
    - 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
    - PID done and error interrupts for each channel
    - PCR/DTS/PTS extraction interrupt for each channel
  - Supports 1 PVR(Personal Video Recording) output channel.
  - 1 built-in multi-channel DMA Controller.

- PS2 interface
  - Support PS/2 data communication protocol
  - Support PS/2 master mode
  - Software programmable timing requirement to support max PS/2 clock frequency to 33KHZ
  - Support status to be queried for data communication error
  - Support interrupt mode for data communication finish
  - Support timeout mechnism for data communication
  - Support interrupt mode for data communication timeout

- Smart Card
  - support card activation and deactivation
  - support cold/warm reset
  - support Answer to Reset (ATR) response reception
  - support T0 for asynchronous half-duplex character transmission
  - support T1 for asynchronous half-duplex block transmission
  - support automatic operating voltage class selection
  - support adjustable clock rate and bit (baud) rate
  - support configurable automatic byte repetition

- Host interface
  - Low Pin Count interface(8 inputs/16 outputs or 16 inputs/8 outputs)
  - No mandatory Tri-State signals
  - All signals driven using source synchrounous clock.(2 DDR clock signals per direction for TX and RX paths)

- Low latency throught serialization/deserialization
- Transport clocks and bus clock are independent
- Support Asymmetric(Host/Peripheral) communication operations
- Support multiple outstanding transactions Reads,Writes and interrupts
- Support Mirror Mode to enable self tett with identical device

- GPS Interface
  - Single chip, integrate GPS bb with cpu
  - 32 DMA channels for AHB master access
  - Complete 1-band, C/A, and NMEA-0183 compatibility
  - Support reference frequencies 16.368MHz
  - High sensitivity for indoor fixes
  - Low power consumption
  - Low cost with smaller size
  - Multi modes support both standalone GPS and A_GPS

- GMAC 10/100/1000M Ethernet Controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
    - Optional forwarding of received pause control frames to the user application in full-duplex operation
    - Back-pressure support for half-duplex operation
    - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable Inter Frame Gap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
  - Comprehensive status reporting for normal operation and transfers with errors
  - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
  - Handles automatic retransmission of Collision frames for transmission
  - Discards frames on late collision, excessive collisions, excessive deferral and under run conditions

- SPI Controller
  - 3 on-chip SPI controller inside RK3288
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller

- 5 on-chip uart controller inside RK3288
- DMA-based or interrupt-based operation
- For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
- Support 5bit,6bit,7bit,8bit serial data transmit or receive
- Standard asynchronous communication bits such as start,stop and parity
- Support different input clock for uart operation to get up to 4Mbps or other special baud rate
- Support non-integer clock divides for baud clock generation
- Auto flow control mode is for all UART, except UART_DBG

- I2C controller
  - 6 on-chip I2C controller in RK3288
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - Totally 160 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A17
  - GPIO0 can be used to wakeup system from low-power mode
  - The pull direction(pullup or pulldown) for all of GPIOs are software-programmable
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength for all of GPIOs is software-programmable

- USB Host2.0
  - Embedded 2 USB Host2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

- HSIC Interface
  - Compliant with the USB2.0 Specification and Enhanced Host Controller Interface Specification 2.0
  - 1 Port HSIC PHY Interface Operates in host mode
  - Built-in one 512x64 bits FIFO
  - Internal DMA with scatter/gather function

1.1.18 Others

- Temperature Sensor(TS-ADC)
  - 3 bipolar-based temperature-sensing cell embedded
  - 3-channel 12-bits SAR ADC
  - Temperature accuracy sensed is ±5 degree
  - SAR-ADC clock must be less than 50KHz

- Power Down Current is about 1uA for anolog and 2uA for digital logic

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter
  - Conversion speed range is up to 1 MSPS
  - SAR-ADC clock must be less than 1MHz
  - DNL is less than ±1 LSB , INL is less than ±2.0 LSB
  - Power down current is about 0.5uA for analog and digital logic
  - Power supply is 1.8V (±10%) for analog interface

- eFuse
  - Two high-density electrical Fuse is integrated: 256bits (32x8) / 1024bits (32x32)
  - Support standby mode

Notes :① DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddr nand flash
② In RK3288, Video decoder and encoder are not used simultaneously because of shared internal buffer
③ Actual maximum frame rate will depend on the clock frequency and system bus performance
④ Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK3288.

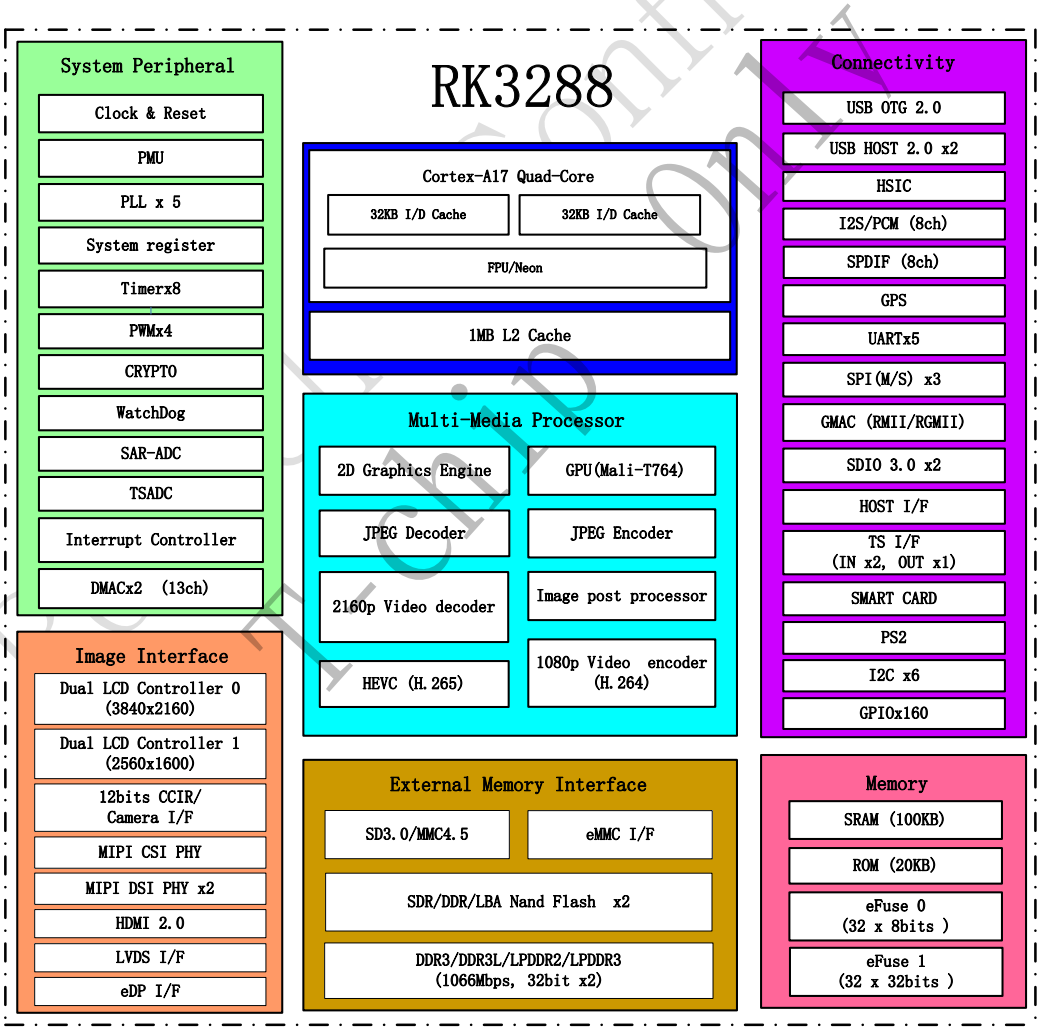

Fig. 1-1 RK3288 Block Diagram