Rockchip RK3188T Datasheet

Revision 1.1
JUN. 2014

Revision History

Date	Revision	Description
2013-12-05	1.0	first Release
2014-6-20	1.1	

Table of Content

Figure Index

Table Index

Warranty Disclaimer

Rockchip Electronics Co., Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co.,Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co., Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co., Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co., Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co., Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co., Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co.,Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co., Ltd does not convey any license under its patent rights nor the rights of others.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co., Ltd's products are trademarks of Rockchip Electronics Co., Ltd. and are exclusively owned by Rockchip Electronics Co., Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Chapter 1 Introduction

1.1 Overview

RK3188T is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A9 with separately NEON and FPU coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3188T supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3188T completely compatible with OpenGL ES2.0 and 1.1, OpenVG1.1. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3188T has high-performance external memory interface (DDR3/LPDDR2/LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

1.2.1 Processor

- Quad-core ARM Cortex-A9 MPCore processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the four CPUs
- Integrated timer and watchdog timer per CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 512KB unified L2 Cache
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Six separate power domains for every core to support internal power switch and externally turn on/off based on different application scenario
  - PD_A9_0: 1st Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_A9_1: 2nd Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_A9_2: 3rd Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_A9_3: 4th Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_DBG: CoreSight-DK for Cortex-A9
  - PD_SCU: SCU + L2 Cache controller + L2 Dataram, and including PD_A9_0, PD_A9_1, PD_A9_2, PD_A9_3, PD_DGB
- One isolated voltage domain to support DVFS
- Maximum frequency can be up to 1.1GHz@1.0V.

1.2.2 Memory Organization

- Internal on-chip memory
  - 10KB BootRom
  - 32KB internal SRAM for security and non-security access, detailed size is programmable

- External off-chip memory①
  - DDR3-900, 16/32bits data widths, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
  - LPDDR2-900, 32bits data width, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
  - Async SRAM/Nor Flash, 8/16bits data width,2banks
  - Async Nand Flash(include LBA Nand), 8/16bits data width, 4 banks, 60bits ECC
  - Sync ONFI Nand Flash , 8bits data width, 8 banks, 60bits ECC

1.2.3 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device:
    - 8bits/16bits Async Nand Flash
    - 8bits ONFI Nand Flash
    - SPI0 interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
    - UART2Interface
- Internal SRAM
  - Size : 32KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB,32KB continuous size

1.1.1 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LPDDR2)
  - Compatible with JEDEC standard DDR3/LPDDR2 SDRAM
  - Data rates up to 900Mbps(450MHz) for DDR3/LPDDR2
  - Support up to 2 ranks (chip selects), totally 2GB(max) address space, maximum address space for one rank is also 2GB, which is software-configurable.
  - 16bits/32bits data width is software programmable
  - 7 host ports with 64bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/LPDDR2 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2 SDRAM; clock stop and deep power-down forLPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and two cke output signals, make SDRAM still in self-refresh state to prevent data missing.

- Static Memory Interface (ASRAM/Nor Flash)
  - Compatible with standard async SRAM or Nor Flash
  - Support up to 2 banks (chip selects)
  - For bank0, 8bits/16bits data width is software programmable; For bank1, 16bits data width is fixed
  - Support separately data and address bus, also support shared data and address bus to save IO numbers

- Nand Flash Interface
  - Support 8bits/16bits async nand flash, up to 4 banks
  - Support 8bits sync DDR nand flash, up to 4 banks
  - Support LBA nand flash in async or sync mode
  - Up to 60bits hardware ECC
  - For DDR nand flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
  - For async nand flash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded special DMA interface to do data transfer
  - Also support data transfer together with general DMAC1 in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.2 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3188T
  - One oscillator with 24MHz clock input and 4 embedded PLLs
  - Up to 2.2GHz clock output for all PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - 6 work modes(slow mode, normal mode, idle mode, stop mode, sleep mode, power-off mode) to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 3 separate voltage domains
  - 10 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 7 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation

- Programmable 4-bit pre-scalar from apb bus clock
- Embedded 32-bit timer/counter facility
- Support single-run or continuous-run PWM mode
- Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 64-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with three 64-bits AXI masters, two 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, one 32-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with six 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master and 64-bits AXI slave ,they are point-to-point AXI-lite architecture
    - VCODEC interconnect also with one 64-bits AXI master and one 32-bits AHB slave ,they are point-to-point AXI-lite architecture
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 76 SPI interrupt sources input from different components inside RK3188T
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A9, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , DMAC0 is for cpu system, DMAC1 is for peri system
  - DMAC0 features:
    - 6 channels totally
    - 11 hardware request from peripherals
    - 2 interrupt output

- Dual APB slave interface for register configure, designated as secure and non-secure
- Support Trustzone technology and programmable secure state for each DMA channel

- DMAC1 features:
  - 7 channels totally
  - 13 hardware request from peripherals
  - 2 interrupt outputs
  - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK3188T
    - Cortex-A9, support security and non-security mode, switch by software
    - DMAC0, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A9 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)

1.1.3 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Video Decoder
- Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , AVS , VC-1 , RV , VP6/VP8 , Sorenson Spark, MVC
- Error detection and concealment support for all video formats
- Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
- H.264 up to HP level 4.2 : 1080p@60fps (1920x1088)®
- MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
- MPEG-2 up to MP : 1080p@60fps (1920x1088)
- MPEG-1 up to MP : 1080p@60fps (1920x1088)
- H.263 : 576p@60fps(720x576)
- Sorenson Spark : 1080p@60fps (1920x1088)
- VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
- RV8/RV9/RV10 : 1080p@60fps (1920x1088)
- VP6/VP8 : 1080p@60fps (1920x1088)
- AVS : 1080p@60fps (1920x1088)
- MVC : 1080p@60fps (1920x1088)
- For AVS, 4:4:4 sampling not supported
- For H.264, Image cropping not supported
- For MPEG-4,GMC(global motion compensation) not supported
- For VC-1, upscaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.1.4 Video Encoder

- Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
- Only support I and P slices, not B slices
- Support error resilience based on constrained intra prediction and slices
- Input data format :
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - CbYCrY 4:2:2 interleaved
  - RGB444 and BGR444
  - RGB555 and BGR555

- RGB565 and BGR565
- RGB888 and BRG888
- RGB101010 and BRG101010

- Image size is from 96x96 to 1920x1088(Full HD)
- Maximum frame rate is up to 30fps@1920x1080[8]
- Bit rate supported is from 10Kbps to 20Mbps

1.1.5 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Maximum data rate[4] is up to 76million pixels per second

  - JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[4] up to 90million pixels per second

1.1.6 Image Enhancement

- Image pre-processor
- Only used together with HD video encoder inside RK3188T, not support stand-alone mode
- Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
- Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
- Support cropping operation from 8192x8192 to any supported encoding size
- Support rotation with 90 or 270 degrees

- Video stabilization
  - Work in combined mode with HD video encoder inside RK3188T and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image Post-Processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - Any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2

- CbYCrY 4:2:2
- CrYCbY 4:2:2

- Ouput data format:
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - YCrYCb 4:2:2
  - CbYCrY 4:2:2
  - CrYCbY 4:2:2
  - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
- Input image size:
  - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling :
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering) for 4,5,6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha +YUV444, big-endian channel order with AYUV8888
  - 8bit alpha +24bit RGB, big-endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Post-Processor (IPP) (standalone)
  - memory to memory mode
  - input data format and size
    - RGB888 : 16x16 to 8191x8191
    - RGB565 : 16x16 to 8191x8191
    - YUV422/YUV420 : 16x16 to 8190x8190
    - YUV444 : 16x16 to 8190x8190
  - pre scaler
    - integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter
    - deinterlace(up to 1080i) to support YUV422&YUV420 input format
  - post scaler
    - down-scaling with 1/2 ~ 1 arbitary non-integer ratio
    - up-scaling with 1~4 arbitary non-integer ratio
    - 4-tap vertical, 2-tap horizontal filter
    - The max output image width of post scaler is 4096
  - Support rotation with 90/180/270 degrees and x-mirror,y-mirror

1.1.7 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Seperate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 128KB size

- 2D Graphics Engine :
  - BitBlit with Stretch Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2,ROP3,ROP4
  - Alpha blending modes including global alpha, per_pixel alpha, porter-duff and fading
  - 8K x 8K input and 2K x 2K output raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Blending, scaling and rotation are supported in one pass for Bitbilt
  - Source format:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
    - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.1.8 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits BT656(PAL/NTSC) interface
  - 16bits BT601 DDR interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Display Interface
  - Two independent display controllers
  - Support LCD or TFT interfaces up to 1366x800
  - Parallel RGB LCD Interface : RGB888(24bits),RGB666(18bits),RGB565(15bits)
  - Serial RGB LCD Interface: 3x8bits with RGB delta support, 3x8bits followed by dummy data, 16bits followed by 8bits
  - MCU LCD interface : i-8080 with up to 24bits RGB

- Support DDR output mode with differential clocks output
- Support DDR output mode with single clock output
- Four display layers :
  - One background layer with programmable 24bits color
  - One video layer (win0)
    - RGB888, ARGB888, RGB565, YUV422, YUV420
    - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
    - Support virtual display
    - 256 level alpha blending
    - Support transparency color key
    - Support 3D display
  - One video layer (win1)
    - RGB888, ARGB888, RGB565, 1/2/4/8BPP
    - Support virtual display
    - 256 level alpha blending
    - Support transparency color key
  - Hardware cursor(hwc)
    - 2BPP
    - Maximum resolution 64x64
    - 3-color and transparent mode
    - 2-color + transparency + tran_invert mode
    - 16 level alpha blending
- 3 x 256 x 8 bits display LUTs
- Win0 and Win1 layer overlay exchangeable
- Support color space conversion:
  YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
- Deflicker support for interlace output
- 24bits to 16bits/18bitsditheringoperation
- Blank and black display
- Standby mode

1.1.9 Audio Interface

- I2S/PCM with 2ch
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time
- SPDIF
  - Audio resolution: 16bits/20bits/24bits
  - Software configurable sample rates (48KHz, 44.1KHz, 32KHz)
  - Stereo voice replay with 2 channels

1.1.10 Connectivity

- SDIO interface
- Compatible with SDIO 3.0 protocol
- Support FIFO over-run and under-run prevention by stopping card clock Automatically
- 4bits data bus widths
-
- High-speed ADC stream interface
- Support single-channel 8bits/10bits interface
- DMA-based and interrupt-based operation
- Support 8bits TS stream interface
- Support PID filter operation
  - Combined with high-speed ADC interface to implement filter from original TS data

- Provide PID filter up to 64 channels PID simultaneously
- Support sync-byte detection in transport packet head
- Support packet lost mechanism in condition of limited bandwidth

- MAC 10/100MEthernet Controller
  - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
  - Support only RMII(Reduced MII) mode
  - 10Mbps and 100Mbps compatible
  - Automatic retry and automatic collision frame deletion
  - Full duplex support with flow-control
  - Address filtering(broadcast, multicast, logical, physical)

- GPS Interface
  - Single chip, integrate GPS bb with cpu.
  - 32 DMA channels for ahb master access
  - Complete l1-band, C/A, and NMEA-0183 compatibility.
  - Support reference frequencies 16.368MHz.
  - High sensitivity for indoor fixes.
  - Low power consumption.
  - Low cost with smaller size.
  - Multi modes support both standalone GPS and A_GPS

- SPI Controller
  - 2 on-chip SPI controller inside RK3188T
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller
  - 4 on-chip uart controller inside RK3188T
  - DMA-based or interrupt-based operation
  - For UART1/UART2/UART3, Embedded two 32Bytes FIFO for TX and RX operation respectively
  - For UART0, two 64Bytes FIFOs are embedded for TX/RX operation
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Auto flow control mode is only for UART0, UART1, UART3

- I2C controller
  - 5 on-chip I2C controller in RK3188T
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3,) , 32 GPIOs per group, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - GPIO0 can be used to wakeup system from stop/sleep/power-off mode
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not

- All of GPIOs are always in input direction in default after power-on-reset
- The drive strength for all of GPIOs is software-programmable

- USB Host2.0
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels
  - Provides UART support to receive and transmit asynchronous, serial data by reusing DP/DM ports

- HSIC Interface
  - Compliant with the USB2.0 Specification and Enhanced Host Controller Interface Specification 2.0
  - 1 Port HSIC PHY Interface Operates in host mode
  - Built-in one 840x35 bits FIFO
  - Internal DMA with scatter/gather function

1.1.11 Others

- SAR-ADC(Successive Approximation Register)
- 3-channel single-ended 10-bit SAR analog-to-digital converter
- Conversion speed range is up to 1 MSPS
- SAR-ADC clock must be less than 1MHz
- DNL is less than ±1 LSB , INL is less than ±2.0 LSB
- Power down current is about 0.5uA for analog and digital logic
- Power supply is 1.8V (±10%) for analog interface

- eFuse
- 256bits (32x8) high-density electrical Fuse
- Programming condition : VQPS must be 1.5(±10%)
- Program time is about 10us(±1us)
- Read condition : VQPS must be 0V
- Support standby mode

1.1.12 Package Type

- TFBGA453LD (body: 19mm x 19mm; ball size: 0.4mm; ball pitch: 0.8mm)

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3188T.

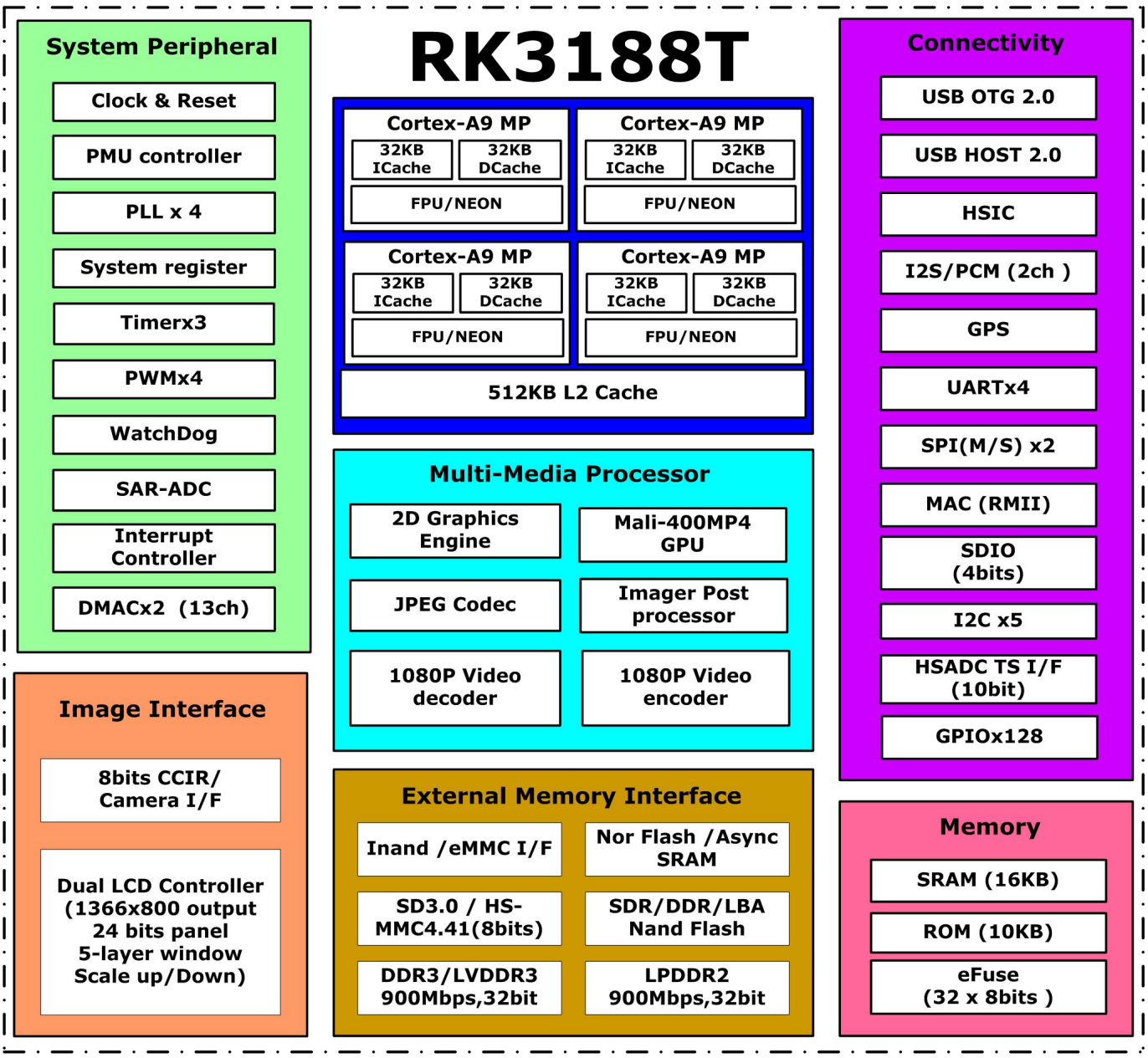


Fig. 1-1 RK3188T Block Diagram

Chapter 2 Package information

2.1 Dimension

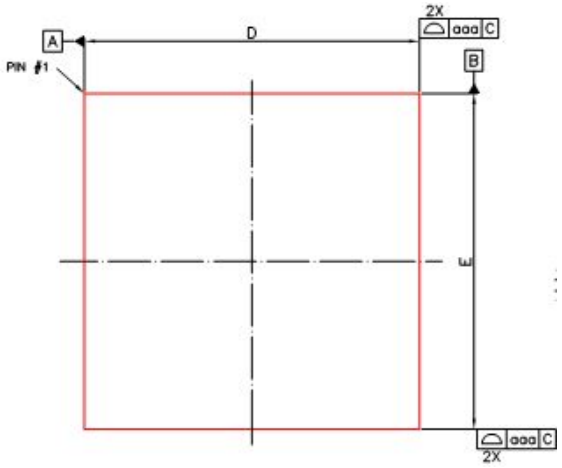


Fig. 2-1 RK3188T TFBGA453 Package Top View

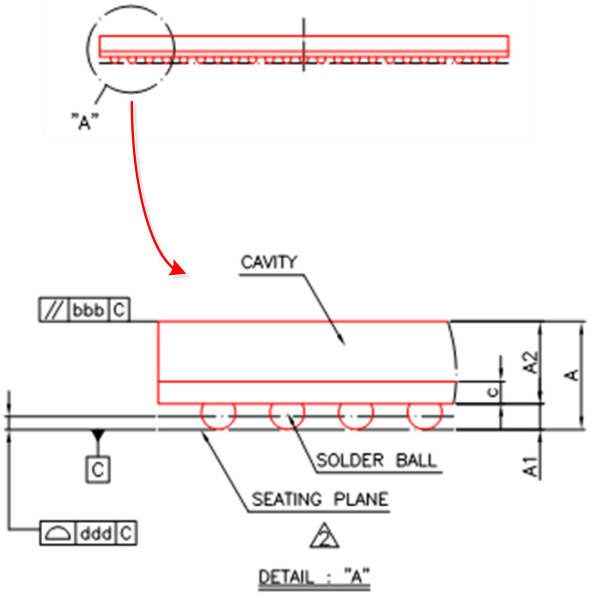


Fig. 2-2 RK3188T TFBGA453 Package Side View

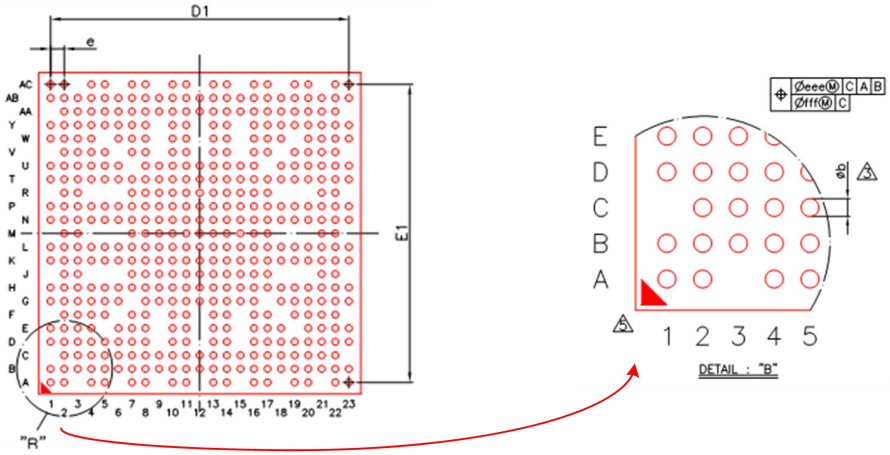


Fig. 2-3 RK3188T TFBGA453 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Fig. 2-4 RK3188T TFBGA453 Package Dimension

2.2 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	LCD0_HSYNC	MDM3	NP	MDQS_B3	MDQ31	NP	MDQS_B1	MCSN0	NP	MRASN	MA0	NP
B	LCD0_VSYNC	MDQ24	MDQ25	MDQS_3	MDQ30	MDQ10	MDQS_1	MCKE1	MCSN1	MCASN	MBA2	MA2
C	NP	VSS	MDQ26	MDQ27	MDQ29	MDQ9	MDQ12	MDQ15	MCKE0	MWEN	MBA1	MA1
D	LCD0_D0	LCD0_DCLK	LCD0_DEN	VSS	MDQ28	MDQ8	VSS	MDQ14	NP	VSS	MBA0	NP
E	LCD0_D1	LCD0_D2	LCD0_D3	LCD0_D4	NP	MDM1	MDQ11	MDQ13	NP	MRETEN	MRESET	NP
F	NP	LCD0_D9	LCD0_D8	LCD0_D7	LCD0_D6	NP	MVDD	MVDD	NP	MVDD	MVDD	NP
G	LCD0_D14	LCD0_D13	LCD0_D12	LCD0_D11	LCD0_D10	LCD0_D5	NP	CVDD_1V0	VSS	CVDD_1V0	MVDDAO	MVREFAO
H	LCD0_D20	LCD0_D19	LCD0_D18	LCD0_D17	LCD0_D16	LCD0_D15	CVDD_1V0	VSS	VSS	VSS	VSS	VSS
J	NP	LCD0_D23	LCD0_D22	NP	NP	NP	LCD0_VCC1	VSS	VSS	VSS	VSS	VSS
K	LCD0_D21	GPIO2_A5/LCD1_D5/SMC_D5	GPIO2_A4/LCD1_D4/SMC_D4	GPIO2_A3/LCD1_D3/SMC_D3	GPIO2_A1/LCD1_D1/SMC_D1	GPIO2_A0/LCD1_D0/SMC_D0	LCD0_VCC0	VSS	VSS	VSS	VSS	VSS
L	GPIO2_B3/LCD1_D11/SMC_D11	GPIO2_B2/LCD1_D10/SMC_D10	GPIO2_B1/LCD1_D9/SMC_D9	GPIO2_A2/LCD1_D2/SMC_D2	GPIO2_A7/LCD1_D7/SMC_D7	GPIO2_A6/LCD1_D6/SMC_D6	LCD1_VCC	VSS	VSS	VSS	VSS	VSS
M	NP	GPIO2_B4/LCD1_D12/SMC_D12	GPIO2_B0/LCD1_D8/SMC_D8	NP	NP	NP	CIF_VCC	VSS	VSS	VSS	VSS	VSS
N	GPIO2_C1/LCD1_D17/SMC_A1	GPIO2_C0/LCD1_D16/SMC_A0	GPIO2_B7/LCD1_D15/SMC_D15	GPIO2_B5/LCD1_D13/SMC_D13	AVDD	AVDD	CVDD_1V0	VSS	VSS	VSS	VSS	VSS

P	GPIO2_C2/ LCD1_D18 /SMC_A2	GPIO2_C3/ LCD1_D19 /SMC_A3	GPIO2_C4/ LCD1_D20 /SMC_A4	GPIO2_B6/ LCD1_D14 /SMC_D14	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS
R	NP	GPIO2_C6/ LCD1_D22 /SMC_A6	GPIO2_C5/ LCD1_D21 /SMC_A5	NP	NP	NP	VSS	VSS	VSS	VSS	VSS	VSS
T	GPIO2_D0 /LCD1_DC LK/SMC_C SN0	GPIO2_D1 /LCD1_DE N/SMC_W EN	GPIO2_D2 /LCD1_HS YNC/SMC_ OEN	GPIO2_C7/ LCD1_D23 /SMC_A7	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS
U	GPIO2_D3 /LCD1_VS YNC/SMC_ ADVN	GPIO2_D4 /SMC_BLS _N0	GPIO2_D5 /SMC_BLS _N1	GPIO2_D6 /SMC_CSN 1	AVDD	AVDD	NP	AVDD	AVDD	AVDD	APLL_AVS S	C/GPLL_AV SS
V	NP	CIF_CLKI/ TS_CLKO	VSS	CIF_D6/TS _D4	AVDD	NP	AVDD	AVDD	NP	AVDD	APLL_1V0	NP
W	CIF_D3/TS _D1	CIF_D4/TS _D2	CIF_D5/TS _D3	CIF_D9/TS _D7	NP	GPIO0_A5	GPIO0_A3	GPIO0_B0	NP	AVDD_CO M	GPIO0_A6	NP
Y	CIF_D12	CIF_D13	CIF_D7/TS _D5	CIF_D8/TS _D6	CIF_CLKO/ GPIO3_B3	GPIO0_A1	TEST	GPIO0_B3	NP	EFUSE	GPIO0_B6	NP
AA	NP	CIF_D14	CIF_VSYN C/TS_SYN C	CIF_D10/I 2C3_SDA/ GPIO3_B6	GPIO0_A2	GPIO0_A4	GPIO0_B1	VSS	DDRIO_PW ROFF	DDRIO_RE T_EN	GPIO0_B7	GPIO1_A4/ UART1_RX /SPI0_RXD
AB	CIF_D15	CIF_HREF	CIF_D2/TS _D0	CIF_D11/I 2C3_SCL/ GPIO3_B7	CLK32K_I N	GPIO0_B2	CPU_PWR OFF	XIN24M	CORE_PW ROFF	GPIO0_B5	GPIO1_B7/ SPI0_CSN 1	GPIO1_A7/ UART1_RT SN/SPI0_C SN0
AC	CIF_D1/TS _D9/GPIO 3_B5	CIF_D0/TS _D8/GPIO 3_B4	NP	GPIO0_A0	NPOR	NP	GPIO0_A7	XOUT24M	NP	GPIO0_B4	GPIO1_D6 /I2C4_SDA	NP
	1	2	3	4	5	6	7	8	9	10	11	12

13	14	15	16	17	18	19	20	21	22	23	
MCK_N	MA5	NP	MA15	MDQ18	NP	MDQS_B2	MDQ19	NP	MDQS_B0	MDQ4	A
MCK	MA6	MA11	MA14	MDQ17	MDQ21	MDQS_2	MDQ22	MDQ23	MDQS_0	MDQ5	B
MA4	MA7	MA10	MA13	MODT1	MDQ16	MDQ20	MDM2	VSS	MDQ2	NP	C
VSS	MA8	NP	VSS	MODT0	MA12	VSS	MDM0	MDQ1	MDQ3	MDQ6	D
MA3	MA9	NP	MT_ATO	MT_DTO1	MT_DTO0	NP	GPIO1_D5/ I2C2_SCL	VSS	MDQ0	MDQ7	E
MVDD	MVDD	NP	MVDD	MVDD	NP	JTAG_SEL	GPIO3_B2	GPIO1_D4/ I2C2_SDA	GPIO2_D7	NP	F
MVREF	VSS	MPZQ	CVDD_1V0	NP	CVDD_1V0	GPIO1_D3/ I2C1_SCL	GPIO1_D2/ I2C1_SDA	GPIO1_D1/ I2C0_SCL	GPIO1_D0/ I2C0_SDA	GPIO3_D0/ SDMMC1_PWR/MII_MD	G
VSS	VSS	VSS	VSS	CVDD_1V0	VCCIO1	ADC_IN2	ADC_IN1	ADC_IN0	GPIO3_D1/ SDMMC1_BACKEND/MII_MDCLK	GPIO3_D2/ SDMMC1_INT	H
VSS	VSS	VSS	VSS	CVDD_1V0	NP	NP	NP	GPIO3_C6/ SDMMC1_DET/RMII_RX_ERR	GPIO3_C7/ SDMMC1_WP/RMII_CSR_VALID	NP	J
VSS	VSS	VSS	VSS	VCCIO0	ADCVDD_1V8	GPIO3_C3/ SDMMC1_D2/RMII_RX_D0	GPIO3_C4/ SDMMC1_D3/RMII_RX_D1	GPIO3_C5/ SDMMC1_CLKO/RMII_CLKO	GPIO3_C1/ SDMMC1_D0/RMII_TX_D1	GPIO3_C2/ SDMMC1_D1/RMII_TX_D0	K
VSS	VSS	VSS	VSS	CVDD_1V0	CVDD_1V0	GPIO1_A1/ UART0_TX	GPIO1_A0/ UART0_RX	GPIO1_A2/ UART0_CTSN	GPIO3_C0/ SDMMC1_CMD/RMII_TX_EN	GPIO1_A3/ UART0_RTSN	L
VSS	VSS	VSS	VSS	CVDD_1V0	NP	NP	NP	GPIO3_B0/ SDMMC0_DET	GPIO3_B1/ SDMMC0_WP	NP	M
VSS	VSS	VSS	VSS	VSS	FLASH_VCC	GPIO3_A0/ SDMMC0_RSTN	GPIO1_B6/ SPDIF_TX/ SPI1_CSN1	GPIO3_A1/ SDMMC0_PWR	GPIO3_D7	GPIO3_D3/ PWM0	N

VSS	VSS	VSS	VSS	VSS	CVDD_1V0	GPIO1_B1/UART2_TX/JTAG_TDO	GPIO1_B0/UART2_RX/JTAG_TDI	GPIO1_B5/UART3_RTSN	GPIO3_D5/PWM2/JTAG_TCK	GPIO3_D6/PWM3/JTAG_TMS	P
VSS	VSS	VSS	VSS	CVDD_1V0	NP	NP	NP	GPIO0_D5/SPI1_TX	GPIO3_D4/PWM1/JTAG_TRSTN	NP	R
VSS	VSS	VSS	VSS	CVDD_1V0	GPIO3_A3/SDMMC0_CMD	GPIO3_A2/SDMMC0_CLKO	GPIO0_D7/SPI1_CSN0	GPIO0_D6/SPI1_CLK	GPIO1_B3/UART3_TX/GPS_SIG	GPIO1_B4/UART3_CTSN/GPS_CLK	T
DPLL_AVSS	USBDVDD_1V0	USBVDD_3V3	HSIC_VDD12	NP	AP1_VCC	FLASH_ALE	GPIO3_A7/SDMMC0_D3	GPIO1_B2/UART3_RX/GPS_MAG	GPIO3_A5/SDMMC0_D1	GPIO0_D4/SPI1_RX	U
C/GPLL_1V0	DPLL_1V0	NP	USBVDD_1V8	AP0_VCC	NP	GPIO0_C6/FLASH_D14	GPIO3_A4/SDMMC0_D0	GPIO0_C5/FLASH_D13	GPIO3_A6/SDMMC0_D2	NP	V
PVCC_3V3	PVDD_1V0	NP	GPIO1_C1/I2S_SCLK	FLASH_RDY	FLASH_CLE	NP	GPIO0_C1/FLASH_D9	GPIO0_C2/FLASH_D10	GPIO0_C0/FLASH_D8	GPIO0_C7/FLASH_D15	W
GPIO1_C0/I2S_CLK	GPIO1_C3/I2S_LRCK_TX	NP	GPIO1_A5/UART1_TX/SPI0_TXD	OTG_ID	FLASH_WP/EMMC_PWR	FLASH_CSN0	GPIO0_D1/FLASH_CSN1	FLASH_D5/EMMC_D5	FLASH_D3/EMMC_D3	GPIO0_C3/FLASH_D11	Y
GPIO1_A6/UART1_CTSN/SPI0_CLK	VSS	GPIO1_D7/I2C4_SCL	VSS	OTG_VBUS	VSS	FLASH_WRN	GPIO0_D3/FLASH_CSN3/EMMC_RSTN	FLASH_D2/EMMC_D2	GPIO0_D2/FLASH_CSN2/EMMC_CMD	NP	AA
GPIO1_C4/I2S_SDI	OTG_DM	OTG_RKELVIN	HOST_DM	HSIC_STROBE	HSIC_DATA	FLASH_RDN	GPIO0_D0/FALSH_DQS/EMMC_CLKO	FLASH_D1/EMMC_D1	FLASH_D7/EMMC_D7	GPIO0_C4/FLASH_D12	AB
GPIO_C5/I2S_SDO	OTG_DP	NP	HOST_DP	HOST_RKELVIN	NP	GPIO1_C2/I2S_LRCK_RX	FLASH_D0/EMMC_D0	NP	FLASH_D4/EMMC_D4	FLASH_D6/EMMC_D6	AC
13	14	15	16	17	18	19	20	21	22	23	

Fig. 2-5 RK3188T Ball Mapping Diagram

2.3 Ball Pin Number Order

Table 2-1 RK3188T Ball Pin Number Order Information

Ball #	Pin Name	Ball #	Pin Name	Ball #	Pin Name
A1	LCD0_HSYNC	B1	LCD0_VSYNC	C1	NC
A2	MDM3	B2	MDQ24	C2	VSS
A3	NC	B3	MDQ25	C3	MDQ26
A4	MDQS_B3	B4	MDQS_3	C4	MDQ27
A5	MDQ31	B5	MDQ30	C5	MDQ29
A6	NC	B6	MDQ10	C6	MDQ9
A7	MDQS_B1	B7	MDQS_1	C7	MDQ12
A8	MCSN0	B8	MCKE1	C8	MDQ15
A9	NC	B9	MCSN1	C9	MCKE0
A10	MRASN	B10	MCASN	C10	MWEN
A11	MA0	B11	MBA2	C11	MBA1
A12	NC	B12	MA2	C12	MA1
A13	MCK_N	B13	MCK	C13	MA4
A14	MA5	B14	MA6	C14	MA7
A15	NC	B15	MA11	C15	MA10
A16	MA15	B16	MA14	C16	MA13
A17	MDQ18	B17	MDQ17	C17	MODT1
A18	NC	B18	MDQ21	C18	MDQ16
A19	MDQS_B2	B19	MDQS_2	C19	MDQ20
A20	MDQ19	B20	MDQ22	C20	MDM2
A21	NC	B21	MDQ23	C21	VSS
A22	MDQS_B0	B22	MDQS_0	C22	MDQ2
A23	MDQ4	B23	MDQ5	C23	NC
D1	LCD0_D0	E1	LCD0_D1	F1	NC
D2	LCD0_DCLK	E2	LCD0_D2	F2	LCD0_D9
D3	LCD0_DEN	E3	LCD0_D3	F3	LCD0_D8
D4	VSS	E4	LCD0_D4	F4	LCD0_D7
D5	MDQ28	E5	NC	F5	LCD0_D6
D6	MDQ8	E6	MDM1	F6	NC
D7	VSS	E7	MDQ11	F7	MVDD
D8	MDQ14	E8	MDQ13	F8	MVDD
D9	NC	E9	NC	F9	NC
D10	VSS	E10	MRETEN	F10	MVDD
D11	MBA0	E11	MRESET	F11	MVDD
D12	NC	E12	NC	F12	NC
D13	VSS	E13	MA3	F13	MVDD
D14	MA8	E14	MA9	F14	MVDD
D15	NC	E15	NC	F15	NC
D16	VSS	E16	MT_ATO	F16	MVDD
D17	MODT0	E17	MT_DTO1	F17	MVDD
D18	MA12	E18	MT_DTO0	F18	NC
D19	VSS	E19	NC	F19	JTAG_SEL

D20	MDM0	E20	GPIO1_D5/I2C2_SCL	F20	GPIO3_B2
D21	MDQ1	E21	VSS	F21	GPIO1_D4/I2C2_SDA
D22	MDQ3	E22	MDQ0	F22	GPIO2_D7
D23	MDQ6	E23	MDQ7	F23	NC
G1	LCD0_D14	H1	LCD0_D20	J1	NC
G2	LCD0_D13	H2	LCD0_D19	J2	LCD0_D23
G3	LCD0_D12	H3	LCD0_D18	J3	LCD0_D22
G4	LCD0_D11	H4	LCD0_D17	J4	NC
G5	LCD0_D10	H5	LCD0_D16	J5	NC
G6	LCD0_D5	H6	LCD0_D15	J6	NC
G7	NC	H7	CVDD_1V0	J7	LCD0_VCC1
G8	CVDD_1V0	H8	VSS	J8	VSS
G9	VSS	H9	VSS	J9	VSS
G10	CVDD_1V0	H10	VSS	J10	VSS
G11	MVDDAO	H11	VSS	J11	VSS
G12	MVREFAO	H12	VSS	J12	VSS
G13	MVREF	H13	VSS	J13	VSS
G14	VSS	H14	VSS	J14	VSS
G15	MPZQ	H15	VSS	J15	VSS
G16	CVDD_1V0	H16	VSS	J16	VSS
G17	NC	H17	CVDD_1V0	J17	CVDD_1V0
G18	CVDD_1V0	H18	VCCIO1	J18	NC
G19	GPIO1_D3/I2C1_SCL	H19	ADC_IN2	J19	NC
G20	GPIO1_D2/I2C1_SDA	H20	ADC_IN1	J20	NC
G21	GPIO1_D1/I2C0_SCL	H21	ADC_IN0	J21	GPIO3_C6/SDMMC1_DET/RMII_RX_ERR
G22	GPIO1_D0/I2C0_SDA	H22	GPIO3_D1/SDMMC1_BACKEND/MII_MDCLK	J22	GPIO3_C7/SDMMC1_WP/RMII_CSR_VALID
G23	GPIO3_D0/SDMMC1_PWR/MII_MD	H23	GPIO3_D2/SDMMC1_INT	J23	NC
K1	LCD0_D21	L1	GPIO2_B3/LCD1_D11/SMC_D11	M1	NC
K2	GPIO2_A5/LCD1_D5/SMC_D5	L2	GPIO2_B2/LCD1_D10/SMC_D10	M2	GPIO2_B4/LCD1_D12/SMC_D12
K3	GPIO2_A4/LCD1_D4/SMC_D4	L3	GPIO2_B1/LCD1_D9/SMC_D9	M3	GPIO2_B0/LCD1_D8/SMC_D8
K4	GPIO2_A3/LCD1_D3/SMC_D3	L4	GPIO2_A2/LCD1_D2/SMC_D2	M4	NC
K5	GPIO2_A1/LCD1_D1/SMC_D1	L5	GPIO2_A7/LCD1_D7/SMC_D7	M5	NC
K6	GPIO2_A0/LCD1_D0/SMC_D0	L6	GPIO2_A6/LCD1_D6/SMC_D6	M6	NC
K7	LCD0_VCC0	L7	LCD1_VCC	M7	CIF_VCC
K8	VSS	L8	VSS	M8	VSS
K9	VSS	L9	VSS	M9	VSS
K10	VSS	L10	VSS	M10	VSS
K11	VSS	L11	VSS	M11	VSS
K12	VSS	L12	VSS	M12	VSS
K13	VSS	L13	VSS	M13	VSS
K14	VSS	L14	VSS	M14	VSS

K15	VSS	L15	VSS	M15	VSS
K16	VSS	L16	VSS	M16	VSS
K17	VCCIO0	L17	CVDD_1V0	M17	CVDD_1V0
K18	ADCVDD_1V8	L18	CVDD_1V0	M18	NC
K19	GPIO3_C3/SDMMC1_D2/RMII_RX_D0	L19	GPIO1_A1/UART0_TX	M19	NC
K20	GPIO3_C4/SDMMC1_D3/RMII_RX_D1	L20	GPIO1_A0/UART0_RX	M20	NC
K21	GPIO3_C5/SDMMC1_CLKO/RMII_CLKO	L21	GPIO1_A2/UART0_CTSN	M21	GPIO3_B0/SDMMC0_DET
K22	GPIO3_C1/SDMMC1_D0/RMII_TX_D1	L22	GPIO3_C0/SDMMC1_CMD/RMII_TX_EN	M22	GPIO3_B1/SDMMC0_WP
K23	GPIO3_C2/SDMMC1_D1/RMII_TX_D0	L23	GPIO1_A3/UART0_RTSN	M23	NC
N1	GPIO2_C1/LCD1_D17/SMC_A1	P1	GPIO2_C2/LCD1_D18/SMC_A2	R1	NC
N2	GPIO2_C0/LCD1_D16/SMC_A0	P2	GPIO2_C3/LCD1_D19/SMC_A3	R2	GPIO2_C6/LCD1_D22/SMC_A6
N3	GPIO2_B7/LCD1_D15/SMC_D15	P3	GPIO2_C4/LCD1_D20/SMC_A4	R3	GPIO2_C5/LCD1_D21/SMC_A5
N4	GPIO2_B5/LCD1_D13/SMC_D13	P4	GPIO2_B6/LCD1_D14/SMC_D14	R4	NC
N5	AVDD	P5	AVDD	R5	NC
N6	AVDD	P6	AVDD	R6	NC
N7	CVDD_1V0	P7	VSS	R7	VSS
N8	VSS	P8	VSS	R8	VSS
N9	VSS	P9	VSS	R9	VSS
N10	VSS	P10	VSS	R10	VSS
N11	VSS	P11	VSS	R11	VSS
N12	VSS	P12	VSS	R12	VSS
N13	VSS	P13	VSS	R13	VSS
N14	VSS	P14	VSS	R14	VSS
N15	VSS	P15	VSS	R15	VSS
N16	VSS	P16	VSS	R16	VSS
N17	VSS	P17	VSS	R17	CVDD_1V0
N18	FLASH_VCC	P18	CVDD_1V0	R18	NC
N19	GPIO3_A0/SDMMC0_RSTN	P19	GPIO1_B1/UART2_TX/JTAG_TDO	R19	NC
N20	GPIO1_B6/SPDIF_TX/SPI1_CSN1	P20	GPIO1_B0/UART2_RX/JTAG_TDI	R20	NC
N21	GPIO3_A1/SDMMC0_PWR	P21	GPIO1_B5/UART3_RTSN	R21	GPIO0_D5/SPI1_TX
N22	GPIO3_D7	P22	GPIO3_D5/PWM2/JTAG_TCK	R22	GPIO3_D4/PWM1/JTAG_TRSTN
N23	GPIO3_D3/PWM0	P23	GPIO3_D6/PWM3/JTAG_TMS	R23	NC
T1	GPIO2_D0/LCD1_DCLK/SMC_CSN0	U1	GPIO2_D3/LCD1_VSYNC/SMC_ADVN	V1	NC
T2	GPIO2_D1/LCD1_DEN/SMC_WEN	U2	GPIO2_D4/SMC_BLS_N0	V2	CIF_CLKI/TS_CLKO

T3	GPIO2_D2/LCD1_HSYNC/SMC_OEN	U3	GPIO2_D5/SMC_BLS_N1	V3	VSS
T4	GPIO2_C7/LCD1_D23/SMC_A7	U4	GPIO2_D6/SMC_CSN1	V4	CIF_D6/TS_D4
T5	AVDD	U5	AVDD	V5	AVDD
T6	AVDD	U6	AVDD	V6	NC
T7	VSS	U7	NC	V7	AVDD
T8	VSS	U8	AVDD	V8	AVDD
T9	VSS	U9	AVDD	V9	NC
T10	VSS	U10	AVDD	V10	AVDD
T11	VSS	U11	APLL_AVSS	V11	APLL_1V0
T12	VSS	U12	DPLL_AVSS	V12	NC
T13	VSS	U13	C/GPLL_AVSS	V13	DPLL_1V0
T14	VSS	U14	USBDVDD_1V0	V14	C/GPLL_1V0
T15	VSS	U15	USBVDD_3V3	V15	NC
T16	VSS	U16	HSIC_VDD12	V16	USBVDD_1V8
T17	CVDD_1V0	U17	NC	V17	AP0_VCC
T18	GPIO3_A3/SDMMC0_CMD	U18	AP1_VCC	V18	NC
T19	GPIO3_A2/SDMMC0_CLKO	U19	FLASH_ALE	V19	GPIO0_C6/FLASH_D14
T20	GPIO0_D7/SPI1_CSN0	U20	GPIO3_A7/SDMMC0_D3	V20	GPIO3_A4/SDMMC0_D0
T21	GPIO0_D6/SPI1_CLK	U21	GPIO1_B2/UART3_RX/GPS_MAG	V21	GPIO0_C5/FLASH_D13
T22	GPIO1_B3/UART3_TX/GPS_SIG	U22	GPIO3_A5/SDMMC0_D1	V22	GPIO3_A6/SDMMC0_D2
T23	GPIO1_B4/UART3_CTSN/GPS_CLK	U23	GPIO0_D4/SPI1_RX	V23	NC
W1	CIF_D3/TS_D1	Y1	CIF_D12	AA1	NC
W2	CIF_D4/TS_D2	Y2	CIF_D13	AA2	CIF_D14
W3	CIF_D5/TS_D3	Y3	CIF_D7/TS_D5	AA3	CIF_VSYNC/TS_SYNC
W4	CIF_D9/TS_D7	Y4	CIF_D8/TS_D6	AA4	CIF_D10/I2C3_SDA/GPIO3_B6
W5	NC	Y5	CIF_CLKO/GPIO3_B3	AA5	GPIO0_A2
W6	GPIO0_A5	Y6	GPIO0_A1	AA6	GPIO0_A4
W7	GPIO0_A3	Y7	TEST	AA7	GPIO0_B1
W8	GPIO0_B0	Y8	GPIO0_B3	AA8	VSS
W9	NC	Y9	NC	AA9	DDRIO_PWROFF
W10	AVDD_COM	Y10	EFUSE	AA10	DDRIO_RET_EN
W11	GPIO0_A6	Y11	GPIO0_B6	AA11	GPIO0_B7
W12	NC	Y12	NC	AA12	GPIO1_A4/UART1_RX/SPI0_RXD
W13	PVCC_3V3	Y13	GPIO1_C0/I2S_CLK	AA13	GPIO1_A6/UART1_CTSN/SPI0_CLK
W14	PVDD_1V0	Y14	GPIO1_C3/I2S_LRCK_TX	AA14	VSS
W15	NC	Y15	NC	AA15	GPIO1_D7/I2C4_SCL
W16	GPIO1_C1/I2S_SCLK	Y16	GPIO1_A5/UART1_TX/SPI0_TXD	AA16	VSS
W17	FLASH_RDY	Y17	OTG_ID	AA17	OTG_VBUS
W18	FLASH_CLE	Y18	FLASH_WP/EMMC_PWR	AA18	VSS
W19	NC	Y19	FLASH_CSN0	AA19	FLASH_WRN

W20	GPIO0_C1/FLASH_D9	Y20	GPIO0_D1/FLASH_CSN1	AA20	GPIO0_D3/FLASH_CSN3/EMMC_RSTN
W21	GPIO0_C2/FLASH_D10	Y21	FLASH_D5/EMMC_D5	AA21	FLASH_D2/EMMC_D2
W22	GPIO0_C0/FLASH_D8	Y22	FLASH_D3/EMMC_D3	AA22	GPIO0_D2/FLASH_CSN2/EMMC_CMD
W23	GPIO0_C7/FLASH_D15	Y23	GPIO0_C3/FLASH_D11	AA23	NC
AB1	CIF_D15	AC1	CIF_D1/TS_D9/GPIO3_B5		
AB2	CIF_HREF	AC2	CIF_D0/TS_D8/GPIO3_B4		
AB3	CIF_D2/TS_D0	AC3	NC		
AB4	CIF_D11/I2C3_SCL/GPIO3_B7	AC4	GPIO0_A0		
AB5	CLK32K_IN	AC5	NPOR		
AB6	GPIO0_B2	AC6	NC		
AB7	CPU_PWROFF	AC7	GPIO0_A7		
AB8	XIN24M	AC8	XOUT24M		
AB9	CORE_PWROFF	AC9	NC		
AB10	GPIO0_B5	AC10	GPIO0_B4		
AB11	GPIO1_B7/SPI0_CSN1	AC11	GPIO1_D6/I2C4_SDA		
AB12	GPIO1_A7/UART1_RTSN/SPI0_CSN0	AC12	NC		
AB13	GPIO1_C4/I2S_SDI	AC13	GPIO_C5/I2S_SDO		
AB14	OTG_DM	AC14	OTG_DP		
AB15	OTG_RKELVIN	AC15	NC		
AB16	HOST_DM	AC16	HOST_DP		
AB17	HSIC_STROBE	AC17	HOST_RKELVIN		
AB18	HSIC_DATA	AC18	NC		
AB19	FLASH_RDN	AC19	GPIO1_C2/I2S_LRCK_RX		
AB20	GPIO0_D0/FALSH_DQS/EMMC_CLKO	AC20	FLASH_D0/EMMC_D0		
AB21	FLASH_D1/EMMC_D1	AC21	NC		
AB22	FLASH_D7/EMMC_D7	AC22	FLASH_D4/EMMC_D4		
AB23	GPIO0_C4/FLASH_D12	AC23	FLASH_D6/EMMC_D6		

2.4 Power/ground IO descriptions

Table 2-2 RK3188T Power/Ground IO information

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C2, D4, D7, D10, D13, D16, D19, C21, E21, G9, G14, H8, H9, H10, H11, H12, H13, H14, H15, H16, J8, J9, J10, J11, J12, J13, J14, J15, J16, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, L16, M8, M9, M10, M11, M12, M13, M14, M15, M16, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R8, R9, R10, R11, R12, R13, R14, R15, R16, T7, T8, T9, T11, T12, T13, T14, T15, T16, V3, AA8, AA14, AA16, AA18, R7, T10	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
AVDD	N5, N6, P5, P6, T5, T6, U5, U6, V5, V7, U8, U9, U10, V8, V10	0.9	1.0	1.05	Internal CPU Power (@ cpu frequency <= 1GHz)
		0.9	1.0	1.25	Internal CPU Power (@ cpu frequency <= 1.5GHz)
CVDD	G8, G10, G16, G18, H17, J17, H7, N7, L17, L18, M17, P18, R17, T17	0.9	1.0	1.2	Internal Core Logic Power
PVDD	W14	0.9	1.0	1.1	Internal PMU Domain Logic Power
PVCC	W13	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	PMU Domain Digital IO Power
VCCIO0	K17	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	Digital GPIO Power
VCCIO1	H18	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	
LCD0_VCC0	K7	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	LCDC0 Digital IO Power

LCD0_VCC1	J7	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	
LCD1_VCC	L7	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	LCDC1 Digital IO Power
CIF_VCC	M7	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	Camera Digital IO Power
FLASH_VCC	N18	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	Nand Flash Digital IO Power
AP0_VCC	V17	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	UART0/SDIO/MAC for Mobile phone Digital IO Power
AP1_VCC	U18	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	UART1/SPI0/I2S/I2C4 for Mobile phone Digital IO Power
MVDD	F7, F8, F10, F11, F13, F14, F16, F17	1.425 1.14	1.5 1.2	1.575 1.30	DDR3 Digital IO Power LPDDR2 Digital IO Power
APLL_AVSS	U11	N/A	N/A	N/A	ARM PLL Analog Ground
APLL_AVDD	V11	0.9	1.0	1.1	ARM PLL Analog Power
DPLL_AVSS	V13	N/A	N/A	N/A	DDR PLL Analog Ground
DPLL_AVDD	V13	0.9	1.0	1.1	DDR PLL Analog Power
CGPLL_AVSS	U13	N/A	N/A	N/A	CODEC/GENERAL PLL Analog Ground
CGPLL_1V0	V14	0.9	1.0	1.1	CODEC/GENERAL PLL Analog Power
ADCVDD_1V8	K18	1.62	1.8	1.98	SAR-ADC Analog Power
USBDVDD_1V0	U14	0.9	1.0	1.1	USB OTG2.0/Host2.0 Digital Power
USBVDD_1V8	V16	1.62	1.8	1.98	USB OTG2.0/Host2.0 Analog Power
USBVDD_3V3	U15	3.069	3.3	3.63	USB OTG2.0/Host2.0 Analog Power
EFUSE_VDDQ	Y10	1.35	1.5	1.65	eFuse IO Digital Power

HSIC	U16	1.08	1.2	1.32	HSIC 1.2V Transmitter Power Supply

2.5 Function IO descriptions

Table 2-3 RK3188T IO descriptions

Pad#	Ball#	func0	func1	func2	func3	Pad type[1]	Current[2]	Pull	Reset State[3]	Power Supply[4]:
LCDC0_DATA[7]	F4	LCDC0_DATA[7]				I/O	8	N/A	O	
LCDC0_DATA[8]	F3	LCDC0_DATA[8]				I/O	8	N/A	O	
LCDC0_DATA[9]	F2	LCDC0_DATA[9]				I/O	8	N/A	O	
LCDC0_DATA[10]	G5	LCDC0_DATA[10]				I/O	8	N/A	O	
LCDC0_DATA[11]	G4	LCDC0_DATA[11]				I/O	8	N/A	O	
LCDC0_DATA[12]	G3	LCDC0_DATA[12]				I/O	8	N/A	O	
LCDC0_DATA[13]	G2	LCDC0_DATA[13]				I/O	8	N/A	O	
LCDC0_DATA[14]	G1	LCDC0_DATA[14]				I/O	8	N/A	O	
LCDC0_DATA[15]	H6	LCDC0_DATA[15]				I/O	8	N/A	O	LCDC0_VCC
LCDC0_DATA[16]	H5	LCDC0_DATA[16]				I/O	8	N/A	O	
LCDC0_DATA[17]	H4	LCDC0_DATA[17]				I/O	8	N/A	O	
LCDC0_DATA[18]	H3	LCDC0_DATA[18]				I/O	8	N/A	O	
LCDC0_DATA[19]	H2	LCDC0_DATA[19]				I/O	8	N/A	O	
LCDC0_DATA[20]	H1	LCDC0_DATA[20]				I/O	8	N/A	O	
LCDC0_DATA[21]	K1	LCDC0_DATA[21]				I/O	8	N/A	O	
LCDC0_DATA[22]	J3	LCDC0_DATA[22]				I/O	8	N/A	O	
LCDC0_DATA[23]	J2	LCDC0_DATA[23]				I/O	8	N/A	O	
GPIO2_A[0]	K6	GPIO2_A[0]	lcdc1_data0	smc_data0	trace_data0	I/O	8	Down[6]	I	
GPIO2_A[1]	K5	GPIO2_A[1]	lcdc1_data1	smc_data1	trace_data1	I/O	8	Down[6]	I	
GPIO2_A[2]	L4	GPIO2_A[2]	lcdc1_data2	smc_data2	trace_data2	I/O	8	Down[6]	I	
GPIO2_A[3]	K4	GPIO2_A[3]	lcdc1_data3	smc_data3	trace_data3	I/O	8	Down[6]	I	
GPIO2_A[4]	K3	GPIO2_A[4]	lcdc1_data4	smc_data4	trace_data4	I/O	8	Down[6]	I	
GPIO2_A[5]	K2	GPIO2_A[5]	lcdc1_data5	smc_data5	trace_data5	I/O	8	Down[6]	I	LCDC1_VCC
GPIO2_A[6]	L6	GPIO2_A[6]	lcdc1_data6	smc_data6	trace_data6	I/O	8	Down[6]	I	
GPIO2_A[7]	L5	GPIO2_A[7]	lcdc1_data7	smc_data7	trace_data7	I/O	8	Down[6]	I	
GPIO2_B[0]	M3	GPIO2_B[0]	lcdc1_data8	smc_data8	trace_data8	I/O	8	Down[6]	I	
GPIO2_B[1]	L3	GPIO2_B[1]	lcdc1_data9	smc_data9	trace_data9	I/O	8	Down[6]	I	
GPIO2_B[2]	L2	GPIO2_B[2]	lcdc1_data10	smc_data10	trace_data10	I/O	8	Down[6]	I	
GPIO2_B[3]	L1	GPIO2_B[3]	lcdc1_data11	smc_data11	trace_data11	I/O	8	Down[6]	I	
GPIO2_B[4]	M2	GPIO2_B[4]	lcdc1_data12	smc_data12	trace_data12	I/O	8	Down[6]	I	
GPIO2_B[5]	N4	GPIO2_B[5]	lcdc1_data13	smc_data13	trace_data13	I/O	8	Down[6]	I	
GPIO2_B[6]	P4	GPIO2_B[6]	lcdc1_data14	smc_data14	trace_data14	I/O	8	Down[6]	I	
GPIO2_B[7]	N3	GPIO2_B[7]	lcdc1_data15	smc_data15	trace_data15	I/O	8	Down[6]	I	
GPIO2_C[0]	N2	GPIO2_C[0]	lcdc1_data16	smc_addr0	trace_clk	I/O	8	Down[6]	I	
GPIO2_C[1]	N1	GPIO2_C[1]	lcdc1_data17	smc_addr1	trace_ctl	I/O	8	Down[6]	I	
GPIO2_C[2]	P1	GPIO2_C[2]	lcdc1_data18	smc_addr2		I/O	8	Down[6]	I	

GPIO2_C[3]	P2	GPIO2_C[3]	lcdc1_data19	smc_addr3		I/O	8	Down⑥	I	
GPIO2_C[4]	P3	GPIO2_C[4]	lcdc1_data20	smc_addr4		I/O	8	Down⑥	I	
GPIO2_C[5]	R3	GPIO2_C[5]	lcdc1_data21	smc_addr5		I/O	8	Down⑥	I	
GPIO2_C[6]	R2	GPIO2_C[6]	lcdc1_data22	smc_addr6		I/O	8	Down⑥	I	
GPIO2_C[7]	T4	GPIO2_C[7]	lcdc1_data23	smc_addr7		I/O	8	Down⑥	I	
GPIO2_D[0]	T1	GPIO2_D[0]	lcdc1_dclk	smc_csn0		I/O	12	Down⑥	I	
GPIO2_D[1]	T2	GPIO2_D[1]	lcdc1_den	smc_we_n		I/O	8	Down⑥	I	
GPIO2_D[2]	T3	GPIO2_D[2]	lcdc1_hsync	smc_oe_n		I/O	8	Down⑥	I	
GPIO2_D[3]	U1	GPIO2_D[3]	lcdc1_vsync	smc_adv_n		I/O	8	Down⑥	I	
GPIO2_D[4]	U2	GPIO2_D[4]	smc_bls_n0			I/O	4	Up⑥	I	
GPIO2_D[5]	U3	GPIO2_D[5]	smc_bls_n1			I/O	4	Up⑥	I	
GPIO2_D[6]	U4	GPIO2_D[6]	smc_csn1			I/O	4	Up⑥	I	
CIF_CLKIN	V2	CIF_CLKIN	hsadc_clkout	gps_clk		I/O	2	down	I	CIF_VCC
CIF_DATA[3]	W1	CIF_DATA[3]	hsadc_data1			I	2	down	I	
CIF_DATA[4]	W2	CIF_DATA[4]	hsadc_data2			I	2	down	I	
CIF_DATA[5]	W3	CIF_DATA[5]	hsadc_data3			I	2	down	I	
CIF_DATA[6]	V4	CIF_DATA[6]	hsadc_data4			I	2	down	I	
CIF_DATA[7]	Y3	CIF_DATA[7]	hsadc_data5			I	2	down	I	
CIF_DATA[8]	Y4	CIF_DATA[8]	hsadc_data6			I	2	down	I	
CIF_DATA[9]	W4	CIF_DATA[9]	hsadc_data7			I	2	down	I	
CIF_DATA_15_12[12]	Y1	CIF_DATA_15_12[12]				I	2	down	I	
CIF_DATA_15_12[13]	Y2	CIF_DATA_15_12[13]				I	2	down	I	
CIF_DATA_15_12[14]	AA2	CIF_DATA_15_12[14]				I	2	down	I	
CIF_DATA_15_12[15]	AB1	CIF_DATA_15_12[15]				I	2	down	I	
CIF_VSYNC	AA3	CIF_VSYNC	ts_sync			I	2	down	I	
CIF_HREF	AB2	CIF_HREF				I	2	down	I	
CIF_DATA[2]	AB3	CIF_DATA[2]	hsadc_data0			I	2	down	I	
GPIO3_B[3]	Y5	GPIO3_B[3]	cif_clkout			I/O	4	Down⑥	I	
GPIO3_B[4]	AC2	GPIO3_B[4]	cif_data0	hsadc_data8		I/O	2	Down⑥	I	
GPIO3_B[5]	AC1	GPIO3_B[5]	cif_data1	hsadc_data9		I/O	2	Down⑥	I	
GPIO3_B[6]	AA4	GPIO3_B[6]	cif_data10	i2c3_sda		I/O	2	Up⑥	I	
GPIO3_B[7]	AB4	GPIO3_B[7]	cif_data11	i2c3_scl		I/O	2	Up⑥	I	
GPIO0_A[0]	AC4	GPIO0_A[0]				I/O	2	Down⑥	I	PVCC_3V3
GPIO0_A[1]	Y6	GPIO0_A[1]				I/O	2	Down⑥	I	
GPIO0_A[2]	AA5	GPIO0_A[2]				I/O	2	Down⑥	I	
GPIO0_A[3]	W7	GPIO0_A[3]				I/O	2	Down⑥	I	
GPIO0_A[4]	AA6	GPIO0_A[4]				I/O	2	Up⑥	I	
GPIO0_A[5]	W6	GPIO0_A[5]				I/O	2	Up⑥	I	
GPIO0_A[6]	W11	GPIO0_A[6]				I/O	2	Up⑥	I	
GPIO0_A[7]	AC7	GPIO0_A[7]				I/O	2	Up⑥	I	
CLK32K	AB5	CLK32K				I	2	Down	I	
NPOR	AC5	NPOR				I	2	N/A	I	
GPIO0_B[0]	W8	GPIO0_B[0]				I/O	2	Up⑥	I	
GPIO0_B[1]	AA7	GPIO0_B[1]				I/O	2	Up⑥	I	
GPIO0_B[2]	AB6	GPIO0_B[2]				I/O	2	Up⑥	I	
GPIO0_B[3]	Y8	GPIO0_B[3]				I/O	2	Up⑥	I	

CORE_PWROFF	AB9	CORE_PWROFF				O	2	Down	I	
CPU_PWROFF	AB7	CPU_PWROFF				O	2	Down	I	
XIN24M	AB8	XIN24M				I		N/A	I	
XOUT24M	AC8	XOUT24M				O		N/A	I	
VDD2_APLL	V11	1.0V				AP		N/A	NA	PLL Domain
VSS2_APLL	U11	Analog Ground				AG		N/A	NA	
VDD1_APLL	V11	1.0V				AP		N/A	NA	
VSS1_APLL	U11	Analog Ground				AG		N/A	NA	
VDD2_DPLL	U12	1.0V				AP		N/A	NA	
VSS2_DPLL	V13	Analog Ground				AG		N/A	NA	
VDD1_DPLL	U12	1.0V				AP		N/A	NA	
VSS1_DPLL	V13	Analog Ground				AG		N/A	NA	
VDD2_GPLL	V14	1.0V				AP		N/A	NA	
VSS2_GPLL	U13	Analog Ground				AG		N/A	NA	
VDD1_GPLL	V14	1.0V				AP		N/A	NA	
VSS1_GPLL	U13	Analog Ground				AG		N/A	NA	
VSS1_CPLL	U13	Analog Ground				AG		N/A	NA	
VDD1_CPLL	V14	1.0V				AP		N/A	NA	
VSS2_CPLL	U13	Analog Ground				AG		N/A	NA	
VDD2_CPLL	V14	1.0V				AP		N/A	NA	
OTG_ID	Y17	OTG_ID				A		N/A	NA	USB_OTG
OTG_DVDD	U14	OTG_DVDD				DP		N/A	NA	
OTG_VBUS	AA17	OTG_VBUS				A		N/A	NA	
OTG_VDD330	U15	OTG_VDD330				AP		N/A	NA	
OTG_DP	AC14	OTG_DP				A		N/A	NA	
OTG_DM	AB14	OTG_DM				A		N/A	NA	
OTG_RKELVIN	AB15	OTG_RKELVIN				A		N/A	NA	
OTG_VDD180	V16	OTG_VDD180				AP		N/A	NA	
HOST_DVDD	U14	HOST_DVDD				DP		N/A	NA	
HOST_VDD330	U15	HOST_VDD330				AP		N/A	NA	
HOST_DP	AC16	HOST_DP				A		N/A	NA	
HOST_DM	AB16	HOST_DM				A		N/A	NA	
HOST_RKELVIN	AC17	HOST_RKELVIN				A		N/A	NA	
HOST_VDD180	V16	HOST_VDD180				AP		N/A	NA	
HSIC_DATA	AB18	HSIC_DATA						N/A		
HSIC_VDD12	U16	HSIC_VDD12				AP		N/A	NA	
HSIC_STROBE	AB17	HSIC_STROBE						N/A		
EFUSE_VQPS	Y10	EFUSE_VQPS				AP		N/A	NA	EFUSE
GPIO0_B[4]	AC10	GPIO0_B[4]				I/O	2	Up⑥	I	AP1_VCC
GPIO0_B[5]	AB10	GPIO0_B[5]				I/O	2	Up⑥	I	
GPIO0_B[6]	Y11	GPIO0_B[6]				I/O	2	Up⑥	I	
GPIO0_B[7]	AA11	GPIO0_B[7]				I/O	2	Up⑥	I	
GPIO1_A[4]	AA12	GPIO1_A[4]	uart1_sin	spi0_rxd		I/O	2	Up⑥	I	
GPIO1_A[5]	Y16	GPIO1_A[5]	uart1_sout	spi0_txd		I/O	2	Down⑥	I	
GPIO1_A[6]	AA13	GPIO1_A[6]	uart1_cts_n	spi0_clk		I/O	2	Up⑥	I	
GPIO1_A[7]	AB12	GPIO1_A[7]	uart1_rts_n	spi0_csn0		I/O	2	Up⑥	I	

GPIO1_B[7]	AB11	GPIO1_B[7]	spi0_csn1			I/O	2	Up⑥	I	
GPIO1_D[6]	AC11	GPIO1_D[6]	i2s4_sda			I/O	2	Up⑥	I	
GPIO1_D[7]	AA15	GPIO1_D[7]	i2s4_scl			I/O	2	Up⑥	I	
GPIO1_C[0]	Y13	GPIO1_C[0]	i2s_clk			I/O	4	Down⑥	I	
GPIO1_C[1]	W16	GPIO1_C[1]	i2s_sclk			I/O	2	Down⑥	I	
GPIO1_C[2]	AC19	GPIO1_C[2]	i2s_lrck_rx			I/O	2	Down⑥	I	
GPIO1_C[3]	Y14	GPIO1_C[3]	i2s_lrck_tx			I/O	2	Down⑥	I	
GPIO1_C[4]	AB13	GPIO1_C[4]	i2s_sdi			I/O	2	Down⑥	I	
GPIO1_C[5]	AC13	GPIO1_C[5]	i2s_sdo			I/O	2	Down⑥	I	
FLASH_RDY	W17	FLASH_RDY				I/O	4	Up⑥	I	
FLASH_WP	Y18	FLASH_WP	emmc_pwr_en			O	4	Down⑥	I	
FLASH_RDN	AB19	FLASH_RDN				O	8	Up⑥	O	
FLASH_ALE	U19	FLASH_ALE				O	4	Down⑥	O	
FLASH_CLE	W18	FLASH_CLE				O	4	Down⑥	O	
FLASH_WRN	AA19	FLASH_WRN				O	8	Up⑥	O	
FLASH_CSN	Y19	FLASH_CSN				O	4	Up⑥	O	
GPIO0_D[1]	Y20	GPIO0_D[1]	flash_csn1			I/O	4	Up⑥	I	
GPIO0_D[2]	AA22	GPIO0_D[2]	flash_csn2	emmc_cmd		I/O	4	Up⑥	I	
GPIO0_D[3]	AA20	GPIO0_D[3]	flash_csn3	emmc_rstn_out		I/O	4	Up⑥	I	
GPIO0_D[0]	AB20	GPIO0_D[0]	flash_dqs	emmc_clkout		I/O	8	Down⑥	I	
FLASH_DATA[0]	AC20	FLASH_DATA[0]	emmc_data0			I/O	8	Down⑥	I	
FLASH_DATA[1]	AB21	FLASH_DATA[1]	emmc_data1			I/O	8	Down⑥	I	
FLASH_DATA[2]	AA21	FLASH_DATA[2]	emmc_data2			I/O	8	Down⑥	I	
FLASH_DATA[3]	Y22	FLASH_DATA[3]	emmc_data3			I/O	8	Down⑥	I	
FLASH_DATA[4]	AC22	FLASH_DATA[4]	emmc_data4			I/O	8	Down⑥	I	
FLASH_DATA[5]	Y21	FLASH_DATA[5]	emmc_data5			I/O	8	Down⑥	I	
FLASH_DATA[6]	AC23	FLASH_DATA[6]	emmc_data6			I/O	8	Down⑥	I	
FLASH_DATA[7]	AB22	FLASH_DATA[7]	emmc_data7			I/O	8	Down⑥	I	
GPIO0_C[0]	W22	GPIO0_C[0]	flash_data8			I/O	8	Down⑥	I	
GPIO0_C[1]	W20	GPIO0_C[1]	flash_data9			I/O	8	Down⑥	I	
GPIO0_C[2]	W21	GPIO0_C[2]	flash_data10			I/O	8	Down⑥	I	FLASH_VCC
GPIO0_C[3]	Y23	GPIO0_C[3]	flash_data11			I/O	8	Down⑥	I	
GPIO0_C[4]	AB23	GPIO0_C[4]	flash_data12			I/O	8	Down⑥	I	
GPIO0_C[5]	V21	GPIO0_C[5]	flash_data13			I/O	8	Down⑥	I	
GPIO0_C[6]	V19	GPIO0_C[6]	flash_data14			I/O	8	Down⑥	I	
GPIO0_C[7]	W23	GPIO0_C[7]	flash_data15			I/O	8	Down⑥	I	
GPIO3_A[2]	T19	GPIO3_A[2]	sdmmc0_clkout			I/O	4	Down⑥	I	VCCIO0
GPIO3_A[3]	T18	GPIO3_A[3]	sdmmc0_cmd			I/O	4	Up⑥	I	
GPIO3_A[4]	V20	GPIO3_A[4]	sdmmc0_data0			I/O	4	Up⑥	I	
GPIO3_A[5]	U22	GPIO3_A[5]	sdmmc0_data1			I/O	4	Up⑥	I	
GPIO3_A[6]	V22	GPIO3_A[6]	sdmmc0_data2			I/O	4	Up⑥	I	
GPIO3_A[7]	U20	GPIO3_A[7]	sdmmc0_data3			I/O	4	Up⑥	I	
GPIO0_D[4]	U23	GPIO0_D[4]	spi1_rxd			I/O	2	Down⑥	I	
GPIO0_D[5]	R21	GPIO0_D[5]	spi1_txd			I/O	2	Down⑥	I	
GPIO0_D[6]	T21	GPIO0_D[6]	spi1_clk			I/O	4	Down⑥	I	
GPIO0_D[7]	T20	GPIO0_D[7]	spi1_csn0			I/O	2	Down⑥	I	

GPIO1_B[2]	U21	GPIO1_B[2]	uart3_sin	gps_map		I/O	2	Up⑥	I	
GPIO1_B[3]	T22	GPIO1_B[3]	uart3_sout	gps_sig		I/O	2	Down⑥	I	
GPIO1_B[4]	T23	GPIO1_B[4]	uart3_cts_n	gps_rfclk		I/O	2	Up⑥	I	
GPIO1_B[5]	P21	GPIO1_B[5]	uart3_rts_n			I/O	2	Up⑥	I	
GPIO1_B[0]	P20	GPIO1_B[0]	jtag_tdi	jtag_tdi		I/O	2	Up⑥	I	
GPIO1_B[1]	P19	GPIO1_B[1]	jtag_tdo	jtag_tdo		I/O	2	Down⑥	I	
GPIO3_D[4]	R22	GPIO3_D[4]	pwm1	jtag_trstn		I/O	2	Down⑥	I	
GPIO3_D[5]	P22	GPIO3_D[5]	pwm2	jtag_tck	otg_drv_vbus	I/O	2	Up⑥	I	
GPIO3_D[6]	P23	GPIO3_D[6]	pwm3	jtag_tms	host_drv_vbus	I/O	2	Up⑥	I	
GPIO3_D[7]	N22	GPIO3_D[7]				I/O	2	Down⑥	I	
GPIO3_D[3]	N23	GPIO3_D[3]	pwm0			I/O	2	Down⑥	I	
GPIO1_B[6]	N20	GPIO1_B[6]	spdif_tx	spi1_csn1		I/O	2	Down⑥	I	
GPIO3_A[0]	N19	GPIO3_A[0]				I/O	2	Up⑥	I	
GPIO3_A[1]	N21	GPIO3_A[1]				I/O	2	Down⑥	I	
GPIO3_B[0]	M21	GPIO3_B[0]				I/O	2	Up⑥	I	
GPIO3_B[1]	M22	GPIO3_B[1]				I/O	2	Down⑥	I	
GPIO1_A[0]	L20	GPIO1_A[0]	uart0_sin			I/O	2	Up⑥	I	AP0_VCC
GPIO1_A[1]	L19	GPIO1_A[1]	uart0_sout			I/O	2	Down⑥	I	
GPIO1_A[2]	L21	GPIO1_A[2]	uart_cts_n			I/O	2	Up⑥	I	
GPIO1_A[3]	L23	GPIO1_A[3]	uart0_rts_n			I/O	2	Up⑥	I	
GPIO3_C[0]	L22	GPIO3_C[0]	sdmmc1_cmd	rmiitx_en		I/O	4	Up⑥	I	
GPIO3_C[1]	K22	GPIO3_C[1]	sdmmc1_data0	rmii_txd1		I/O	4	Up⑥	I	
GPIO3_C[2]	K23	GPIO3_C[2]	sdmmc1_data1	rmii_rxd0		I/O	4	Up⑥	I	
GPIO3_C[4]	K20	GPIO3_C[4]	sdmmc1_data3	rmii_rxd1		I/O	4	Up⑥	I	
GPIO3_C[5]	K21	GPIO3_C[5]	sdmmc1_clkout	rmii_clkout	rmii_clkin	I/O	4	Down⑥	I	
GPIO3_C[6]	J21	GPIO3_C[6]	sdmmc1_detect_n	rmii_rx_err		I/O	2	Down⑥	I	
GPIO3_C[7]	J22	GPIO3_C[7]	sdmmc1_write_prt	rmii_crs_dvalid		I/O	2	Down⑥	I	
GPIO3_D[0]	G23	GPIO3_D[0]	sdmmc1_pwr_en	mii_md		I/O	2	Down⑥	I	
GPIO3_D[1]	H22	GPIO3_D[1]	sdmmc1_backend_pwr	mii_mdclk		I/O	2	Down⑥	I	
GPIO3_D[2]	H23	GPIO3_D[2]	sdmmc1_int_n			I/O	2	Down⑥	I	
GPIO3_C[3]	K19	GPIO3_C[3]				I/O	4	Up⑥	I	
DVDD_SARADC	K18	1.8V				P		N/A	NA	ADCVDD_1V8
VDDA_SARADC	K18	1.8V				AP		N/A	NA	
SARADC_AIN[2]	H19	SARADC_AIN[2]	sdmmc0_cmd			A		N/A	NA	
SARADC_AIN[1]	H20	SARADC_AIN[1]				A		N/A	NA	
SARADC_AIN[0]	H21	SARADC_AIN[0]				A		N/A	NA	
GPIO1_D[0]	G22	GPIO1_D[0]	I2c0_sda			I/O	2	Up⑥	I	VCCIO1
GPIO1_D[1]	G21	GPIO1_D[1]	I2c0_scl			I/O	2	Up⑥	I	
GPIO1_D[2]	G20	GPIO1_D[2]	I2c1_sda			I/O	2	Up⑥	I	
GPIO1_D[3]	G19	GPIO1_D[3]	I2c1_scl			I/O	2	Up⑥	I	
GPIO1_D[4]	F21	GPIO1_D[4]	I2c2_sda			I/O	2	Up⑥	I	
GPIO1_D[5]	E20	GPIO1_D[5]	I2c2_scl			I/O	2	Up⑥	I	
GPIO2_D[7]	F22	GPIO2_D[7]	test_clock_out			I/O	8	Down⑥	I	
GPIO3_B[2]	F20	GPIO3_B[2]				I/O	2	Down⑥	I	
JTAGSEL	F19	JTAGSEL				I/O	2	down	I	

DDR_DQ[7]	E23	DDR_DQ[7]				I/O		N/A	I	
DDR_DQ[6]	D23	DDR_DQ[6]				I/O		N/A	I	
DDR_DQ[5]	B23	DDR_DQ[5]				I/O		N/A	I	
DDR_DQ[4]	A23	DDR_DQ[4]				I/O		N/A	I	
DDR_DQS[0]	B22	DDR_DQS[0]				I/O		N/A	I	
DDR_DQS_B[0]	A22	DDR_DQS_B[0]				I/O		N/A	I	
DDR_DQ[3]	D22	DDR_DQ[3]				I/O		N/A	I	
DDR_DQ[2]	C22	DDR_DQ[2]				I/O		N/A	I	
DDR_DQ[1]	D21	DDR_DQ[1]				I/O		N/A	I	
DDR_DQ[0]	E22	DDR_DQ[0]				I/O		N/A	I	MVDD
DDR_DM[0]	D20	DDR_DM[0]				I/O		N/A	I	
DDR_VREF[0]	G13	DDR_VREF[0]				P		N/A	NA	
DDR_DQ[23]	B21	DDR_DQ[23]				I/O		N/A	I	
DDR_DQ[22]	B20	DDR_DQ[22]				I/O		N/A	I	
DDR_DQ[21]	B18	DDR_DQ[21]				I/O		N/A	I	
DDR_DQ[20]	C19	DDR_DQ[20]				I/O		N/A	I	
DDR_DQS[2]	B19	DDR_DQS[2]				I/O		N/A	I	
DDR_DQS_B[2]	A19	DDR_DQS_B[2]				I/O		N/A	I	
DDR_DQ[19]	A20	DDR_DQ[19]				I/O		N/A	I	
DDR_DQ[18]	A17	DDR_DQ[18]				I/O		N/A	I	
DDR_DQ[17]	B17	DDR_DQ[17]				I/O		N/A	I	
DDR_DQ[16]	C18	DDR_DQ[16]				I/O		N/A	I	
DDR_DM[2]	C20	DDR_DM[2]				I/O		N/A	I	
DDR_PZQ	G15	DDR_PZQ				I/O		N/A	I	
DDR_ODT[1]	C17	DDR_ODT[1]				O		N/A	O	
DDR_ODT[0]	D17	DDR_ODT[0]				O		N/A	O	
DDR_ADDR[15]	A16	DDR_ADDR[15]				O		N/A	O	
DDR_CMD_VREF_1	G13	DDR_CMD_VREF_1				P		N/A	NA	
DDR_ADDR[14]	B16	DDR_ADDR[14]				O		N/A	O	
DDR_ADDR[13]	C16	DDR_ADDR[13]				O		N/A	O	
DDR_ADDR[12]	D18	DDR_ADDR[12]				O		N/A	O	
DDR_ADDR[11]	B15	DDR_ADDR[11]				O		N/A	O	
DDR_ADDR[10]	C15	DDR_ADDR[10]				O		N/A	O	
DDR_ADDR[9]	E14	DDR_ADDR[9]				O		N/A	O	
DDR_ADDR[8]	D14	DDR_ADDR[8]				O		N/A	O	
DDR_ADDR[7]	C14	DDR_ADDR[7]				O		N/A	O	
DDR_ADDR[6]	B14	DDR_ADDR[6]				O		N/A	O	
DDR_ADDR[5]	A14	DDR_ADDR[5]				O		N/A	O	
DDR_CK	B13	DDR_CK				O		N/A	O	
DDR_CK_N	A13	DDR_CK_N				O		N/A	O	
DDR_ADDR[4]	C13	DDR_ADDR[4]				O		N/A	O	
DDR_ADDR[3]	E13	DDR_ADDR[3]				O		N/A	O	
DDR_ADDR[2]	B12	DDR_ADDR[2]				O		N/A	O	
DDR_ADDR[1]	C12	DDR_ADDR[1]				O		N/A	O	
DDR_ADDR[0]	A11	DDR_ADDR[0]				O		N/A	O	
DDR_BA[2]	B11	DDR_BA[2]				O		N/A	O	

DDR_BA[1]	C11	DDR_BA[1]				O		N/A	O	
DDR_BA[0]	D11	DDR_BA[0]				O		N/A	O	
DDR_RASN	A10	DDR_RASN				O		N/A	O	
DDR_CASN	B10	DDR_CASN				O		N/A	O	
DDR_WEN	C10	DDR_WEN				O		N/A	O	
DDR_CSN[1]	B9	DDR_CSN[1]				O		N/A	O	
DDR_CSN[0]	A8	DDR_CSN[0]				O		N/A	O	
DDR_CKE1	B8	DDR_CKE1				O		N/A	O	
DDR_CKE0	C9	DDR_CKE0				O		N/A	O	
DDR_RESET	E11	DDR_RESET				O		N/A	O	
DDR_ISO_VREF_0	G12	DDR_ISO_VREF_0				P		N/A	NA	
DDR_DQ[15]	C8	DDR_DQ[15]				I/O		N/A	I	
DDR_DQ[14]	D8	DDR_DQ[14]				I/O		N/A	I	
DDR_DQ[13]	E8	DDR_DQ[13]				I/O		N/A	I	
DDR_DQ[12]	C7	DDR_DQ[12]				I/O		N/A	I	
DDR_DQS[1]	B7	DDR_DQS[1]				I/O		N/A	I	
DDR_DQS_B[1]	A7	DDR_DQS_B[1]				I/O		N/A	I	
DDR_DQ[11]	E7	DDR_DQ[11]				I/O		N/A	I	
DDR_DQ[10]	B6	DDR_DQ[10]				I/O		N/A	I	
DDR_DQ[9]	C6	DDR_DQ[9]				I/O		N/A	I	
DDR_DQ[8]	D6	DDR_DQ[8]				I/O		N/A	I	
DDR_DM[1]	E6	DDR_DM[1]				I/O		N/A	I	
DDR_VREF[1]	G13	DDR_VREF[1]				P		N/A	I	
DDR_DQ[31]	A5	DDR_DQ[31]				I/O		N/A	I	
DDR_DQ[30]	B5	DDR_DQ[30]				I/O		N/A	I	
DDR_DQ[29]	C5	DDR_DQ[29]				I/O		N/A	I	
DDR_DQ[28]	D5	DDR_DQ[28]				I/O		N/A	I	
DDR_DQS[3]	B4	DDR_DQS[3]				I/O		N/A	I	
DDR_DQS_B[3]	A4	DDR_DQS_B[3]				I/O		N/A	I	
DDR_DQ[27]	C4	DDR_DQ[27]				I/O		N/A	I	
DDR_DQ[26]	C3	DDR_DQ[26]				I/O		N/A	I	
DDR_DQ[25]	B3	DDR_DQ[25]				I/O		N/A	I	
DDR_DQ[24]	B2	DDR_DQ[24]				I/O		N/A	I	
DDR_DM[3]	A2	DDR_DM[3]				I/O		N/A	I	
LCDC0_HSYNC	A1	LCDC0_HSYNC				O	8	N/A	O	
LCDC0_VSYNC	B1	LCDC0_VSYNC				O	8	N/A	O	
LCDC0_DCLK	D2	LCDC0_DCLK				O	12	N/A	O	
LCDC0_DEN	D3	LCDC0_DEN				O	8	N/A	O	
LCDC0_DATA[0]	D1	LCDC0_DATA[0]				O	8	N/A	O	
LCDC0_DATA[1]	E1	LCDC0_DATA[1]				O	8	N/A	O	
LCDC0_DATA[2]	E2	LCDC0_DATA[2]				O	8	N/A	O	
LCDC0_DATA[3]	E3	LCDC0_DATA[3]				O	8	N/A	O	
LCDC0_DATA[4]	E4	LCDC0_DATA[4]				O	8	N/A	O	
LCDC0_DATA[5]	G6	LCDC0_DATA[5]				O	8	N/A	O	
LCDC0_DATA[6]	F5	LCDC0_DATA[6]				O	8	N/A	O	

LCDC0_VC C0

Notes :

①: *Pad types : I = input , O = output , I/O = input/output (bidirectional) ,*
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: *Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value*

③: *Reset state: I = input without any pull resistor O = output*

④: *It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

⑤: *Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring*

⑥ *The pull up/pull down is configurable.*

2.6 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK3188T IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	CLK32K	I	Clock input of 32.768KHz
	CPU_PWROFF	O	Request signal to external PMIC for power down CPU subsystem with dual-core Cortex-A9
	CORE_PWROFF	O	Request signal to external PMIC for SoC Core logic w/o Cortex-A9 subsystem and PMU logic
	NPOR	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	JTAG_SEL	I	JTAG function select input
	TRST_N	I	JTAG interface reset input
	TCK	I	JTAG interface clock input/SWD interface clock input
	TDI	I	JTAG interface TDI input
	TMS	I/O	JTAG interface TMS input/SWD interface data out
	TDO	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
ETM Trace	trace_clk	O	Cortex-A9 ETM trace port clk
	trace_ctl	O	Cortex-A9 ETM trace port control
	trace_data*i*(*i*=0~15)	O	Cortex-A9 ETM trace port data

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_rstn_out	O	sdmmc card reset signal
	sdmmc_pwr_en	O	sdmmc card power-enable control signal

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.
	sdio_detect_n	I	sdio card detect signal, a 0 represents presence of card.
	sdio_write_prt	I	sdio card write protect signal, a 1 represents write is protected.
	sdio_pwr_en	O	sdio card power-enable control signal
	sdio_int_n	O	sdio card interrupt indication
	sdio_backend	O	the back-end power supply for embedded device

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_pwr_en	O	emmc card power-enable control signal
	emmc_rstn_out	O	emmc card reset signal

Interface	Pin Name	Direction	Description
DMC	CK	O	Active-high clock signal to the memory device.
	CK_B	O	Active-low clock signal to the memory device.
	CKE*i* (*i*=0,1)	O	Active-high clock enable signal to the memory device for two chip select.
	CS_B*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RAS_B	O	Active-low row address strobe to the memory device.

	CAS_B	O	Active-low column address strobe to the memory device.
	WE_B	O	Active-low write enable strobe to the memory device.
	BA[2:0]	O	Bank address signal to the memory device.
	A[15:0]	O	Address signal to the memory device.
	DQ[31:0]	I/O	Bidirectional data line to the memory device.
	DQS[3:0]	I/O	Active-high bidirectional data strobes to the memory device.
	DQS_B[3:0]	I/O	Active-low bidirectional data strobes to the memory device.
	DM[3:0]	O	Active-low data mask signal to the memory device.
	ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select.
	RET_EN	I	Active-low retention latch enable input
	RESET	O	DDR3 reset signal to the memory device
	VREF*i* (*i*=0,1,2,3)	I/O	Reference Voltage input for three regions of DDR IO
	ZQ_PIN	I/O	ZQ calibration pad which connects 240ohm±1% resistor

Interface	Pin Name	Direction	Description
SMC	smc_oe_n	O	SMC output enable signal.
	smc_bls_n*i* (*i*=0,1)	O	SMC byte lane strobe signal for two bytes.
	smc_we_n	O	SMC write enable signal.
	smc_csn*i* (*i*=0,1)	O	SMC chip enable signal.
	smc_adv_n	O	SMC address valid signal in shared mode
	smc_addr*i* (*i*=0~7)	O	SMC address signal.
	smc_data*i* (*i*=0~15)	I/O	SMC directional data line to memory device.

Interface	Pin Name	Direction	Description
NandC	FLASH_WP	O	Flash write-protected signal
	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_DATA[*i*](*i*=0~7)	I/O	Low 8bits of flash data inputs/outputs signal
	flash_data*i*(*i*=8~15)	I/O	High 8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH0_CSN	O	Flash chip enable signal for chip 0
	flash_csn*i*(*i*=1~3)	O	Flash chip enable signal for chip i, i=1~3

Interface	Pin Name	Direction	Description
HSADC Interface	hsadc_clkout	O	hsadc/tsi/gps reference clock
	hsadc_data*i* (*i*=0~9)	I	hsadc(i=0~9)/tsi(i=0~7)/gps data(i=0,1)
	ts_sync	I	ts synchronizer signal

Interface	Pin Name	Direction	Description
I2S/PCM Controller (2 channel)	i2s_clk	O	I2S/PCM1 clock source
	i2s_sclk	I/O	I2S/PCM1 serial clock
	i2s_lrck_rx	I/O	I2S/PCM1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM1 serial data input
	i2s_sdo	O	I2S/PCM1 serial data ouput
	i2s_lrck_tx	I/O	I2S/PCM1 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPDIF transmitter	spdif_tx	O	spdif biphase data ouput

Interface	Pin Name	Direction	Description
SPI Controller	spi*x*_clk*(x=0,1)*	I/O	spi serial clock
	spi*x*_csn*y* *(x=0,1)(y=0,1)*	I/O	spi chip select signal,low active
	spi*x*_txd*(x=0,1)*	O	spi serial data output
	spi*x*_rxd*(x=0,1)*	I	spi serial data input

Interface	Pin Name	Direction	Description
LCDC0	LCDC0_DCLK	O	LCDC0 RGB interface display clock out, MCU i80 interface RS signal
	LCDC0_VSYNC	O	LCDC0 RGB interface vertival sync pulse, MCU i80 interface CSN signal
	LCDC0_HSYNC	O	LCDC0 RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	LCDC0_DEN	O	LCDC0 RGB interface data enable, MCU i80 interface REN signal
	LCDC0_DATA[23:0]	I/O	LCDC0 data output/input

Interface	Pin Name	Direction	Description
LCDC1	lcdc1_dclk	O	LCDC1 RGB interface display clock out, MCU i80 interface RS signal

	lcdc1_vsync	O	LCDC1 RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc1_hsync	O	LCDC1 RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc1_den	O	LCDC1 RGB interface data enable, MCU i80 interface REN signal
	lcdc1_data[23:0]	I/O	LCDC1 data output/input

Interface	Pin Name	Direction	Description
Camera IF	CIF_CLKIN	I	Camera0 interface input pixel clock
	cif_clkout	O	Camera0 interface output work clock
	CIF_VSYNC	I	Camera0 interface vertical sync signal
	CIF_HREF	I	Camera0 interface horizontial sync signal
	cif_data[1:0]	I	Camera0 interface low 2-bit input pixel data
	CIF_DATAIN[9:2]	I	Camera0 interface middle low 8-bit input pixel data
	cif_data[11:10]	I	Camera0 interface middle high 2-bit input pixel data
	CIF_DATA_15_12 [15:12]	I	Camera0 interface high 4-bit input pixel data

Interface	Pin Name	Direction	Description
RMII	rmii_clkout	O	RMII REC_CLK output
	rmii_clkin	I	RMII REF_CLK input
	rmii_tx_en	O	rmii transfer enable
	rmii_txd1	O	rmii transfer data
	rmii_txd0	O	rmii transfer data
	rmii_rx_err	I	rmii receive error
	rmii_crs_dvalid	I	rmii carrier sense / receive data valid input
	rmii_rxd1	I	rmii receive data
	rmii_rxd0	I	rmii receive data
	mii_md	I/O	mii management interface data
	mii_mdclk	O	mii management interface clock

Interface	Pin Name	Direction	Description
PWM	pwm3	O	Pulse Width Modulation output
	pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
GPS	gps_rfclk	I	GPS reference clock
	gps_sig	I	GPS SIG input

	gps_mag	I	GPS MAG input

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock
	i2c4_sda	I/O	I2C4 data
	i2c4_scl	I/O	I2C4 clock

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output
	uart3_sin	I	UART3 searial data input
	uart3_sout	O	UART3 searial data output
	uart3_cts_n	I	UART3 clear to send
	uart3_rts_n	O	UART3 request to send

Interface	Pin Name	Direction	Description
USB OTG 2.0	OTG_DM	N/A	USB OTG 2.0 Data signal DM
	OTG_RKELVIN	N/A	USB OTG 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	OTG_DP	N/A	USB OTG 2.0 Data signal DP
	OTG_VBUS	N/A	USB OTG 2.0 5-V power supply pin
	otg_drv_vbus	O	USB OTG 2.0 drive VBUS

Interface	Pin Name	Direction	Description
USB Host 2.0	HOST_DM	N/A	USB HOST 2.0 Data signal DM
	HOST_RKELVIN	N/A	USB HOST 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	HOST_DP	N/A	USB HOST 2.0 Data signal DP

	HOST_VBUS	N/A	USB HOST 2.0 5-V power supply pin
	host_drv_vbus	O	USB HOST 2.0 drive VBUS

Interface	Pin Name	Direction	Description
HSIC	HSIC_DATA	N/A	HSIC DATA signal
	HSIC_STROBE	N/A	HSIC STROBE signal

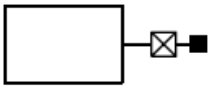
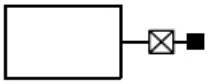
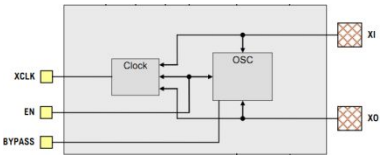
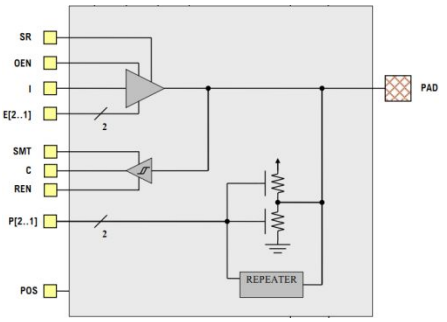
Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN[i] (i=0~2)	N/A	SAR-ADC input signal for 3 channel

Interface	Pin Name	Direction	Description
eFuse	EFUSE_VDDQ	N/A	eFuse program and sense power

2.7 RK3188T IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 2-5 RK3188T IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		Tri-state output pad with input, which pullup/pulldown, slew rate and drive strength is configurable	Part of digital GPIO

Chapter 3 Electrical Specification

3.1Absolute Maximum Ratings

Table 3-1 RK3188T absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD, CVDD, PVDD, USBDVDD	1.4	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	LCD0_VCC0,LCD0_VCC1, LCD1_VCC, CIF_VCC PVCC_3V3, AP0_VCC,AP1_VCC, FLASH_VCC, VCCIO0,VCCIO1	3.6	V
DC supply voltage for DDR IO	MVDD	1.95	V
DC supply voltage for Analog part of SAR-ADC	ADCVDD_1V8	1.98	V
DC supply voltage for Analog part of PLL	APLL_1V0 CGPLL_1V0 DPLL_1V0	1.3	V
DC supply voltage for Analog part of USB OTG/Host2.0	USBVDD_1V8 USBVDD_3V3	1.98 3.63	V
Analog Input voltage for SAR-ADC	ADCVDD_1V8	1.98	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.1 Recommended Operating Conditions

Table 1-7 describes the recommended operating condition for every clock domain.

Table 3-2 RK3188T recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power （except USB OTG)	AVDD, CVDD, PVDD	0.9	1.0	TBD	V
Digital GPIO Power(3.3V/2.5V/1.8V)	VCCIO0,VCCIO1,	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V

Digital GPIO Power(3.3V/2.5V/1.8V)	LCD0_VCC0, LCD0_VCC1, LCD1_VCC, CIF_VCC, PVCC, FLASH_VCC, AP0_VCC, AP1_VCC	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
DDR IO (DDR3 mode) Power	MVDD	1.425	1.5	1.575	V
DDR IO (LPDDR2 mode) Power	MVDD	1.14	1.2	1.3	V
DDR reference supply (VREF) Input	VREF	0.49*MVDD	0.5*MVDD	0.51*MVDD	V
DDR External termination voltage		VREF- 40mV	VREF	VREFi+ 40mV	V
PLL Analog Power	APLL_1V0 CGPLL_1V0 DPLL_1V0	0.9	1.0	1.1	V
SAR-ADC Analog Power	ADCVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USBDVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(1.8V)	USBVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Analog Power(3.3V)	USBVDD_3V3	3.069	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	NA	200	NA	Ohm
HSIC Analog Power	USBDVDD_1V0	1.1	1	0.9	
PLL input clock frequency		N/A	24	N/A	MHz
Max CPU frequency			1.4		GHz
Operating Temperature	Tj	-40	25	125	℃

3.2 DC Characteristics

Table 3-3 RK3188T DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm

DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.09	NA	MVDD	V
	Input Low Voltage	Vil_ddr	-0.3	0	VREF - 0.09	V
	Output High Voltage	Voh_ddr	0.8xMVDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.2*MVDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	MVDD	V
	Input Low Voltage	Vil_ddr	-0.3	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	0.9*VREF	NA	NA	V
	Output Low Voltage	Vol_ddr	NA	NA	0.1*VREF	V

3.3 Recommended Operating Frequency

Table 3-4 Recommended operating frequency for PD_ALIVE domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.0V , 25 ℃	IO_XIN24M	24	24	24	MHz
	1.1V , -40 ℃		24	24	24	
	0.9V , 125 ℃		24	24	24	
DDR PLL	1.0V , 25 ℃	ddr_pll_clk	N/A	N/A	1238	MHz
	1.1V , -40 ℃		N/A	N/A	1346	
	0.9V , 125 ℃		N/A	N/A	1118	
ARM PLL	1.0V , 25 ℃	arm_pll_clk	N/A	N/A	1598	MHz
	1.1V , -40 ℃		N/A	N/A	2161	
	0.9V , 125 ℃		N/A	N/A	1165	
CODEC PLL	1.0V , 25 ℃	cocec_pll_clk	N/A	N/A	1170	MHz
	1.1V , -40 ℃		N/A	N/A	1647	
	0.9V , 125 ℃		N/A	N/A	831	
GENERAL PLL	1.0V , 25 ℃	general_pll_clk	N/A	N/A	1341	MHz
	1.1V , -40 ℃		N/A	N/A	1784	
	0.9V , 125 ℃		N/A	N/A	963	
UART1CLK	1.0V , 25 ℃	clk_uart1	N/A	N/A	50	MHz
	1.1V , -40 ℃		N/A	N/A	50	
	0.9V , 125 ℃		N/A	N/A	50	
TIMER3 CLK	1.0V , 25 ℃	clk_timer3	N/A	N/A	24	MHz
	1.1V , -40 ℃		N/A	N/A	24	
	0.9V , 125 ℃		N/A	N/A	24	

3.4 Electrical Characteristics for General IO

Table 3-5 RK3188T Electrical Characteristics for Digital General IO

Parameters	Symbol	Test condition	Min	Typ	Max	Units

Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-6 RK3188T Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency	Fin	Fin = Fref * NR① @1.0V	0.032	NA	2200	MHz
	Comparison frequency	Fref	Fref = Fin/NR@1.0V	0.032	N/A	50	MHz
	VCO operating range	Fvco	Fvco = Fref * NF① @1.0V	1100	N/A	2200	MHz
	Output clock frequency	Fout	Fout = Fvco/NO① @1.0V	30	N/A	2200	MHz
	Lock time	Tlt		N/A	350	500	Cycles of divided reference clock
	Power consumption (normal mode)	N/A		N/A	4	N/A	mW
	Power consumption (standby mode)	N/A		N/A	100	N/A	uW
	Power consumption (power-down mode)	N/A	No clock input to PLL power down signal high, 80C temperature	N/A	10	N/A	uW

Notes : ①. *NR is the input divider value;*
NF is the feedback divider value;
NO is the output divider value

3.6 Electrical Characteristics for SAR-ADC

Table 3-7 RK3188T Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Conversion speed	Fs	The duty cycle should be between 40%~60%	NA	N/A	1	MSPS
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Nn Linearity	INL		N/A	±2	N/A	LSB
Gain Error	Egain		-8	N/A	8	LSB
Offset Error	Eoffset		-8	N/A	8	mV
Analog Supply Current(VDDA_SARADC)			N/A	200	N/A	uA
Digital Supply Current			N/A	50	N/A	uA
Power Down Current from AVDD			NA	0.5	NA	uA
Power Down Current from DVDD			N/A	1	N/A	uA
Power up time			N/A	7	N/A	1/Fs

3.7 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 3-8 RK3188T Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters		Symbol	Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		55℃, USBDVDD_1V0 = 1.0V USBVDD_1V8=1.0V USBVDD_3V3=3.3V, 15-cm USB cable attached to DP/DM	N/A	6.151	N/A	mA
	Current From OTG_VDD33			N/A	4.97	N/A	mA
	Current From OTG_VDD18			N/A	18.5	N/A	mA
HS transmit, minimum transition density (all 1's data in DP/DM)	Current From OTG_DVDD			N/A	5.521	N/A	mA
	Current From OTG_VDD33			N/A	3.63	N/A	mA
	Current From OTG_VDD18			N/A	15.5	N/A	mA
HS idle mode	Current From OTG_DVDD			N/A	5.841	N/A	mA
	Current From OTG_VDD33			N/A	3.19	N/A	mA
	Current From OTG_VDD18			N/A	6.58	N/A	mA
FS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD			N/A	4.251	N/A	mA
	Current From OTG_VDD33			N/A	11.81	N/A	mA
	Current From OTG_VDD18			N/A	6.56	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD			N/A	5.171	N/A	mA
	Current From OTG_VDD33			N/A	12.81	N/A	mA
	Current From OTG_VDD18			N/A	6.61	N/A	mA
Suspend mode	Current From OTG_DVDD			N/A	53.4	N/A	uA
	Current From OTG_VDD33			N/A	1.1	N/A	uA
	Current From OTG_VDD18			N/A	6.6	N/A	uA
Sleep mode	Current From OTG_DVDD			N/A	0.113	N/A	mA

	Current From OTG_VDD33			N/A	0.1	N/A	uA
	Current From OTG_VDD18			N/A	0.004	N/A	mA

3.8 Electrical Characteristics for HSIC Interface

Table 3-9 RK3188T Electrical Characteristics for HSIC Interface

Parameters		Symbol	Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density	Current From DVDD		55℃ , VDD12 = 1.2V, DVDD = 1.0V , 12MHz reference clock 10pF load on STROBE	N/A	3.26	N/A	mA
	Current From VDD12			N/A	10.20	N/A	mA
HS transmit, minimum transition density	Current From DVDD			N/A	3.05	N/A	mA
	Current From VDD12			N/A	8.28	N/A	mA
HS idle mode	Current From DVDD			N/A	2.71	N/A	mA
	Current From VDD12			N/A	0.001	N/A	mA
HS Receive	Current From DVDD			N/A	3.07	N/A	mA
	Current From VDD12			N/A	1.58	N/A	mA
Suspend mode	Current From DVDD			N/A	0.012	N/A	mA
	Current From VDD12			N/A	0.3	N/A	uA
Sleep mode	Current From DVDD			N/A	0.049	N/A	mA
	Current From VDD12			N/A	0.6	N/A	uA

3.9 Electrical Characteristics for DDR IO

Table 3-10 RK3188T Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	VDDIO_DDR standby current, ODT OFF		@ 1.5V , 125℃	NA	0.01	2.11	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0	0.53	uA
DDR IO @LPDDR2 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA
	VDD(1.2V) quiescent current		@ 1.2V , 125℃	NA	0	1.89	uA

3.10 Electrical Characteristics for eFuse

Table 3-11 RK3188T Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	NA	NA	8	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	NA	NA	0.2	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	NA	NA	14	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	NA	NA	60	uA

Chapter 4 Timing Specification

4.1 DDR Timing Diagram

DDR3 Read/Write Access Timing

Fig. 4-1 DDR3 burst write operation: AL=0,CWL=4, BC4

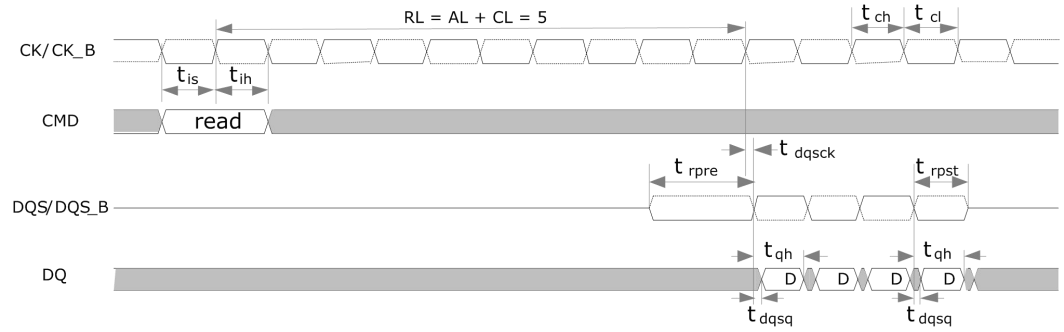


Fig. 4-2 DDR3 burst read operation: AL=0,CL=5, BC4

Table 4-1 meaning of the parameter

Parameter		Min.	Typ.	Max.	Unit
t_{ch}	CK HIGH pulse width	0.43	-	-	tCK
t_{cl}	CK LOW pulse width	0.43	-	-	tCK
t_{ds}	DQ and DM input setup time (differential strobe)	25	-	-	ps
t_{dh}	DQ and DM input hold time (differential strobe)	100	-	-	ps
t_{dss}	DQS falling edge to CK setup time	0.2	-	-	tCK
t_{dsh}	DQS falling edge hold time from CK	0.2	-	-	tCK
t_{is}	Address and control input setup time	125	-	-	ps
t_{ih}	Address and control input hold time	200	-	-	ps
t_{wpre}	Write preamble	0.9	-	-	tCK
t_{wpst}	Write postamble	0.3	-	-	tCK
t_{rpre}	Read preamble	0.9	-	1.1	tCK
t_{rpst}	Read postamble	0.3	-	0.5	tCK
t_{dqsck}	DQS output access time from CK/CK_n	-300	-	+300	ps
t_{dqsq}	DQS-DQ skew for DQS and associated DQ signals	-	-	150	ps
t_{qh}	DQ/DQS output hold time from DQS	0.38	-	-	tCK

Note： This table is for DDR3-900.

LPDDR2 Read/Write Access Timing

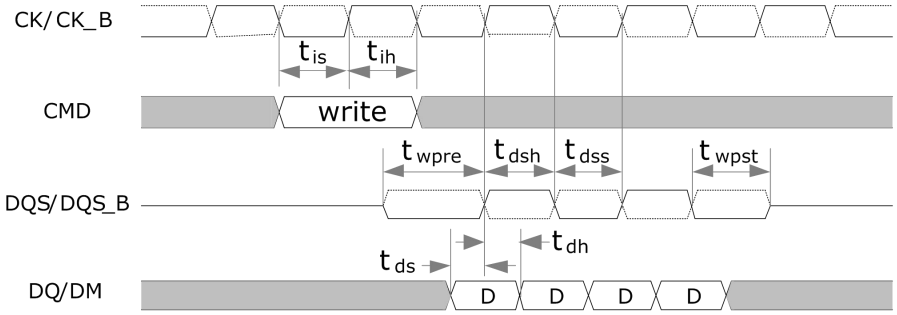


Fig. 4-3 LPDDR2 burst write operation: WL=1,BL=4

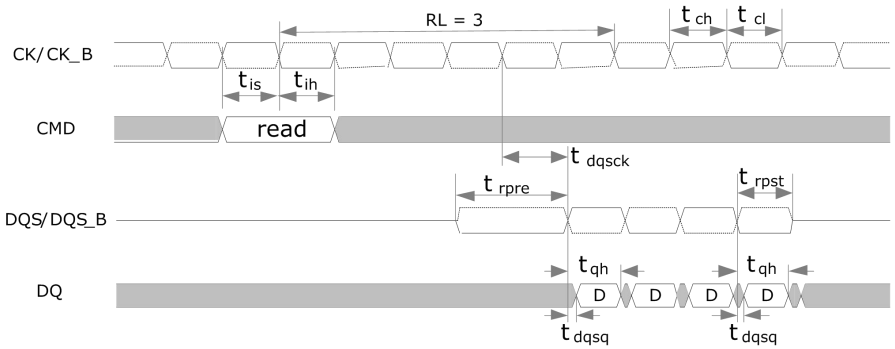


Fig. 4-4 LPDDR2 burst read operation: RL=3, BL=4

Table 4-2 meaning of the parameter

Parameter		Min.	Typ.	Max.	Unit
t_{ch}	CK HIGH pulse width	0.43	-	0.57	tCK
t_{cl}	CK LOW pulse width	0.43	-	0.57	tCK
t_{ds}	DQ and DM inputsetup time	0.21	-	-	ns
t_{dh}	DQ and DM input hold time	0.21	-	-	ns
t_{dss}	DQS falling edge to CK setup time	0.2	-	-	tCK
t_{dsh}	DQS falling edge hold time from CK	0.2	-	-	tCK
t_{is}	Address and control input setup time	0.22	-	-	ns
t_{ih}	Address and control input hold time	0.22	-	-	ns
t_{wpre}	Write preamble	0.35	-	-	tCK
t_{wpst}	Write postamble	0.4	-	-	tCK
t_{rpre}	Read preamble	0.9	-	-	tCK
t_{rpst}	Read postamble	t_{cl} -0.05	-	t_{cl} -0.05	tCK
t_{dqsck}	DQS output access time from CK/CK_n	2.5	-	5.5	ns
t_{dqsq}	DQS-DQ skew for DQS and associated DQ signals	-	-	0.2	ns
t_{qh}	DQ/DQS output hold time from DQS	t_{qhp}- t_{qhs}	-	-	ns
RL	Read Latency	8	-	-	tCK
WL	Write Latency	4	-	-	tCK

Note： This table is for LPDDR2 S4-900.

4.2 SMC Timing Diagram

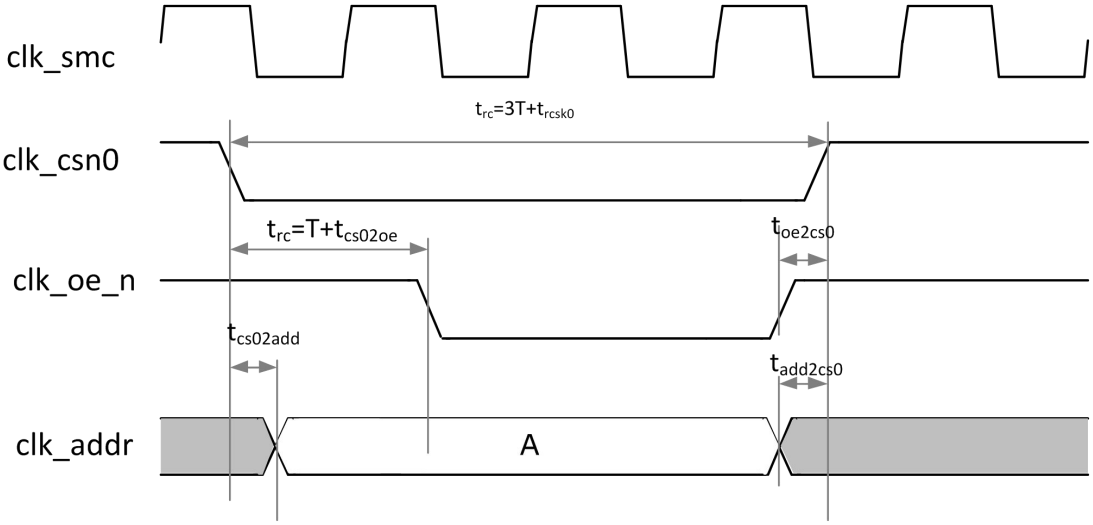


Fig. 4-5 SMC timing diagram of asynchronous read

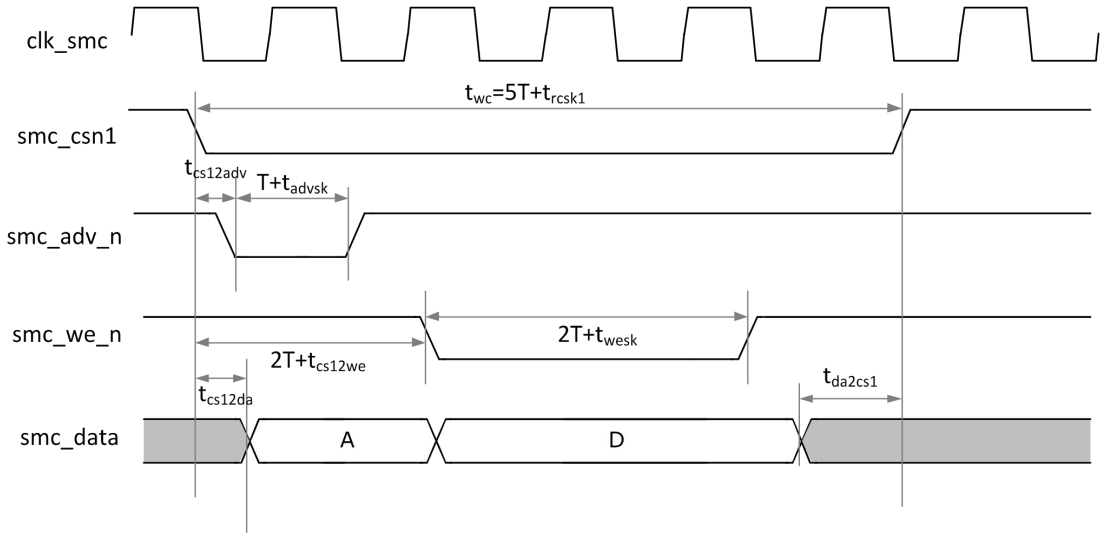


Fig. 4-6 Asynchronous Write Timing Diagram In Multiplexed Mode

Table 4-1 Meaning of The Parameter

*****timing condition: VCCIO=3.3V, $C_L \leqslant 8pF$, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{rcsk0}	Rise and fall skew for smc_csn0	-4	47	872	ps
t_{rcsk1}	Rise and fall skew for smc_csn1	77	117	-20	ps
t_{wesk}	Rise and fall skew for smc_we_n	-27	5	22	ps
t_{cs02oe}	smc_csn0 valid to smc_oe_n valid skew	46	93	157	ps
t_{cs12oe}	smc_csn1 valid to smc_oe_n valid skew	1004	1631	2631	ps
t_{oe2cs0}	smc_oe_n invalid to smc_csn0 invalid skew	-71	-124	-189	ps
t_{oe2cs1}	smc_oe_n invalid to smc_csn1 invalid skew	-1110	-1732	-2556	ps
$t_{cs02add}$	smc_csn0 valid to smc_addr valid skew	3	-33	22	ps
$t_{cs12add}$	smc_csn1 valid to smc_addr valid skew	961	1505	2496	ps
$t_{add2cs0}$	smc_addr invalid to smc_csn0 invalid skew	0	-14	-109	ps
$t_{add2cs1}$	smc_addr invalid to smc_csn1 invalid skew	-1038	-1622	-2476	ps
t_{cs02we}	smc_csn0 valid to smc_we_n valid skew	230	347	491	ps
t_{cs12we}	smc_csn1 valid to smc_we_n valid skew	1188	1886	2966	ps
t_{advsk}	Rise and fall skew for smc_adv_n	-27	12	31	ps
$t_{cs02adv}$	smc_csn0 valid to smc_adv_n valid skew	-96	-79	-112	ps
$t_{cs12adv}$	smc_csn1 valid to smc_adv_n valid skew	861	1459	2362	ps

t_{cs02da}	smc_csn0 valid to smc_data valid skew	-166	-258	-294	ps
t_{cs12da}	smc_csn1 valid to smc_data valid skew	791	1280	2179	ps
t_{da2cs0}	smc_data invalid to smc_csn0 invalid skew	170	210	207	ps
t_{da2cs1}	smc_data invalid to smc_csn1 invalid skew	-868	-1397	-2159	ps

4.3 Nandc Timing Diagram

Following figures show the flash timing diagram for different flash interface.

Parameters in red are flash characteristics determined by flash device.

Parameters in green are NandC characteristics determined by those parameters in red (FMWAIT_ASYN/FMWAIT_SYN).

The relationship between red parameters and green parameters for different flash interface is shown in following description.

Notes:

Tcsrw=FMWAIT_ASYN[17:12], trwpw=FMWAIT_ASYN[10:5], trwcs=FMWAIT_ASYN[4:0];

Tfclk=FMWAIT_SYN[2:0], tpre=FMWAIT_SYN[8:3], tpst=FMWAIT_SYN[14:9]

4.3.1 Asynchronous Interface

a. Asynchronous Address/Command Latch Cycle

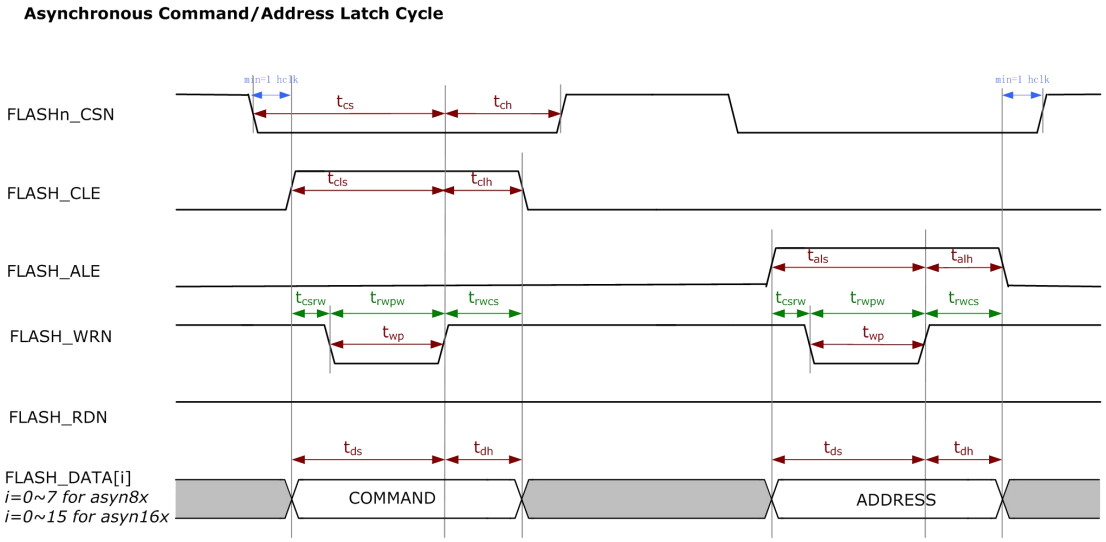


Fig. 4-7 NandC Asyn8x/16x Address/Command Latch Cycle

b. Asynchronous Data Input Cycles

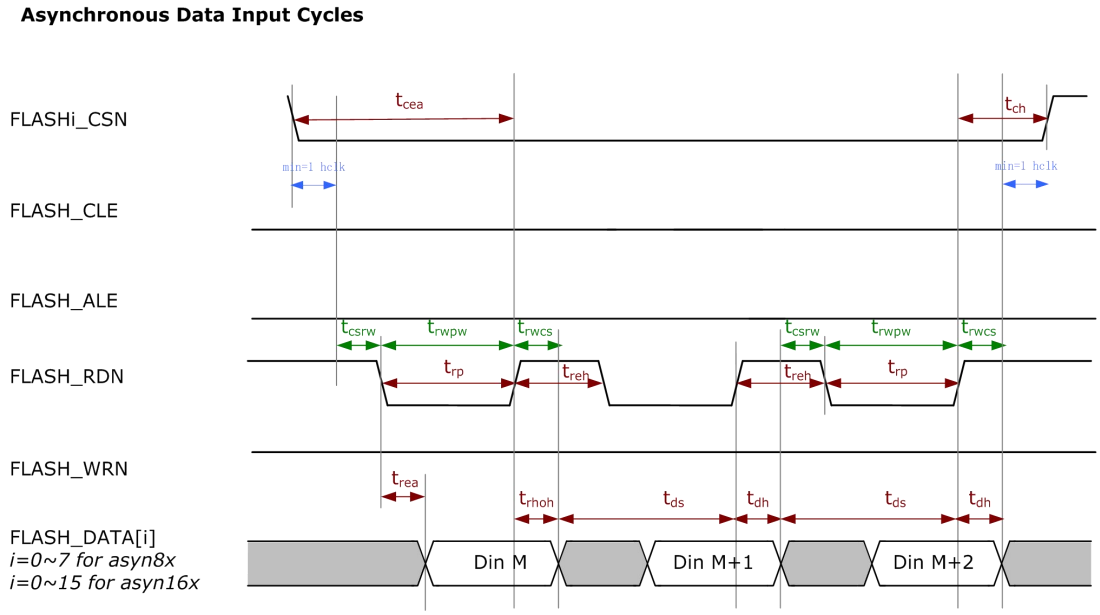


Fig. 4-8 NandC Asyn8x/16x Data Input Cycles

c. Asynchronous Data Output Cycles

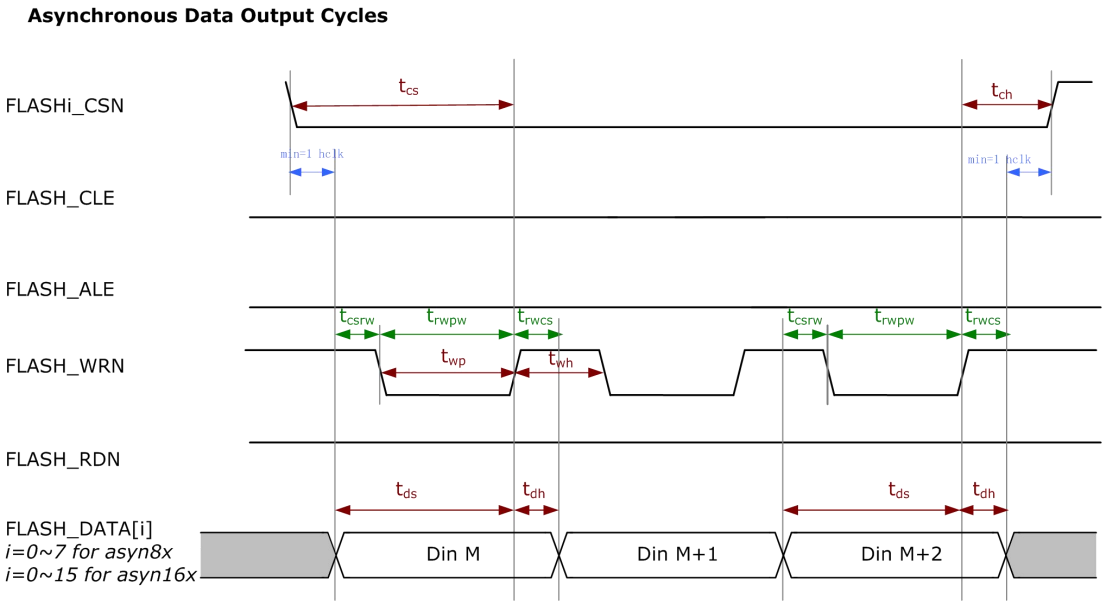


Fig. 4-9 NandC Asyn8x/16x Data Output Cycles

Table 4-3 NandC I/O Skew: Asyn8x/Asyn16x

*timing condition: VCCIO=3.3V, $C_L \leqslant 8pF$, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{wrn}	Chip latency for FLASH_WRN	3.3	4.8	7.0	ns
t_{rdn}	Chip latency for FLASH_RDN	3.3	4.8	7.0	ns
$t_{cle2wrn}$	Skew from FLASH_CLE to FLASH_WRN	-	-	0.1	ns
$t_{ale2wrn}$	Skew from FLASH_ALE to FLASH_WRN	-	-	0.4	ns
$t_{dqo2wrn}$	Skew from FLASH_DATA output(asyn8x/asyn16x) to FLASH_WRN	-	-	0.2	ns

t_{di}	Chip latency for FLASH_DATA input(asyn8x/asyn16x)	-	-	2.0/2.2	ns

4.3.2 ONFI Synchronous Interface

a. ONFI synchronous Address/Command Latch Cycle

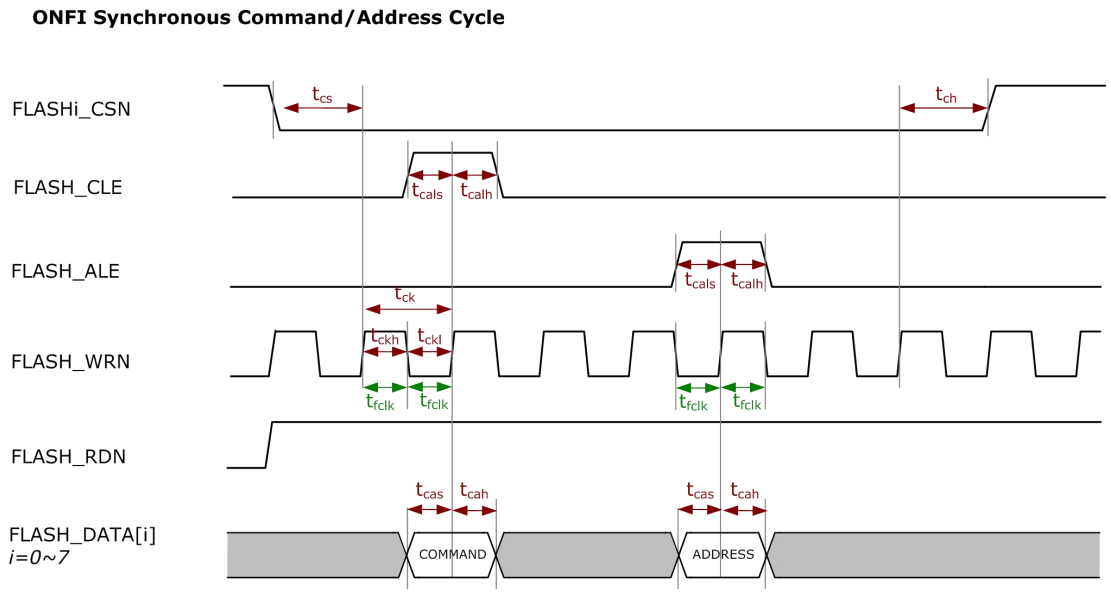


Fig. 4-10 NandC ONFI Syn Address/Command Latch Cycle

b. ONFI Synchronous Data Input Cycles

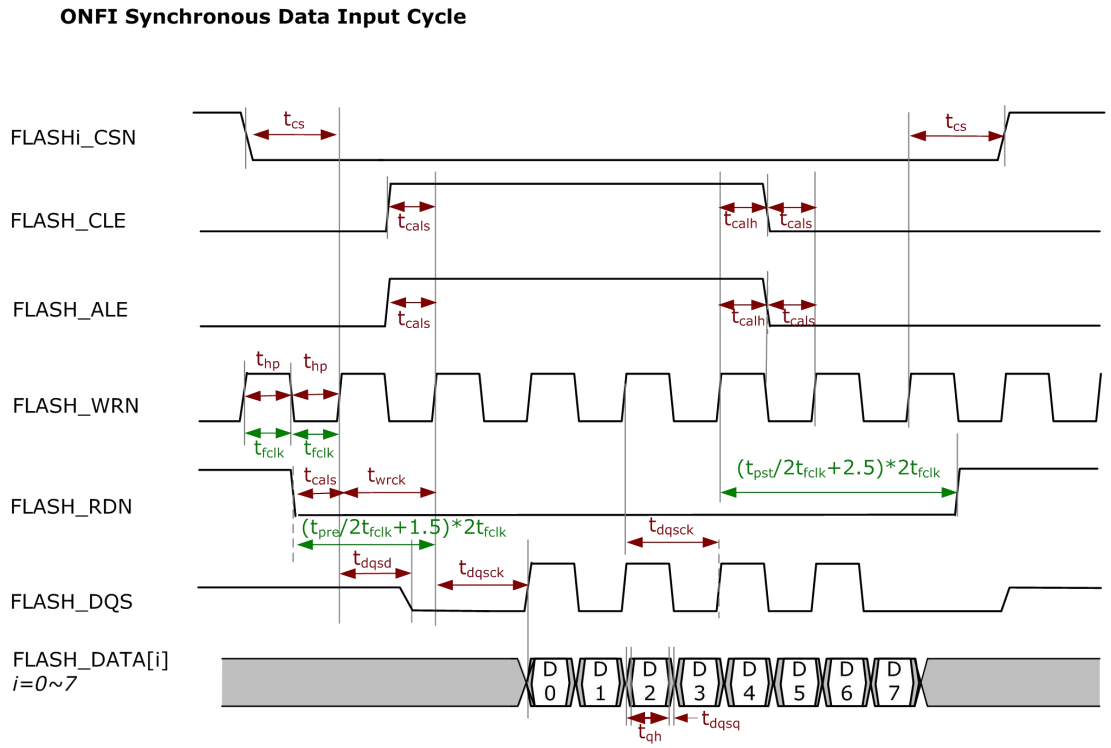


Fig. 4-11 NandC ONFI Synchronous Data Input Cycles

c. ONFI Synchronous Data Output Cycles

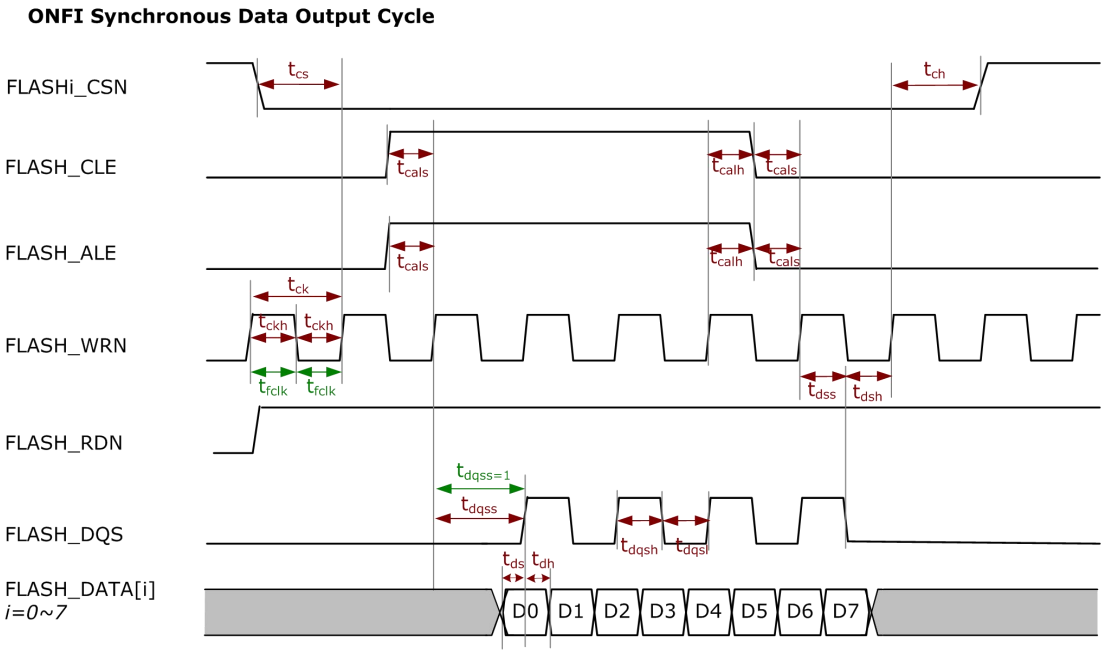


Fig. 4-12 NandC ONFI Syn Data Output Cycles

Table 4-4 NandC I/O Skew: ONFI Synchronous

*timing condition: VCCIO=1.8V, $C_L \leqslant 8pF$, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{wrn}	Chip latency for FLASH_WRN	3.5	5.0	7.2	ns
$t_{rdn2wrn}$	Skew from FLASH_RDN to FLASH_WRN	-0.2	-	-	ns
$t_{cle2wrn}$	Skew from FLASH_CLE to FLASH_WRN	-0.2	-	-	ns
$t_{ale2wrn}$	Skew from FLASH_ALE to FLASH_WRN	-0.2	-	-	ns
$t_{dqo2wrn}$	Skew from FLASH_DATA output(P) to FLASH_WRN	-0.3	-	-	ns
t_{dqso}	Chip latency for FLASH_DQS output	3.6	5.1	7.3	ns
$t_{dqo2dqso}$	Skew from FLASH_DATA output(R/F) to FLASH_DQS output	-0.4/ -0.4			ns
t_{dqsi}	Chip latency for FLASH_DQS input	1.3	1.8	2. 6	ns
$t_{dqi2dqsi}$	Skew from FLASH_DATA input(R/F) to FLASH_DQS input	-1.3/0.3			ns

4.3.3 Toggle Interface

a. Toggle Address/Command Latch Cycle

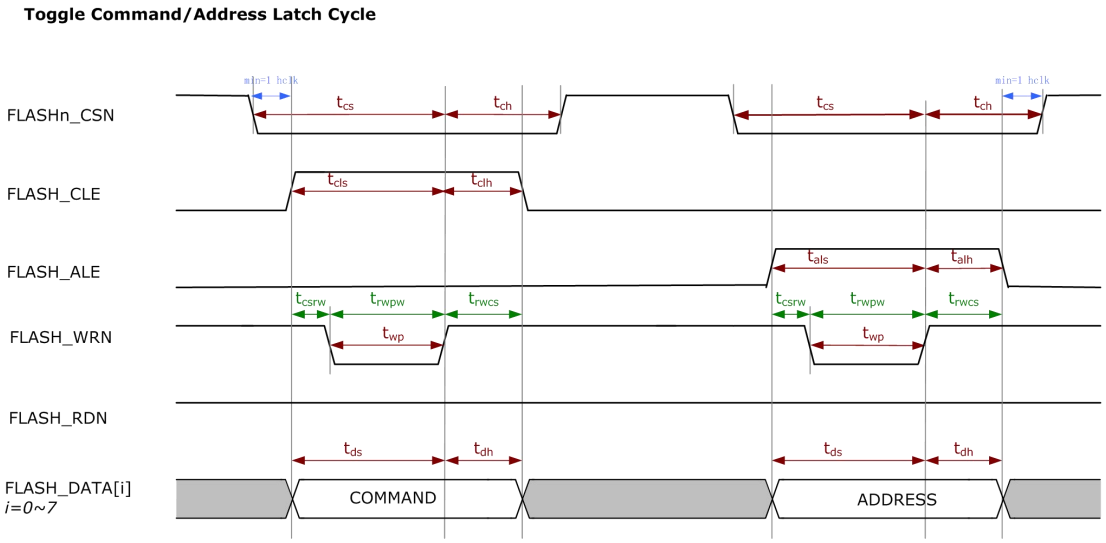


Fig. 4-13 NandC Toggle Address/Command Latch Cycle

b. Toggle Data Input Cycles

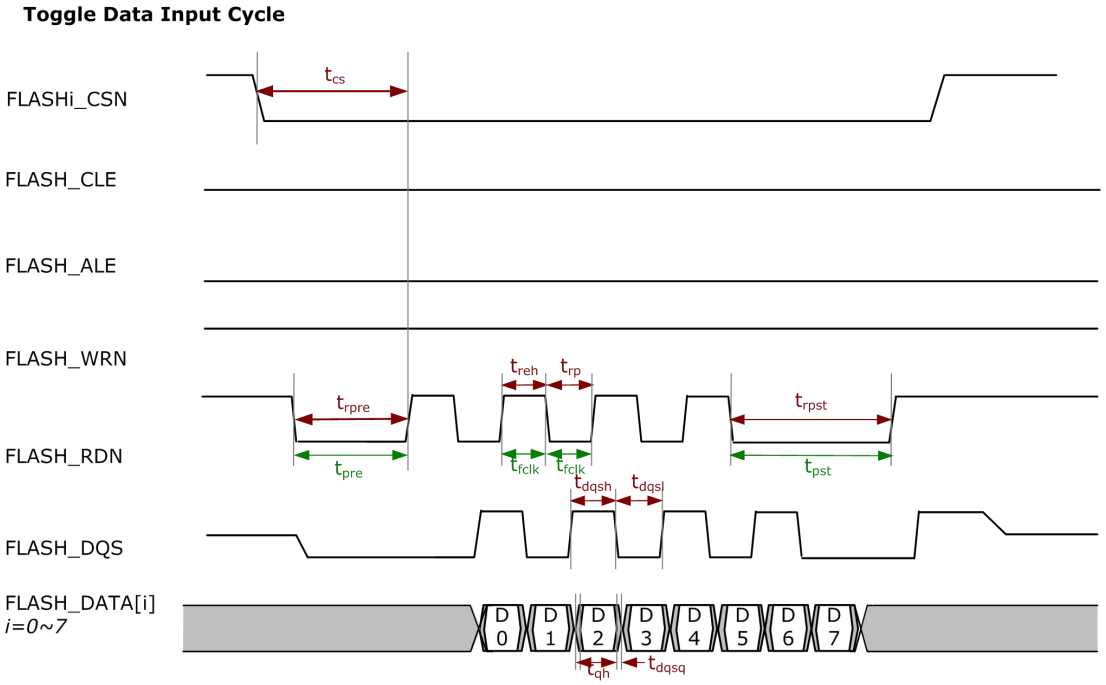


Fig. 4-14 NandC Toggle Data Input Cycles

c. Toggle Data Output Cycles

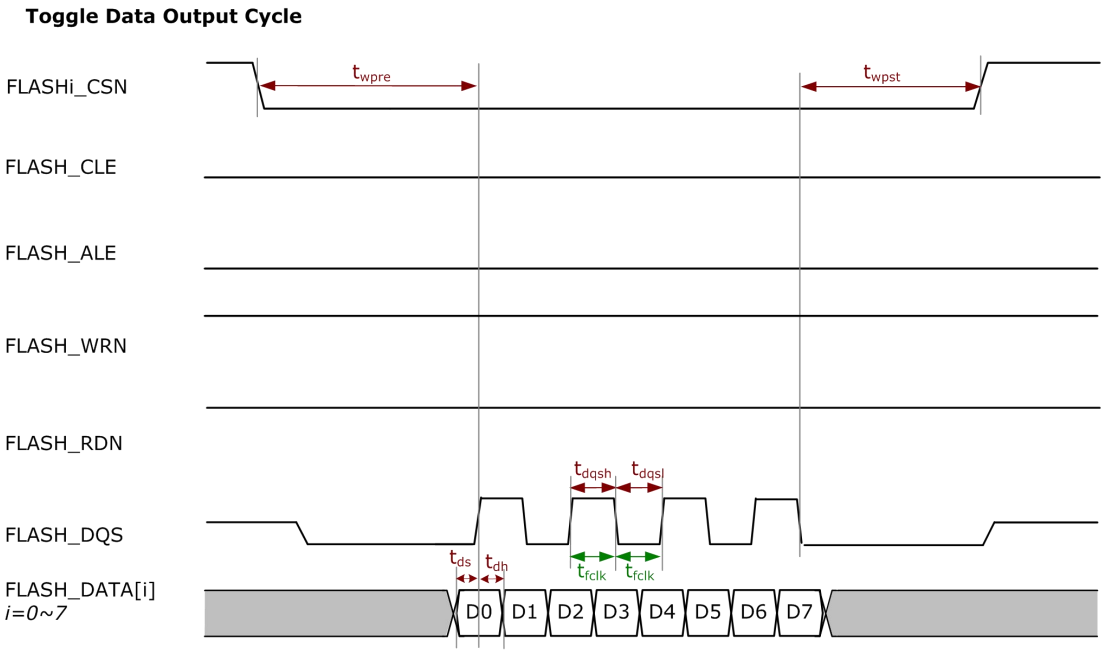


Fig. 4-15 NandC Toggle Data Output Cycles

Table 4-5 NandC I/O Skew: Toggle

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{wrn}	Chip latency for LASH_WRN	3.3	4.8	7.2	ns
t_{rdn}	Chip latency for FLASH_RDN	-0.022	-0.016	-0.035	ns
$t_{cle2wrn}$	Skew from FLASH_CLE to FLASH_WRN	-0.064	-0.081	-0.118	ns
$t_{ale2wrn}$	Skew from FLASH_ALE to FLASH_WRN	-0.071	-0.100	-0.163	ns
$t_{dqo2wrn}$	Skew from FLASH_DATA output(P) to FLASH_WRN	-0.092	-0.095	-0.147	ns
t_{dqso}	Chip latency for FLASH_DQS output	3.604	5.094	7.308	ns
$t_{dqo2dqso}$	Skew from FLASH_DATA output(R/F) to FLASH_DQS output	-0.380/ -0.414	-0.369/ -0.426	-0.302/ -0.395	ns
t_{dqsi}	Chip latency for FLASH_DQS input	1. 295	1. 764	2. 4504	ns
$t_{dqi2dqsi}$	Skew from FLASH_DATA input(R/F) to FLASH_DQS input	-0.944/ 0.343	-1.068/ 0.240	-1.296/ 0.158	ns

4.4 eMMC Timing Diagram

4.4.1 CMD Interface Timing

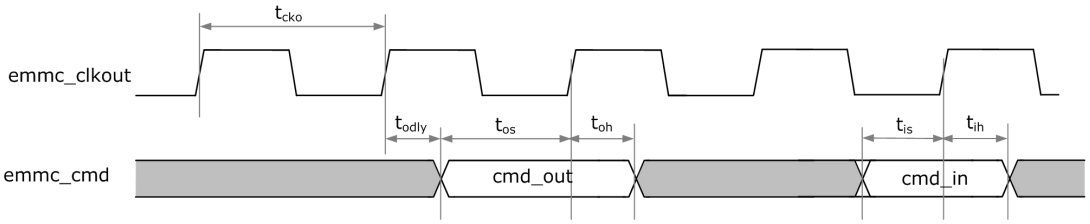


Fig.4-16 eMMC CMD Interface Timing

Table 4-6 eMMC CMD Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
Clock emmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	200	400	KHz
t_{cki}	1/2 emmc_cclkin cycle	10①	-	-	ns
t_{cko}	emmc_clkout cycle	20①	-	-	ns
t_r	Rise time for emmc_clkout	-	-	2.1	ns
t_f	Fall time for emmc_clkout	-	-	2.0	ns
Inputs emmc_cmd					
t_{is}	Input setup time	7.8	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs emmc_cmd					
t_{odly}	Output delay time during data transfer	-	-	7.5	ns
t_{os}	Output setup time	12.5	-	-	ns
t_{oh}	Output hold time	1.3	-	-	ns

Note :The max emmc_cclkin and emmc_clkout is 50MHz.

4.4.2 DAT Interface Timing

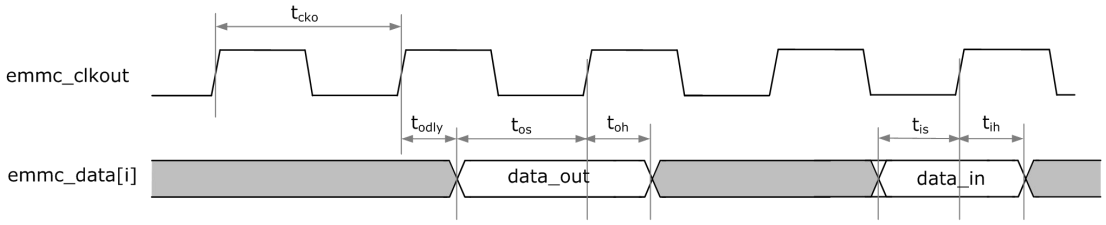


Fig.4-17 eMMC Data Interface Timing

Table 4-7 eMMC Data Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
Clock emmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	-	400	KHz
t_{cki}	1/2 emmc_cclkin cycle	10①	-	-	ns
t_{cko}	emmc_clkout cycle	20①	-	-	ns
t_r	Rise time for emmc_clkout	-	-	2.1	ns
t_f	Fall time for emmc_clkout	-	-	2.0	ns
Inputs emmc_data (i=0,1,…,7)					
t_{is}	Input setup time	7.8	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs emmc_data (i=0,1,…,7)					

t_{odly}	Output delay time during data transfer	-	-	7.5	ns
t_{os}	Output setup time	12.5	-	-	ns
t_{oh}	Output hold time	1.3	-	-	ns

Note :*The max emmc_cclkin and emmc_clkout is 50MHz.*

4.4.3 DAT Interface Timing, DDR4 Mode

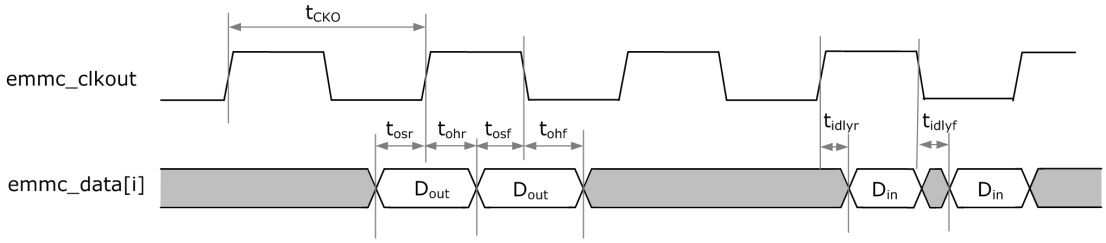


Fig.4-18 eMMC Data Interface Timing, DDR4 Mode

Table 4-2 eMMC Data Interface Timing, DDR4 Mode

*****timing condition: VCCIO=3.3V, $C_L \leqslant 8pF$, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
Clock emmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	-	400	KHz
t_{cki}	1/2 emmc_cclkin cycle	10①	-	-	ns
t_{cko}	emmc_clkout cycle	20①	-	-	ns
t_r	Rise time for emmc_clkout	-	-	2.1	ns
t_f	Fall time for emmc_clkout	-	-	2.0	ns
Inputs emmc_data (i=0,1,2,3)					
t_{idlyr}	Input delay for rising edge	-	-	7.8	ns
t_{idlyf}	Input delay for falling edge	-	-	7.8	ns
Outputs emmc_data (i=0,1,2,3)					
t_{osr}	Output setup time for rising edge	3.5	-	-	ns
t_{ohr}	Output hold time for rising edge	1.3	-	-	ns
t_{osf}	Output setup time for falling edge	3.5	-	-	ns
t_{ohf}	Output hold time for falling edge	1.3	-	-	ns

Note :*The max emmc_cclkin and emmc_clkout is 50MHz.*

4.4.4 DAT Interface Timing, DDR8 Mode

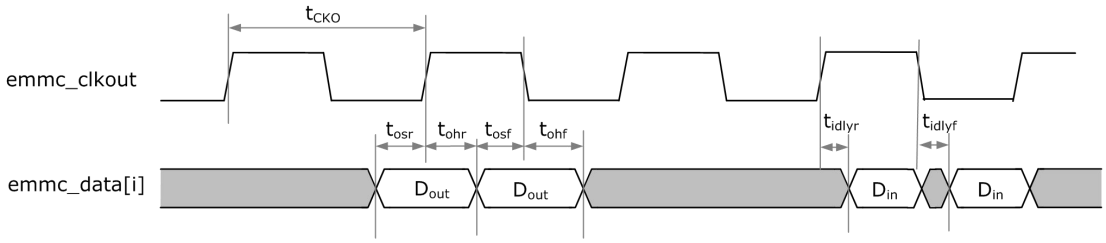


Fig.4-19 eMMC Data Interface Timing, DDR8 Mode

Table 4-2 eMMC Data Interface Timing, DDR8 Mode

*****timing condition: VCCIO=3.3V, $C_L \leqslant 8pF$, drive strength 8mA,(use_ddr_hold should be selected)

Parameter		Min.	Typ.	Max.	Unit
Clock emmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	-	400	KHz
t_{cko}	emmc_clkout cycle	20①	-	-	ns
t_r	Rise time for emmc_clkout	-	-	2.1	ns
t_f	Fall time for emmc_clkout	-	-	2.0	ns
Inputs emmc_data (i=0,1,…,7)					
t_{idlyr}	Input delay for rising edge	-	-	7.8	ns
t_{idlyf}	Input delay for falling edge	-	-	7.8	ns
Outputs emmc_data (i=0,1,…,7)					
t_{osr}	Output setup time for rising edge	3.2	-	-	ns
t_{ohr}	Output hold time for rising edge	4.8	-	-	ns
t_{osf}	Output setup time for falling edge	3.2	-	-	ns
t_{ohf}	Output hold time for falling edge	4.8	-	-	ns

Note :*The max emmc_cclkin and emmc_clkout is 50MHz.*

4.5 SDMMC Timing Diagram

4.5.1CMD Interface Timing

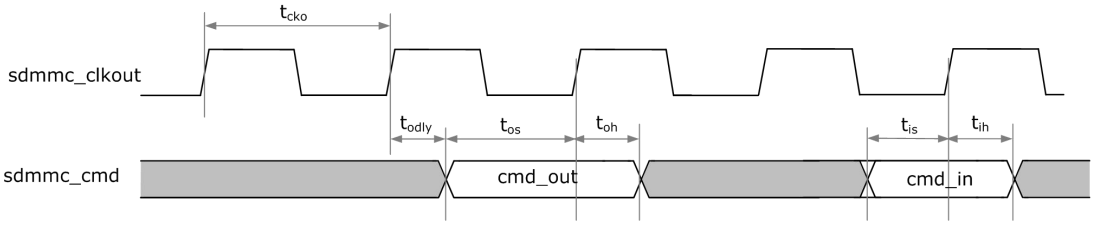


Fig. 4-20 SDMMC CMD Interface Timing

Table 4-8 SDMMC CMD Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 4mA

Parameter	Min.	Typ.	Max.	Unit

Clock sdmmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	200	400	KHz
t_{cki}	1/2 sdmmc_cclkin cycle	10①	-	-	ns
t_{cko}	sdmmc_clkout cycle	20①	-	-	ns
t_r	Rise time for sdmmc_clkout	-	-	3.3	ns
t_f	Fall time for sdmmc_clkout	-	-	3.3	ns
Inputs sdmmc_cmd					
t_{is}	Input setup time	7.0	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs sdmmc_cmd					
t_{odly}	Output delay time during data transfer	-	-	6.5	ns
t_{os}	Output setup time	13.5	-	-	ns
t_{oh}	Output hold time	1.3	-	-	ns

Note:*The max sdmmc_cclkin and sdmmc_clkout is 50MHz.*

4.5.2 DAT Interface Timing

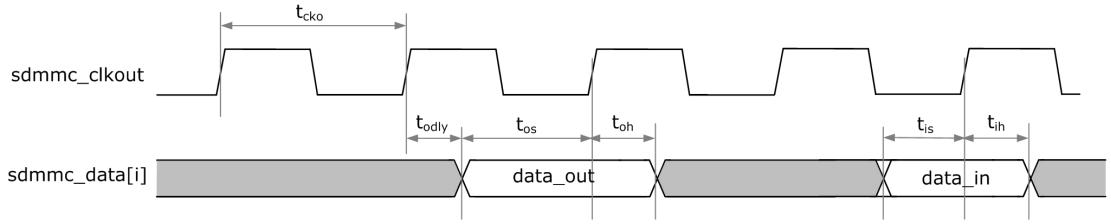


Fig. 4-21 SDMMC Data Interface Timing

Table 4-9 SDMMC Data Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
Clock sdmmc_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	52	MHz
f_{od}	Clock frequency Identification Mode	-	-	400	KHz
t_{cki}	1/2 sdmmc_cclkin cycle	10①	-	-	ns
t_{cko}	sdmmc_clkout cycle	20①	-	-	ns
t_r	Rise time for sdmmc_clkout	-	-	3.3	ns
t_f	Fall time for sdmmc_clkout	-	-	3.3	ns
Inputs sdmmc_data (i=0,1,…,7)					
t_{is}	Input setup time	7.0	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs sdmmc_data (i=0,1,…,7)					
t_{odly}	Output delay time during data transfer	-	-	6.5	ns
t_{os}	Output setup time	13.5	-	-	ns

t_{oh}	Output hold time	1.3	-	-	ns

Note :The max sdmmc_cclkin and sdmmc_clkout is 50MHz.

4.5.3 LCDC Timing Diagram

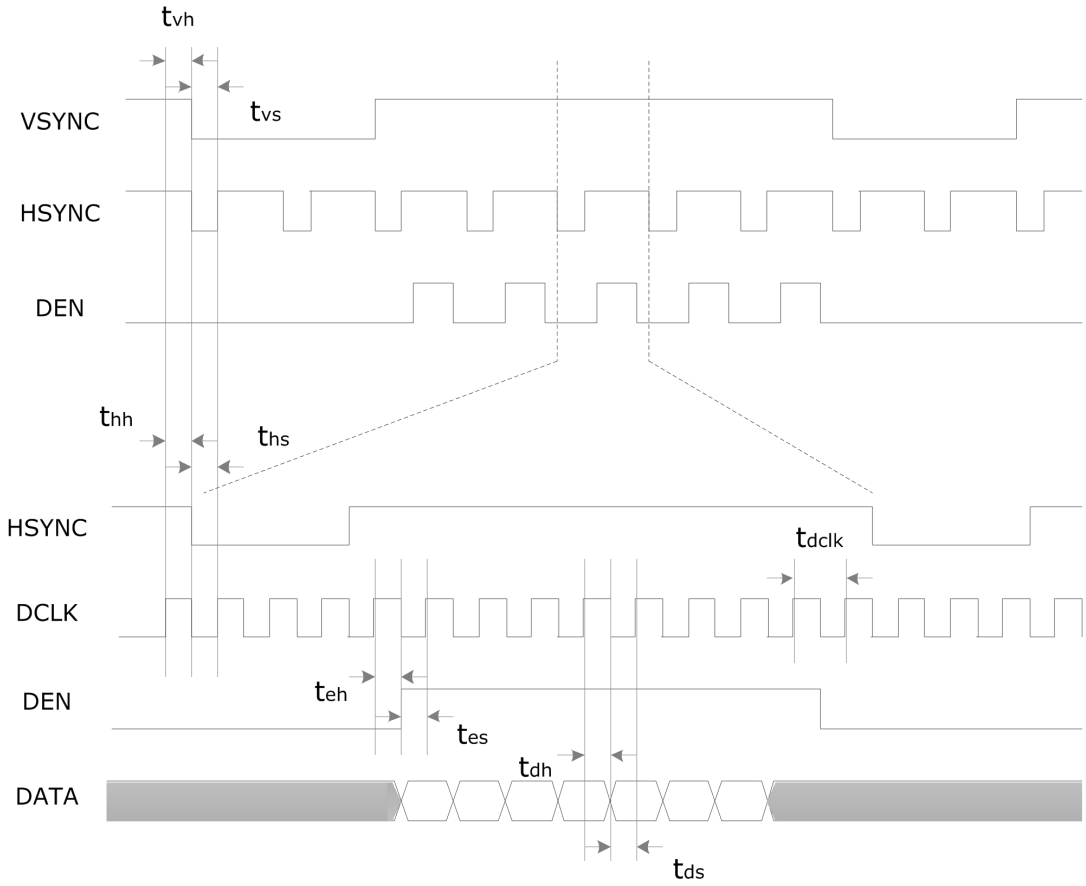


Fig. 4-22 LCDC RGB interface timing (SDR)

Table 4-10 LCDC0 RGB interface (SDR) signal timing constant

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	5	-	-	ns
t_{vs}	VSYNC setup to DCLK rising edge	1.6	-	-	ns
t_{vh}	VSYNC hold from DCLK rising edge	1.5	-	-	ns
t_{hs}	HSYNC setup to DCLK rising edge	1.6	-	-	ns
t_{hh}	HSYNC hold from DCLK rising edge	1.5	-	-	ns
t_{es}	DEN setup to DCLK rising edge	1.4	-	-	ns
t_{eh}	DEN hold from DCLK rising edge	1.5	-	-	ns
t_{ds}	DATA setup to DCLK rising edge	1.5	-	-	ns
t_{dh}	DATA hold from DCLK rising edge	1.5	-	-	ns

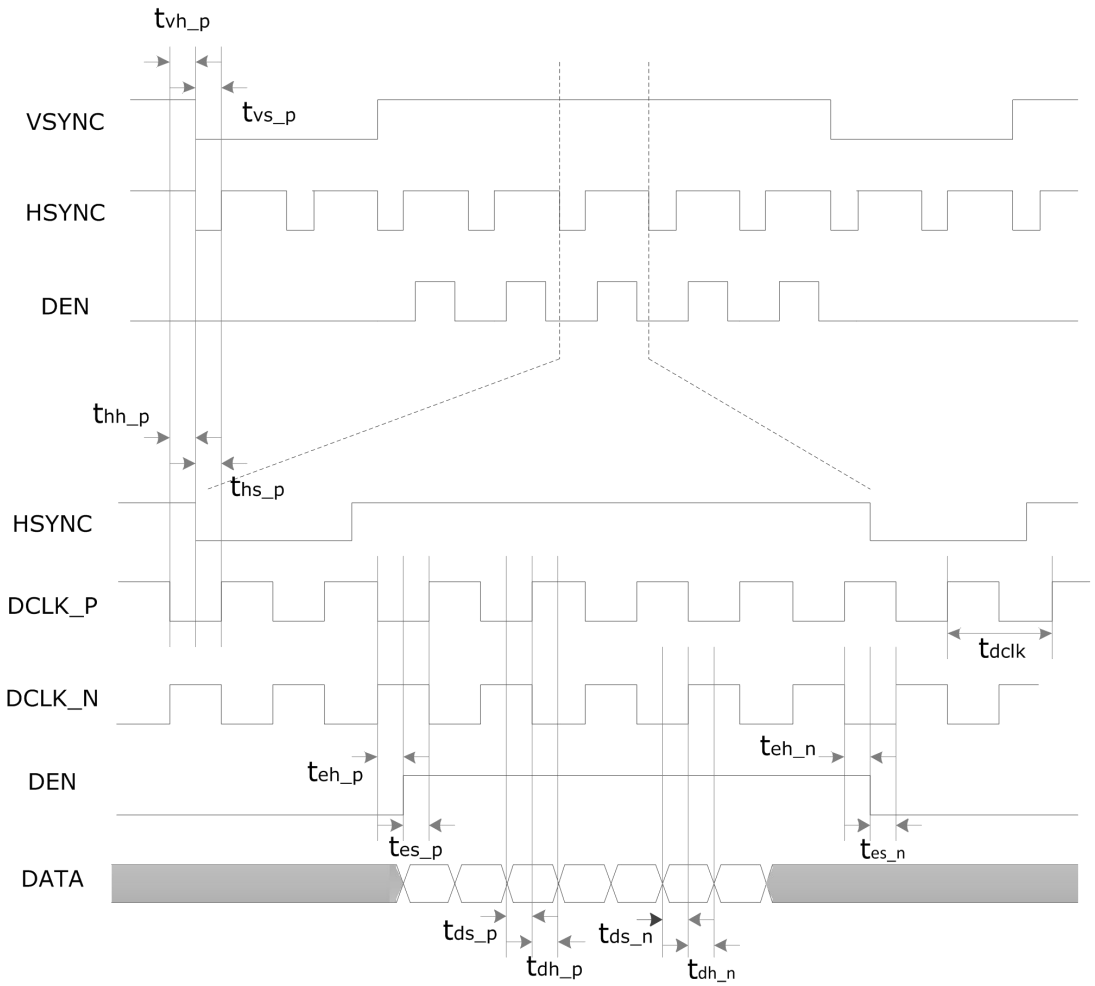


Fig. 4-23 LCDC RGB interface timing (DDR)

Table 4-11 LCDC0 RGB interface (DDR) signal timing constant

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	6.67	-	-	ns
t_{vs_p}	VSYNC setup to DCLK_P rising edge	1.4	-	-	ns
t_{vh_p}	VSYNC hold from DCLK_P rising edge	1.4	-	-	ns
t_{hs_p}	HSYNC setup to DCLK_P rising edge	1.4	-	-	ns
t_{hh_p}	HSYNC hold from DCLK_P rising edge	1.4	-	-	ns
t_{es_p}	DEN setup to DCLK_P rising edge	1.4	-	-	ns
t_{eh_p}	DEN hold from DCLK_P rising edge	1.4	-	-	ns
t_{ds_p}	DEN setup to DCLK_N rising edge	1.4	-	-	ns
t_{dh_p}	DEN hold from DCLK_N rising edge	1.4	-	-	ns
t_{ds_n}	DATA setup to DCLK_P rising edge	1.4	-	-	ns
t_{dh_n}	DATA hold from DCLK_P rising edge	1.4	-	-	ns
t_{ds_p}	DATA setup to DCLK_N rising edge	1.4	-	-	ns
t_{dh_p}	DATA hold from DCLK_N rising edge	1.4	-	-	ns

Table 4-12 LCDC1 RGB interface (SDR) signal timing constant

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	5	-	-	ns
t_{vs}	VSYNC setup to DCLK falling edge	1.8	-	-	ns
t_{vh}	VSYNC hold from DCLK falling edge	1.6	-	-	ns
t_{hs}	HSYNC setup to DCLK falling edge	1.8	-	-	ns

t_{hh}	HSYNC hold from DCLK falling edge	1.6	-	-	ns
t_{es}	DEN setup to DCLK falling edge	1.8	-	-	ns
t_{eh}	DEN hold from DCLK falling edge	1.6	-	-	ns
t_{ds}	DATA setup to DCLK falling edge	1.5	-	-	ns
t_{dh}	DATA hold from DCLK falling edge	1.5	-	-	ns

Table 4-13 LCDC1 RGB interface (DDR) signal timing constant

*timing codition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	6.67	-	-	ns
t_{vs_p}	VSYNC setup to DCLK_P rising edge	1.3	-	-	ns
t_{vh_p}	VSYNC hold from DCLK_P rising edge	1.3	-	-	ns
t_{hs_p}	HSYNC setup to DCLK_P rising edge	1.3	-	-	ns
t_{hh_p}	HSYNC hold from DCLK_P rising edge	1.3	-	-	ns
t_{es_p}	DEN setup to DCLK_P rising edge	1.3	-	-	ns
t_{eh_p}	DEN hold from DCLK_P rising edge	1.3	-	-	ns
t_{ds_p}	DEN setup to DCLK_N rising edge	1.3	-	-	ns
t_{dh_p}	DEN hold from DCLK_N rising edge	1.3	-	-	ns
t_{ds_n}	DATA setup to DCLK_P rising edge	1.3	-	-	ns
t_{dh_n}	DATA hold from DCLK_P rising edge	1.3	-	-	ns
t_{ds_p}	DATA setup to DCLK_N rising edge	1.3	-	-	ns
t_{dh_p}	DATA hold from DCLK_N rising edge	1.3	-	-	ns

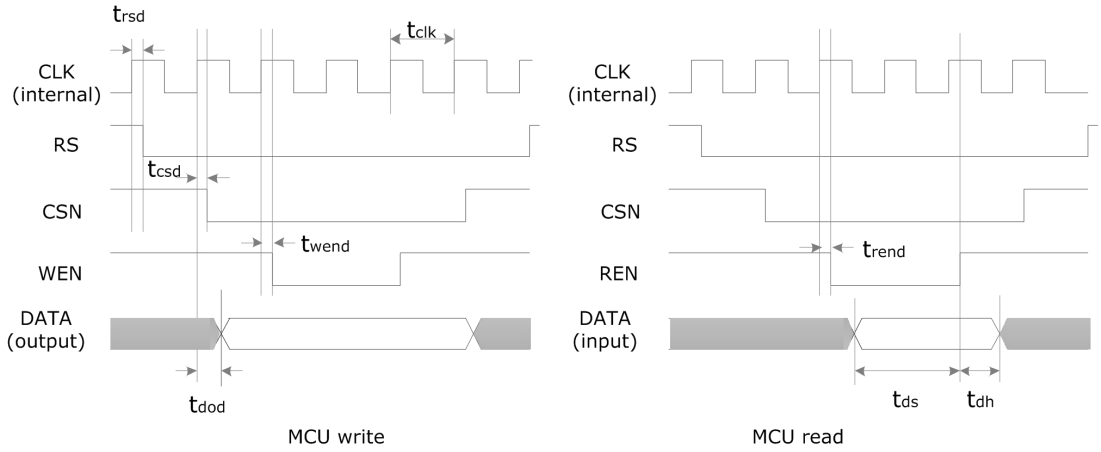


Fig. 4-24 LCDC MCU interface (i80)timing

Table 4-14 LCDC0 RGB interface signal timing constant

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{clk}	Internal clock period	6.64	-	-	ns
t_{rsd}	RS delay from CLK rising edge	4.407	6.605	9.801	ns
t_{csd}	CSN delay from CLK rising edge	5.331	8.070	12.098	ns
t_{wend}	WEN delay from CLK rising edge	5.383	8.166	12.269	ns
t_{rend}	REN delay from CLK rising edge	5.410	8.214	12.387	ns
t_{dod}	D_out delay from CLK rising edge	6.988	8.214	16.135	ns
t_{ds}	D_in setup to REN rising edge	8.442	12.55	18.234	ns
t_{dh}	D_in hold from REN rising edge	-13.1	-8.57	-6.173	ns

Table 4-15 LCDC1 RGB interface signal timing constant

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 8mA

Parameter	Min.	Typ.	Max.	Unit

t_{clk}	Internal clock period	6.64	-	-	ns
t_{rsd}	RS delay from CLK rising edge	4.377	6.547	9.775	ns
t_{csd}	CSN delay from CLK rising edge	5.218	7,953	12.008	ns
t_{wend}	WEN delay from CLK rising edge	5.302	8.073	12.172	ns
t_{rend}	REN delay from CLK rising edge	5.385	8.168	12.301	ns
t_{dod}	D_out delay from CLK rising edge	6.799	10.40	15.547	ns
t_{ds}	D_in setup to REN rising edge	7.118	11.41	17.827	ns
t_{dh}	D_in hold from REN rising edge	-11.9	-7.03	-4.054	ns

4.5.4 CIF Timing Diagram

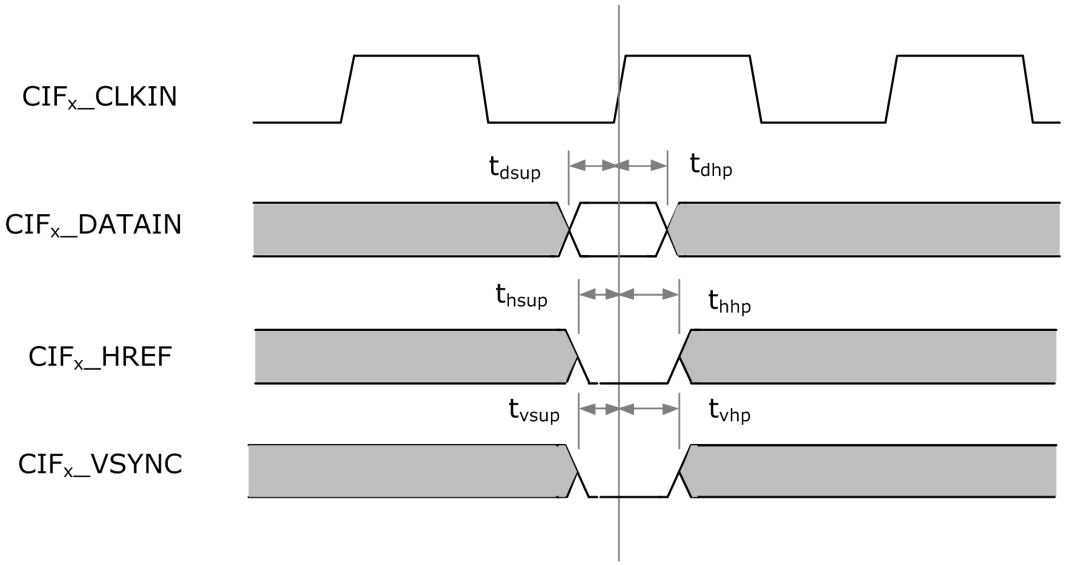


Fig. 4-25 CIF timing diagram

Table 4-16 CIF Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_c(sdr)	Cycle time for sdr	10	-	-	ns
t_{hsup}	Input HREF setup time to CIF_CLKIN rising edge	4.6	-	-	ns
t_{hhp}	Input HREF hold time to CIF_CLKIN rising edge	2.1	-	-	ns
t_{vsup}	Input VSYNC setup time to CIF_CLKIN rising edge	4.6	-	-	ns
t_{vhp}	Input VSYNC hold time to CIF_CLKIN rising edge	2.1	-	-	ns
t_{dsup}	Input DATAIN setup time to CIF_CLKIN rising edge	2.5	-	-	ns
t_{dhp}	Input DATAIN hold time to CIF_CLKIN rising edge	0	-	-	ns

4.5.5 GPS Timing Diagram

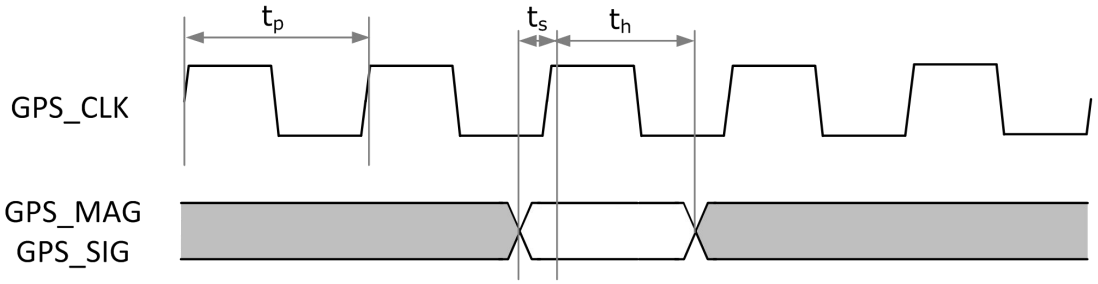


Fig. 4-26 RK3188T GPS timing waveform

Table 4-17 RK3188T GPS Timing parameters

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

parameter		Min.	Typ.	Max.	Unit
t_p	clock period	20	-		ns
t_s	setup time	10	-		ns
t_h	hold time	5	-		ns

4.5.6 I2S Timing Diagram

4.5.7 Master mode

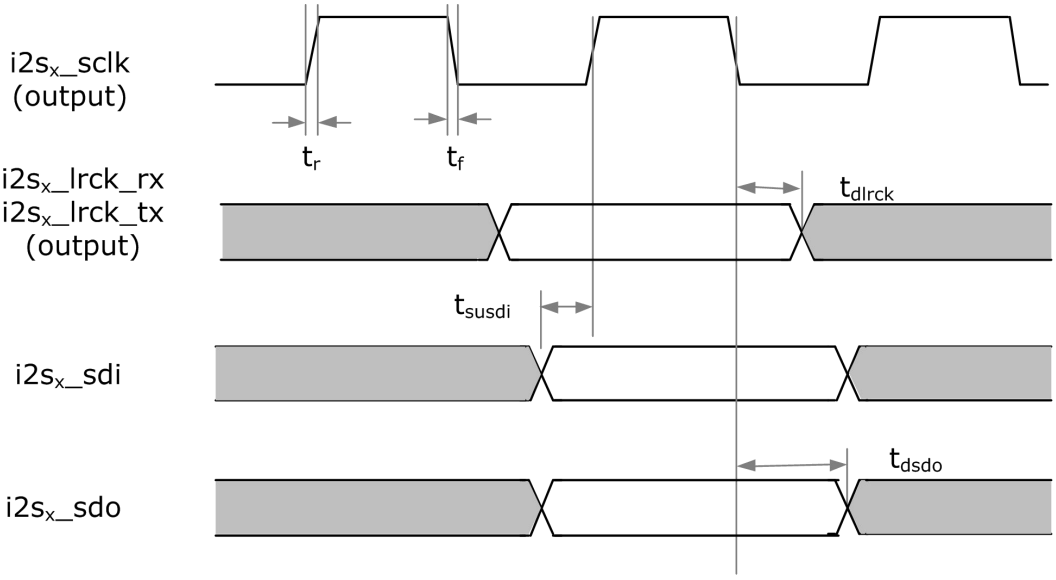


Fig. 4-27 Master mode timing diagram

Table 4-18 Meaning of the parameter in Fig. 9-1

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_r	i2s$_x$_sclk(output) rising time	-	-	6.3	ns
t_f	i2s$_x$_sclk(output) falling time	-	-	5.9	ns
t_{dlrck}	i2s$_x$_lrck_rx/i2s$_x$_lrck_tx propagation delay from i2s$_x$_sclk falling edge			1.9	ns
t_{susdi}	i2s$_x$_sdo setup time to i2s$_x$_sclk rising edge	10.0			ns
t_{dsdo}	i2s$_x$_sdi propagation delay from i2s$_x$_sclk falling edge			1.2	ns

4.5.8 Slave mode

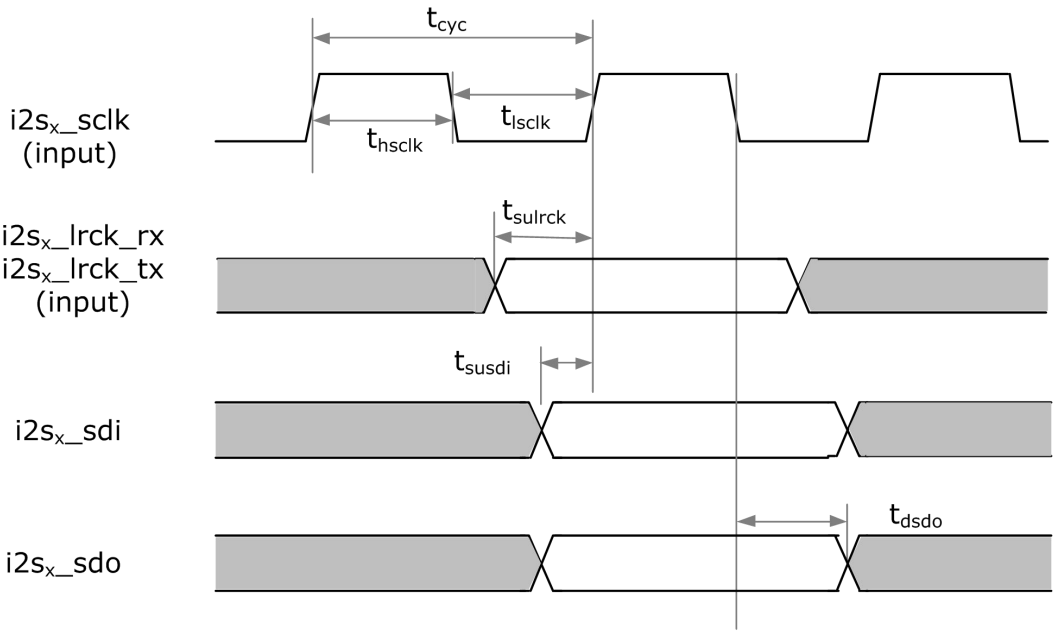


Fig. 4-28 Slave mode timing diagram

Table 4-19 Meaning of the parameter in Fig. 9-2

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{cyc}	$i2s_x$_sclk cycle time	40	-	-	ns
t_{hsclk}	$i2s_x$_sclk pulse width high	20	-	-	ns
t_{lsclk}	i2sx_sclk pulse width low	20	-	-	ns
t_{sulrck}	$i2s_x$_lrck_rx/$i2s_x$_lrck_tx setup time to i2sx_sclk rising edge			12.0	ns
t_{susdi}	$i2s_x$_sdo setup time to $i2s_x$_sclk rising edge	15.0			ns
t_{dsdo}	$i2s_x$_sdi propagation delay from $i2s_x$_sclk falling edge			11.0	ns

4.6 SDIO Timing Diagram

4.6.1 CMD Interface Timing

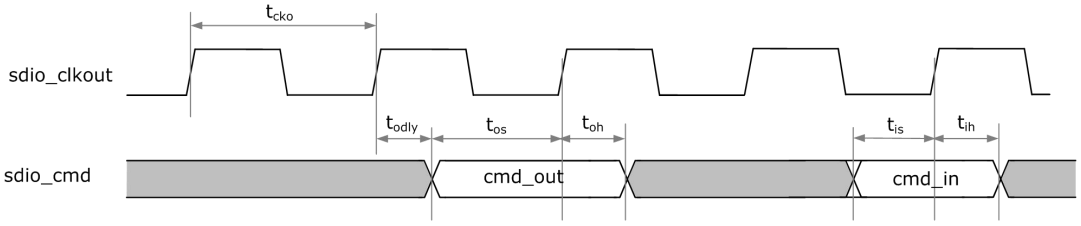


Fig.4-29 SDIO CMD Interface Timing

Table 4-20 SDIO CMD Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
Clock sdio_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz

f_{od}	Clock frequency Identification Mode	-	200	400	KHz
t_{cki}	1/2 sdio_cclkin cycle	10①	-	-	ns
t_{cko}	sdio_clkout cycle	20①	-	-	ns
t_r	Rise time for sdio_clkout	-	-	1.7	ns
t_f	Fall time for sdio_clkout	-	-	1.7	ns
Inputs sdio_cmd					
t_{is}	Input setup time	7.4	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs sdio_cmd					
t_{odly}	Output delay time during data transfer	-	-	7.7	ns
t_{os}	Output setup time	12.3	-	-	ns
t_{oh}	Output hold time	1.3	-	-	ns

Note:*The max sdio_cclkin and sdio_clkout is 50MHz.*

4.6.2 DAT Interface Timing

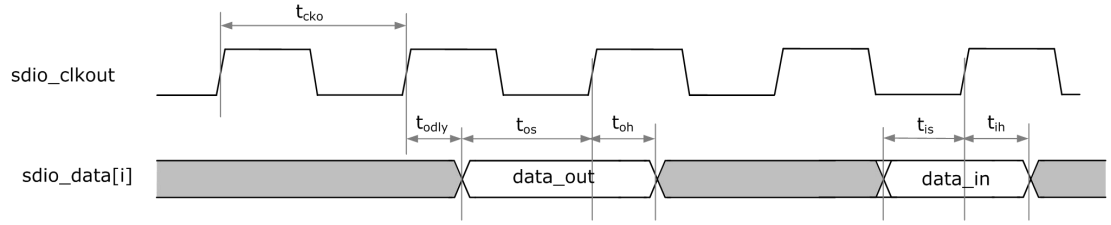


Fig. 4-30 SDIO Data Interface Timing

Table 4-21 SDIO Data Interface Timing

*timing condition: VCCIO=3.3V, CL≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
Clock sdio_clkout					
f_{pp}	Clock frequency Data Transfer Mode	-	-	50	MHz
f_{od}	Clock frequency Identification Mode	-	-	400	KHz
t_{cki}	1/2 sdio_cclkin cycle	10①	-	-	ns
t_{cko}	sdio_clkout cycle	20①	-	-	ns
t_r	Rise time for sdio_clkout	-	-	1.7	ns
t_f	Fall time for sdio_clkout	-	-	1.7	ns
Inputs sdio_datai (i=0,1,2,3)					
t_{is}	Input setup time	7.4	-	-	ns
t_{ih}	Input hold time	1.0	-	-	ns
Outputs sdio_data (i=0,1,2,3)					
t_{odly}	Output delay time during data transfer	-	-	7.7	ns
t_{os}	Output setup time	12.3	-	-	ns
t_{oh}	Output hold time	1.3	-	-	ns

Note :*The max sdio_cclkin and sdio_clkout is 50MHz.*

4.7 MAC Timing Diagram

4.7.1 Management Timing Diagram

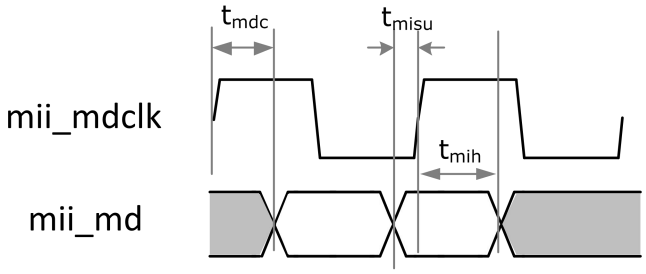


Fig. 4-31 Management timing diagram

Table 4-22 Management timing parameters

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{mdc}	MDC clock period	400	-	-	ns
t_{modly}	Mii_md output delay time from mii_mdclk rising edge	261.2	-	-	ns
t_{misu}	Mii_md input setup time from mii_mdclk rising edge	133.3	-	-	ns
t_{mih}	Mii_md input hold time from mii_mdclk rising edge	0	-	-	ns

4.8 RMII Timing Diagram

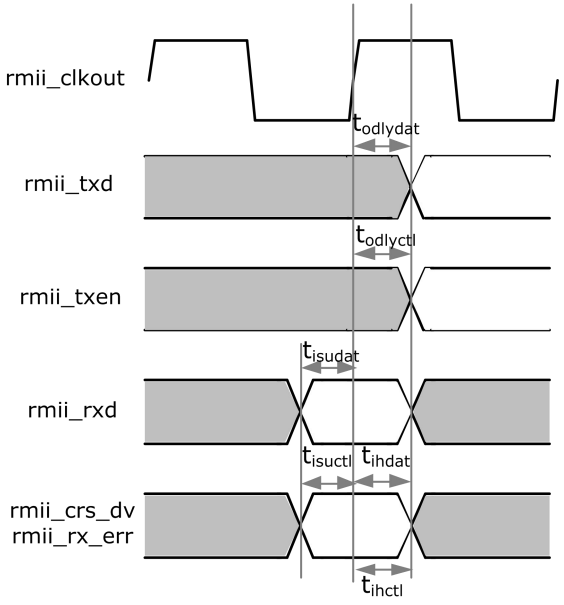


Fig. 4-32 RMII timing diagram

Table 4-23 RMii timing parameters

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
	Rmii_clkout clock frequency	20	-	-	MHz
t_r	Rmii clkout clock rising edge	-	-	1.7	ns
t_f	Rmii clkout clock falling edge	-	-	1.7	ns

$t_{odlydat}$	Rmii txd output delay	-	-	12	ns
$t_{odlyctl}$	Rmii control signals output delay	-	-	12	ns
t_{isudat}	rmii_rxd setup to rmii_clkout rising edge	14	-	-	ns
t_{ihdat}	rmii_rxd hold to rmii_clkout rising edge	5	-	-	ns
t_{isuctl}	rmii_crs_dv, rmii_rx_err setup to rmii_clkout rising edge	14	-	-	ns
t_{ihctl}	rmii_crs_dv, rmii_rx_err hold to rmii_clkout rising edge	5	-	-	ns

4.9 HSADC Timing Diagram

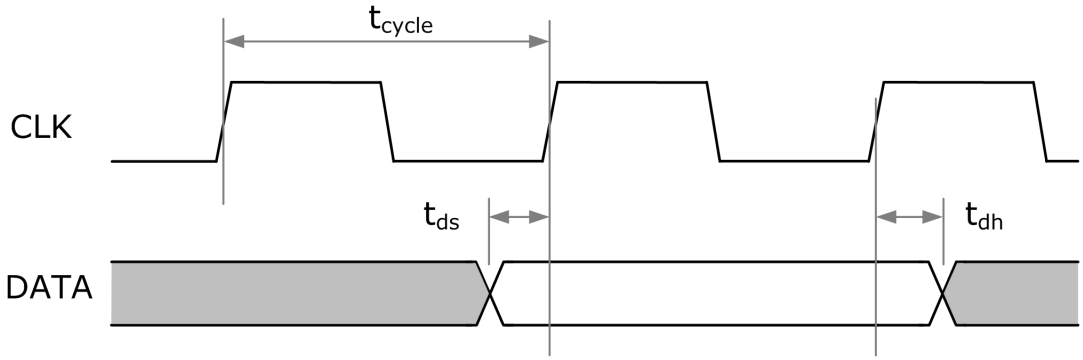


Fig. 4-33 HS-ADC Interface timing diagram

Table 4-24 HS-ADC interface timing parameter, Master mode

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle	15	-	-	ns
t_{ds}	Data to clock setup time	8.0	-	-	ns
t_{dh}	Data to clock hold time	3.9	-	-	ns

Table 4-25 HS-ADC interface timing parameter, Slave mode

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle	16.6	-	-	ns
t_{ds}	Data to clock setup time	7.3	-	-	ns
t_{dh}	Data to clock hold time	3.9	-	-	ns

Note: When interface configured as TS or GPS interface, CLK is input from pad, when configured as ADC interface, CLK is output to pad.

5.0 SPI Timing Diagram

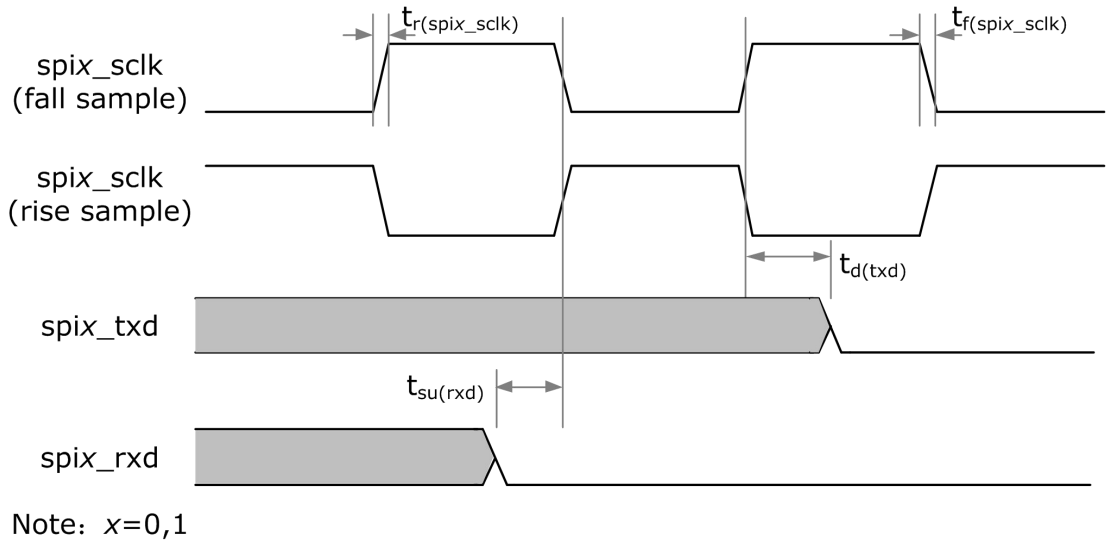


Fig. 4-34 SPI controller timing diagram

Table 4-26 Timing parameter description-1

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
$t_{r(spix\_sclk)}$	rise time for spix_sclk	-	-	3.3	ns
$t_{f(spix\_sclk)}$	fall time for spix_sclk	-	-	3.2	ns
$t_{d(txd)}$	spix_txd propagation delay from spix_sclk drive edge	-	-	8	ns
$t_{su(rxd)}$	spix_rxd setup time to spix_sclk sample edge	5	-	-	ns

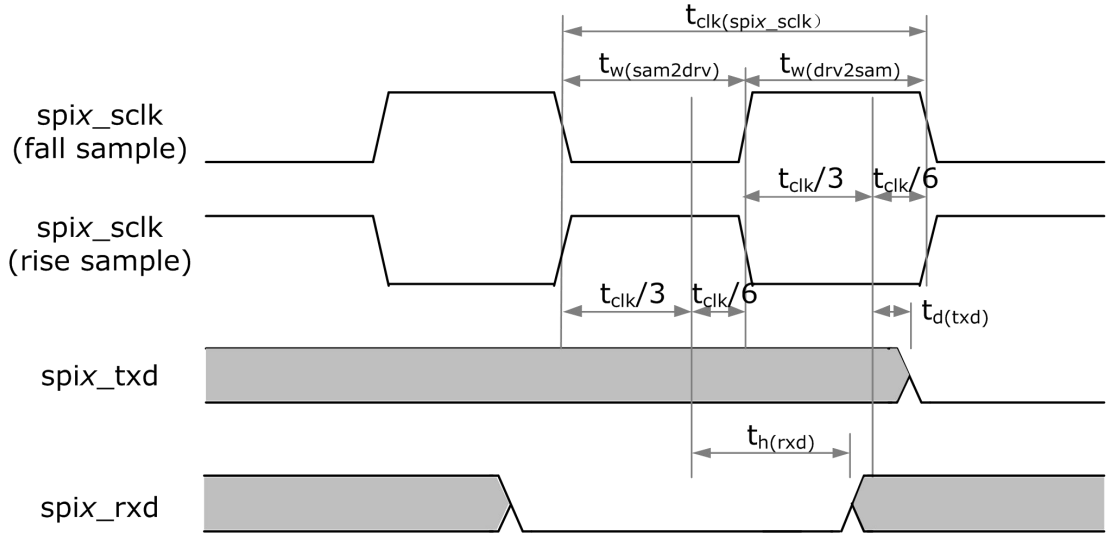
Note: x=0

Table 4-27 Timing parameter description-2

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
$t_{r(spix\_sclk)}$	rise time for spix_sclk	-	-	3.2	ns
$t_{f(spix\_sclk)}$	fall time for spix_sclk	-	-	3.3	ns
$t_{d(txd)}$	spix_txd propagation delay from spix_sclk drive edge	-	-	8	ns
$t_{su(rxd)}$	spix_rxd setup time to spix_sclk sample edge	5	-	-	ns

Note: x=1



Note：*x*=0,1

Fig. 4-35 SPI controller timing diagram in slave mode

Table 4-28 Timing parameter description-3

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
$t_{clk(spix\_clk)}$	spi*x*_sclk cycle time	60	-	-	ns
$t_{w(sam2drv)}$	spi*x*_sclk pulse width from sample edge to drive edge	30	-	-	ns
$t_{w(drv2sam)}$	spi*x*_sclk pulse width from drive edge to sample edge	30	-	-	ns
$t_{d(txd)}$	spi*x*_txd propagation delay from t_{clk}/3 after spi*x*_sclk drive edge	-	-	14.691	ns
$t_{h(rxd)}$	spi*x*_rxd hold time from t_{clk}/3 after spi*x*_sclk sample edge	0.676	-	-	ns

Note: x=0,1

5.1 I2C Timing Diagram

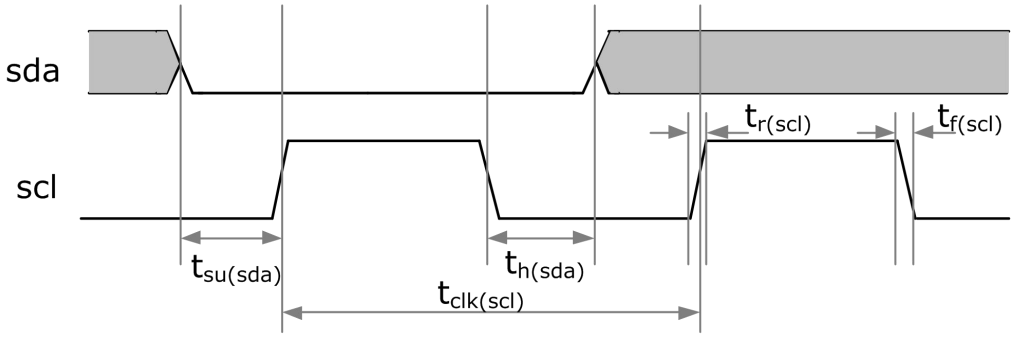


Fig. 4-36 I2C timing diagram

Table 4-29 I2C timing parameters

*timing condition: VCCIO=3.3V, CLOAD≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
100KHz mode					
$t_{clk(scl)}$	SCL clock period	-	10	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	2.5	-	us

$t_{su(sda)}$	SDA setup time to rising edge of SCL	-	2.5	-	us
400KHz mode					
$t_{clk(scl)}$	SCL clock frequency	-	2.5	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	0.6	-	us
$t_{su(sda)}$	SDA setup time to rising edge of SCL	-	0.6	-	us

Chapter 5 Hardware Guideline

5.1 Reference design for oscillator PCB connection

RK3188T only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram , the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model . Especially C1 and C2 value is advised to meet formula (C1 * C2)/(C1+C2) = ~8pF

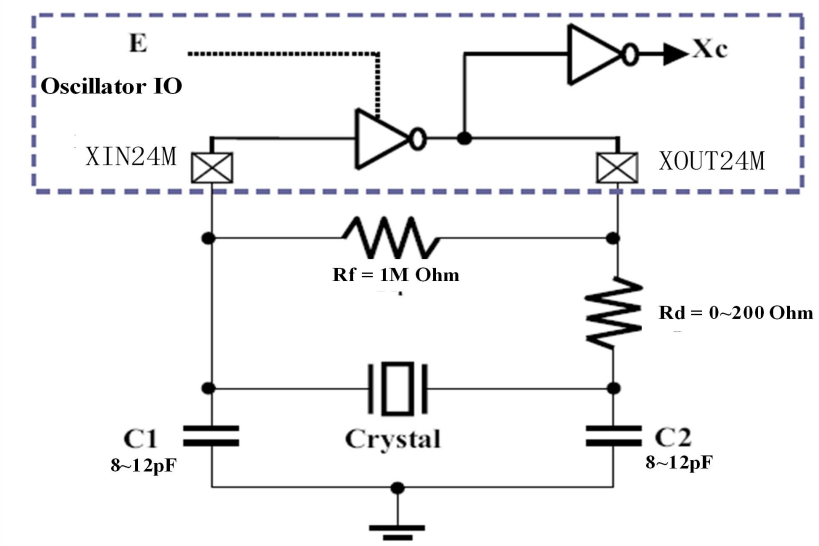


Fig. 5-1 External Reference Circuit for 24MHzOscillators

5.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK3188T.

The PLL's two analog supplies should be filtered with two series ferritebeads and two shunt 0.1uF and 0.01uF capacitors. The ferrite on VSS ispreferred but optional. Adding the ferrite on VSS converts supply noiseto substrate noise as seen by the PLL. The PLLs are designed to berelatively insensitive to supply and substrate noise, so the presenceof this ferrite is a second order issue.

The VDD/VSS is mapped to VDD_APLL/VSS_APLL, VDD_DPLL/VSS_DPLL and VDD_CGPLL/VSS_CGPLL.

The AVDD/AVSS is mapped to AVDD_APLL/AVSS_APLL, AVDD_DPLL/ AVSS_DPLL and AVDD_CGPLL/AVSS_CGPLL.

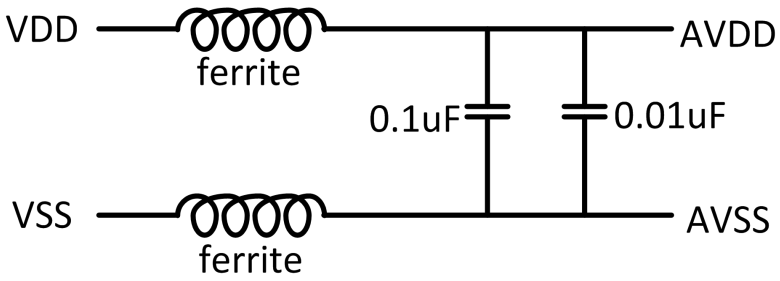


Fig. 5-2 External reference circuit for PLL

The ferrite beads should be similar one of the following from Murata:

Table 5-1 Ferrite Bead Selection

Part number	R@DC	Z@10MHz	Z@100MHz	size
BLM18EG601SN1	0.35	200	600	0603
BLM18PG471SN1	0.2	130	470	0603
BLM18KG601SN1	0.15	160	600	0603
BLM18AG601SN1	0.38	180	600	0603
BLM18AG102SN1	0.5	280	1000	0603
BLM18TG601TN1	0.45	190	600	0603
BLM15AG601SN1	0.6	200	600	0402
BLM15AX601SN1	0.34	190	600	0402
BLM15AX102SN1	0.49	250	1000	0402
BLM03AX601SN1	0.85	120	600	0201

Similar ferrite beads are also available from Panasonic. The key characteristics to select are:

- DC resistance less than 0.40 ohms
- impedance at 10MHz equal to or greater 180 ohms
- impedance at 100MHz equal to or greater than 600 ohms

The capacitors should be mounted as close to the package balls as possible.

5.3 Reference design for USB OTG/Host2.0 connection

In RK3188T there are USB OTG and USB Host2.0 interface, in fact, same interface is for them.The following diagram shows external reference design. Of course, for USB Host2.0some signals can be removed based on different application.

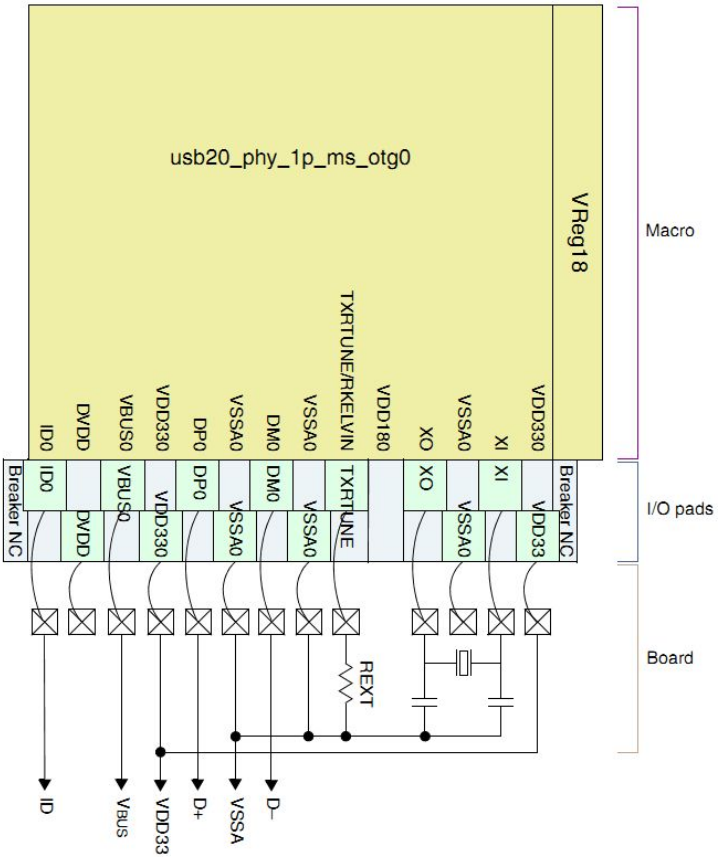


Fig. 5-3 RK3188T USB OTG/Host2.0 interface reference connection

5.4 RK3188T Power up/down sequence requirement

For all of the power supply in RK3188T, there is no any specific requirement of power up/down sequence except power supply between core logic and DDR3/LPDDR2 IO, between USB OTG/Host2.0 power supply.

- Power supply sequence for core logic(CVDD/AVDD) and DDR3/LPDDR2 IO (MVDD)

It is generally recommended that the core logic and DDR IO are powered-up together, and it is also acceptable for core logic supply to power-up a very short time before the DDR IO supply. If DDR IO supply must power-up before the core logic supply, it is advised to keep the time between these two events less than 100ms to limit excessive DDR IO current draws.

- Power supply sequence for core logic(CVDD/AVDD) and digital GPIO power①

There is no requirement on the power-up sequence for two above groups. It is generally recommended that "turn on the higher GPIO voltage first and then the lower core voltage" so that the crowbar current would not occur on the power-up stage.

There is no requirement on the power-down sequence for two above groups. Customers can decide which voltage to be down first based on the application need.

- Power supply sequence for core logic(CVDD/AVDD) and internal PMU voltage domain logic(PVDD) power

It is generally recommended that internal PMU voltage domain logic is powered-up before core logic to ensure that core logic is reset when it is powered-up. It is acceptable that internal PMU voltage domain logic and core logic are powered-up together. But core logic can't be powered-up before internal PMU voltage domain logic.

There is not requirement on the power-down sequence for core logic and internal PMU voltage domain logic.

- Power supply sequence for USB OTG/Host2.0

There is no requirement on the power-up and power-down sequence for the USB power supply USBDVDD_1V0(1.0V), USBVDD_1V8(1.8V) and USBVDD_3V3(3.3V). Customers can decide which voltage to be up and down first based on the application, it is recommended that the time duration between supply ramps be kept as short as possible.

Notes :①: digital GPIO power include LCD0_VCCj, LCD1_VCC, CIF_VCC, PVCC, APj_VCC, FLASH_VCC, VCCIOj

5.5 The relationship between CLK32K and NPOR

When power up, before NPOR de-asserted to high, 32.768KHz clock(CLK32K) must to be maintained at least 10 cycles stabilization. Customers must follow this rule to insure that the system reset can be correctly de-asserted, and RK3188T can normally work.

5.6 RK3188T Power on reset descriptions

The following figure shows power-on-reset sequence. External power-on-reset input signal NPOR is released after stabilization of oscillator input clock XIN24M. Internal signal sysrstn is generated after NPOR is filtered glitch, which can filter out 5 clock cycles(24MHz) for low pulse of NPOR, so 208ns low pulse of NPOR will not be recognized as valid power-on-reset signal for RK3188T.

To make PLLs work normally, the internal power down signal(pllpd) for PLLs must be high after power-on-reset, and maintains high level for more than 1us after sysrstn is deserted. Then PLL reset signals(pllrstn) are asserted for about 10.6us, and PLLs start to lock when pllrstn dessert, and consume about to 1330us to lock.

The system will wait about 1330us, then deactivate internal reset signal chiprstn, which is used to control generation logic of all the clock inside CRU.

After 256 cycles or about 10.7us, rstn_pre for reset signal of all internal IPs will be deserted, in other words, about 10.7us of clock has been generated before reset of every internal module

is released.

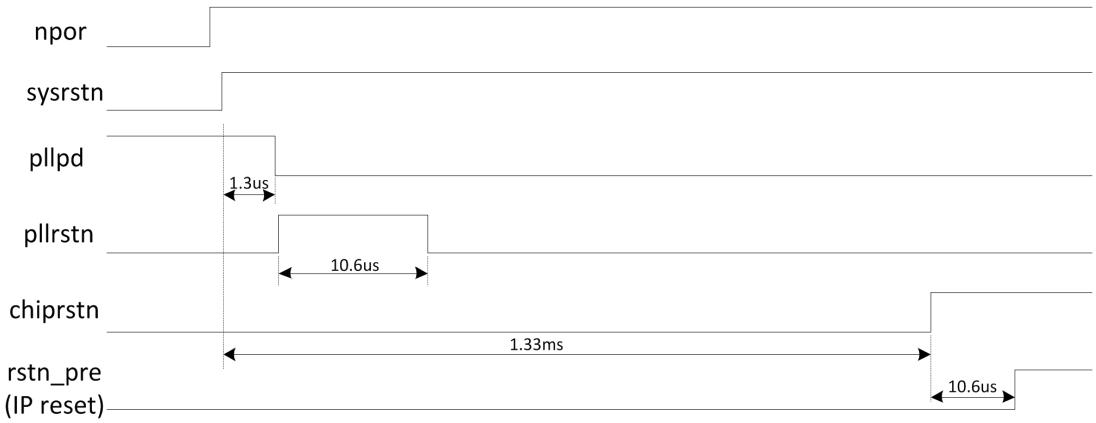


Fig. 5-4 RK3188T reset signals sequence

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3188T has to be below 125ºC.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 5-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

PACKAGE	POWER(W)			
RK3188T	5.15	19.4	11.3	7.0

Note: The testing PCB is base on 6 layers, 208mm x 39 mm, 1 mm Thickness

Rockchip Electronics Co.,Ltd.
No, 18 Building, A District, Fuzhou software park, Fujian, China
Tel: +86-591-83991906 Fax:+86-591-83951833
www.**rock-chips.com**