Chapter 29 Audio Codec

29.1 Overview

The Audio Codec is a capless, low power, high resolution, stereo CODEC solution that employs Sigma-Delta noise-shaping technique.The ADC with 24bit resolution, DAC with 24bit resolution and power amplifier are integrated.

Key Features

- 24 bit DAC with 95dB SNR
- Support DC-coupled capless headphone output
- Support 16Ω to 32Ω headphone output and speaker output
- 24 bit ADC with 92dB SNR
- Support single-ended and differential microphone input and line input
- Automatic Level Control (ALC) for smooth audio recording
- Support Mono, Stereo, 5.1 and 7.1 HiFi channel performance
- Programmable input and output analog gains
- Digital interpolation and decimation filter integrated
- Sampling rate of 8/12/16/24/32/44.1/48/96kHz

29.2 Block Diagram

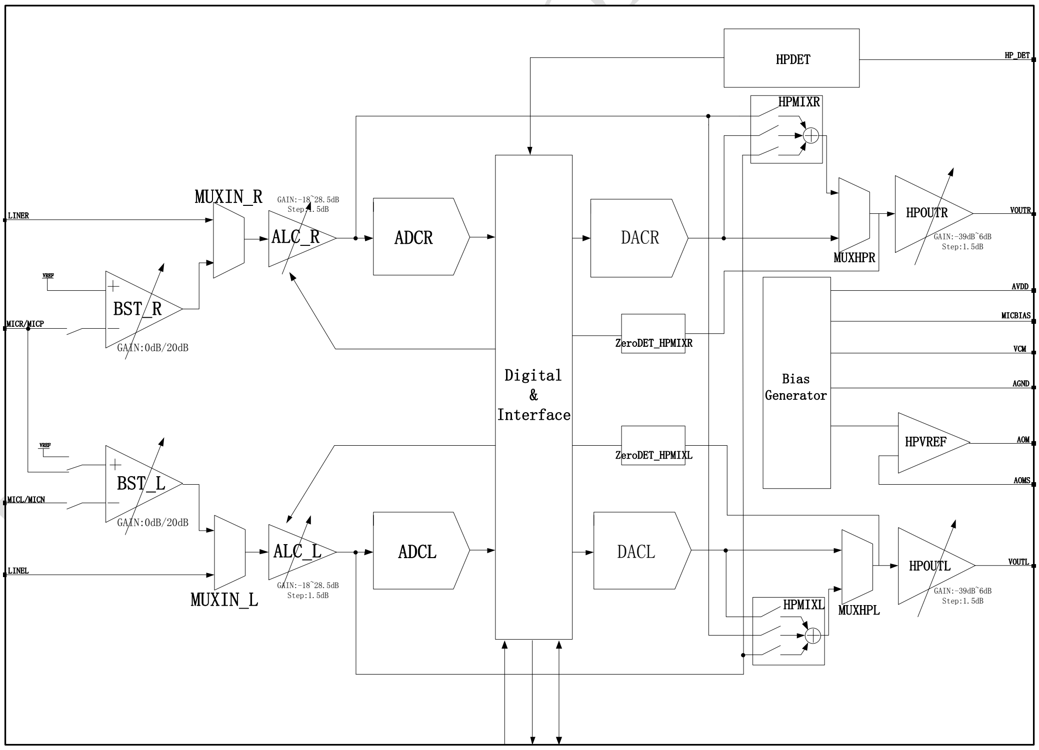

Fig.29-1 Audio Codec Block Diagram

29.3 Electrical Specification

Test conditions: AVDD = 3.3V, DVDD = 1.1V, T_A = 25℃, 1KHz Sine Input, Fs = 48KHz.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Condition						
Analog Supply	AVDD		2.97	3.3	3.63	V
Digital Supply	DVDD		0.99	1.1	1.21	V
Junction Temperature	T_J		-40		125	℃
Microphone Bias						
Bias Voltage	V_{MICB}		0.5* AVDD		0.85* AVDD	V
Bias Current	I_{MICB}				3	mA
Microphone Gain Boost PGA						
Programmable Gain	G_{BST}		0		20	dB
Gain Step Size				20		dB
Input Resistance	R_{IN}	G_{BST}=0dB		83		KΩ
		G_{BST}=20dB		15		KΩ
Input Capacitance	C_{IN}			10		pF
ALC PGA						
Programmable Gain	G_{ALC}		-18		28.5	dB
Gain Step Size				1.5		dB
ADC Input Path (Microphone or Line input to ADC)						
Signal to Noise Ratio	SNR	A-weighted		95		dB
Total Harmonic Distortion	THD	-3dBFS input		-83		dB
Power Supply Rejection	PSRR	1KHz		80		dB
ADC						
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	-3dBFS input		-81		dB
Channel Separation				80		dB
DAC						
Signal to Noise Ratio	SNR	A-weighted		95		dB
Total Harmonic Distortion	THD	-3dBFS output 10KΩ load		-84		dB
Channel Separation				85		dB
Output Driver						
Programmable Gain	G_{DRV}		-39		6	dB
Gain Step Size				1.5		dB
Output Resistance	R_{OUT}			1		KΩ
Output Capacitance	C_{OUT}			20		pF
Power Supply Rejection	PSRR	1KHz		70		dB
Line Output						
Signal to Noise Ratio	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	-3dBFS output 10KΩ load		-84		dB
Headphone Output						
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	16Ω load P_O=20mW		-70		dB
		32Ω load P_O=20mW		-75		dB

Power Consumption						
Standby				0.05		mA
Stereo Recording				6.5		mA
Stereo Playback		Quiescent output		11		mA

29.4 Function description

29.4.1 Digital Interface

The Codec has the I2S PCM interface of audio data stream in for DAC and out for ADC, both of which can be configured in master or slave mode. Different audio data formats are available for different operating modes, which are demonstrated in below table.

Table 29-1 Supported Data Formats in Different Modes

Data Formats	ADC		DAC	
	Master	Slave	Master	Slave
Left Justified	√	×	√	√
Right Justified	√	√	√	√
I^{2}S	√	√	√	√
DSP/PCM mode A	√	√	√	√
DSP/PCM mode B	√	×	√	√

I2S_PCM interface supports five audio data formats: Left Justified mode, Right Justified mode, I^{2}S mode, DSP/PCM mode A and mode B. They are valid when the device operates as a master or slave.

For Left Justified mode, the data format is illustrated in Fig. 29-2.The MSB is valid at the first rising edge of sck after ws transition is done. The other valid bits up to the LSB are transmitted sequentially. Due to varied word length, different sck frequency and sample rate, some unused sck cycles may appear before every ws transition, which means the data in this period is invalid.

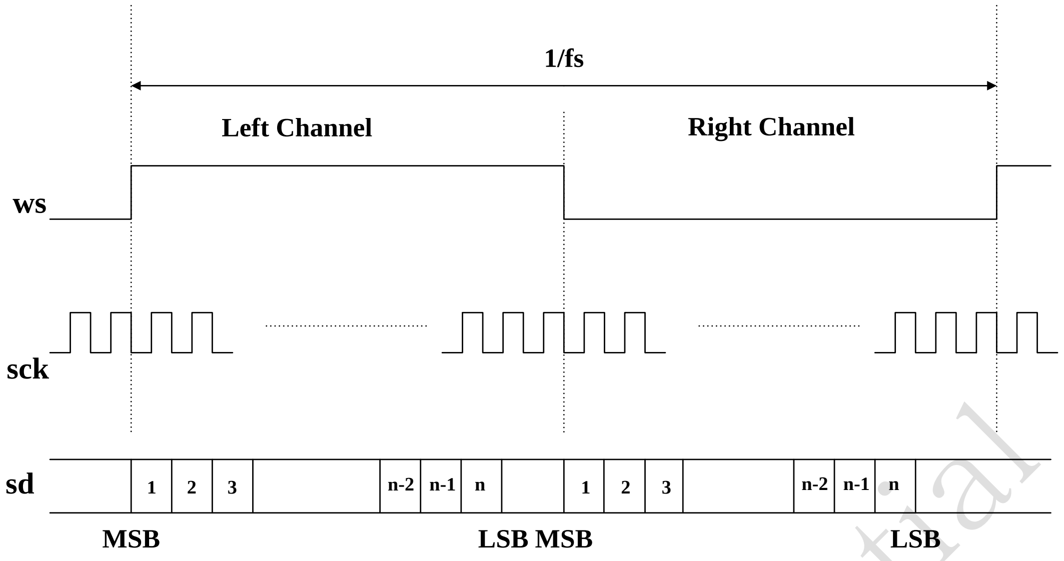

Fig.29-2 Left Justified Mode (assuming n-bit word length)

For Right Justified mode, the data format is shown in Fig. 29-3. The LSB becomes valid at the last rising edge of sck before ws transition is done. As the MSB is transmitted first, the other valid bits up to the MSB are followed in order. Due to varied word length, different sck frequency and sample rate, some unused sck cycles may exist after every ws transition, which means the data in this period is invalid.

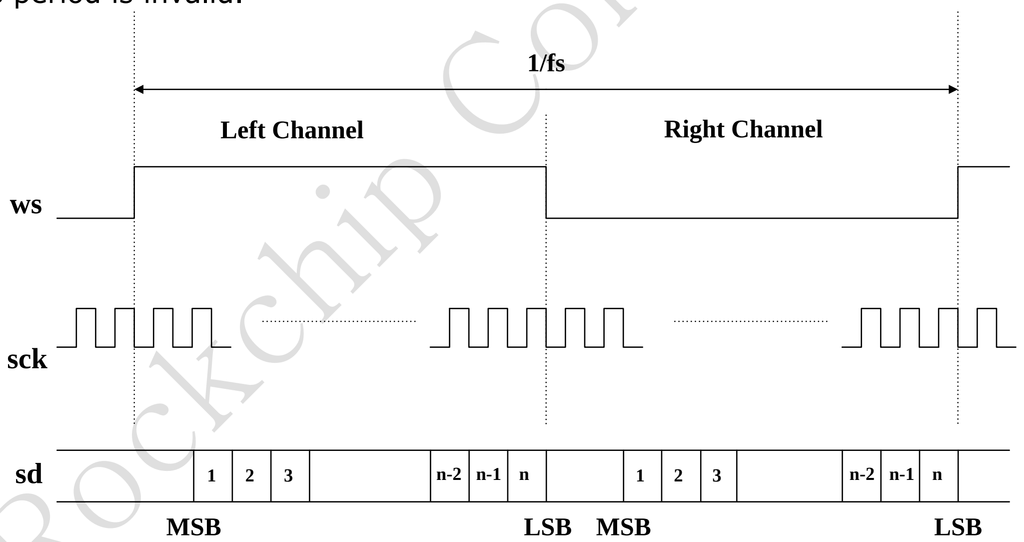

Fig.29-3 Right Justified Mode (assuming n-bit word length)

For I^2S mode, the data format is depicted in Fig. 29-4. The MSB becomes available at the second rising edge of sck when ws transition is done. The other valid bits up to the LSB are transmitted in order. Due to varied word length, different sck frequency and sample rate, some unused sck cycles may appear between the LSB of the current sample and the MSB of the next one, which means the data in this period can be ignored.

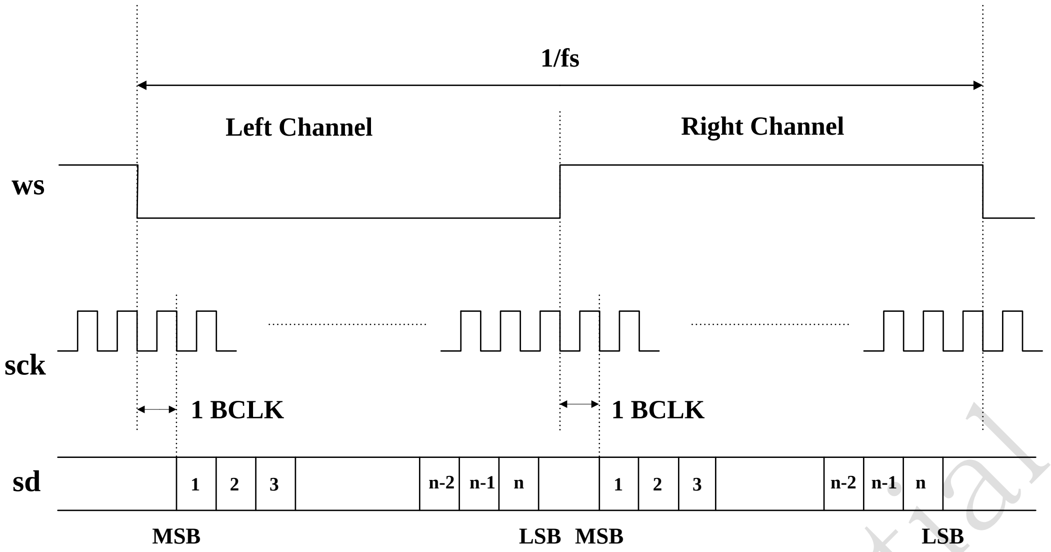

Fig.29-4 I2S Mode (assuming n-bit word length)

For DSP/PCM mode, the left channel data is transmitted first, followed by right channel data. For DSP/PCM mode A/B, the MSB is available at the second and first rising edge of sck after the rising edge of ws respectively, as shown in Fig. 29-5 and Fig.29-6. Based on word length, sck frequency and sample rate, there may be some invalid data between the LSB of the right channel data and the next sample.

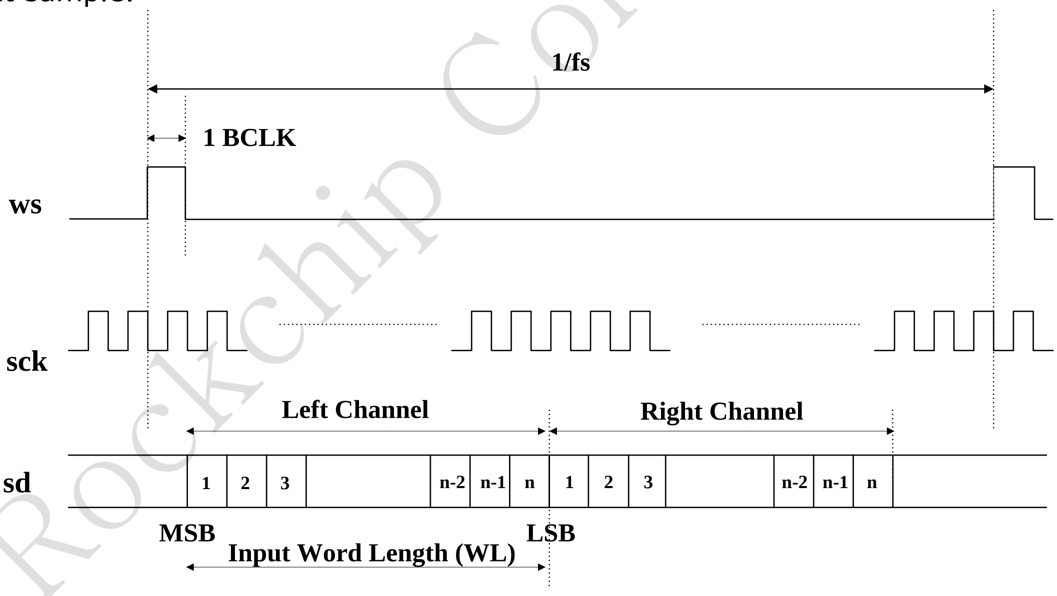

Fig.29-5 DSP/PCM Mode A (assuming n-bit word length)

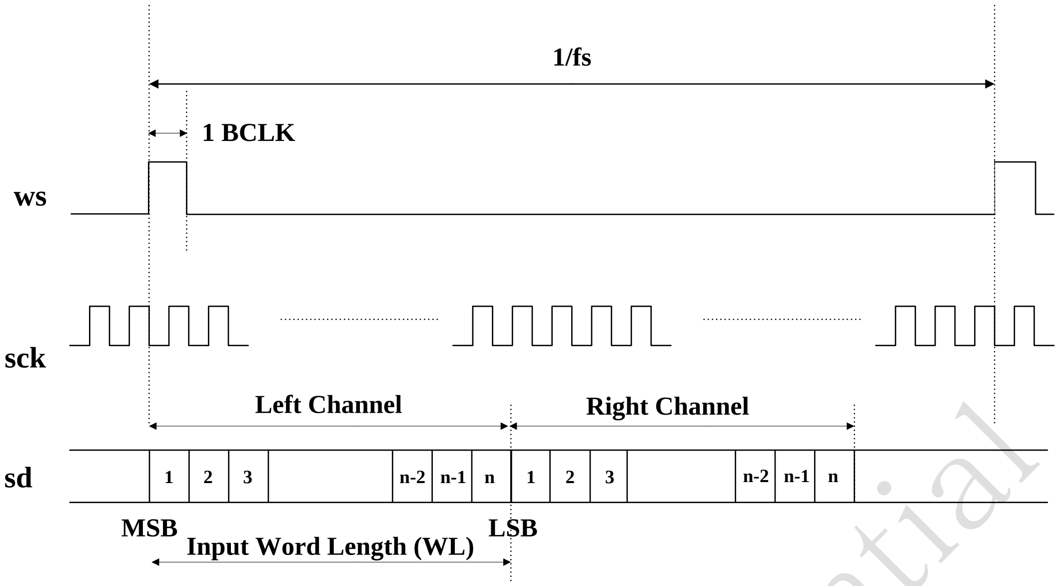

Fig.29-6 DSP/PCM Mode B (assuming n-bit word length)

29.4.2 Analog Interface

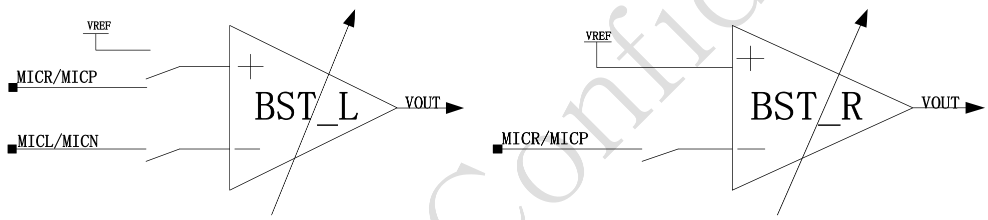

Fig.29-7MicroPhone Input

There are two microphone input channels, left and right channel. In left channel, there are two differential inputs, and they can be configured as either single-ended input or differential inputs by the microphone PGA (BST_L). In right channel, there is only one input, and it is configured as single-ended input by the microphone PGA (BST_R).
In left channel, microphone inputs are MICL and MICR. When working in single-ended configuration, the input signal should be input through MICL.
In right channel, microphone input is MICR.
Microphone PGA has two gains to amplify the input signal, that is, 0dB and +20dB.
There are two line input channels, INL and INR. They are input to left and right channel MUX (MUXIN_L and MUXIN_R), respectively. In each channel, the input MUX can choose line input or microphone PGA output as the input of ALC PGA.
Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.
The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB.
The tuning step is 1.5dB.

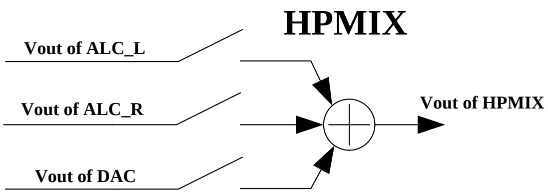

Fig.29-8output mixer

DAC output and ADC input can be mixed by output mixer. There are two output channel mixers, HPMIXL and HPMIXR.

In HPMIXL mixer, output of left channel DAC, output of left channel ALC PGA and output of right channel ALC PGA can be mixed. In HPMIXR mixer, output of right channel DAC, output of left channel ALC PGA and output of right channel ALC PGA can be mixed.

This Codec supports two headphone output configurations. The headphone output can drive 16Ω or 32Ω headphone load either through DC-blocking capacitor or DC-coupled capless configuration.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16Ω headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.

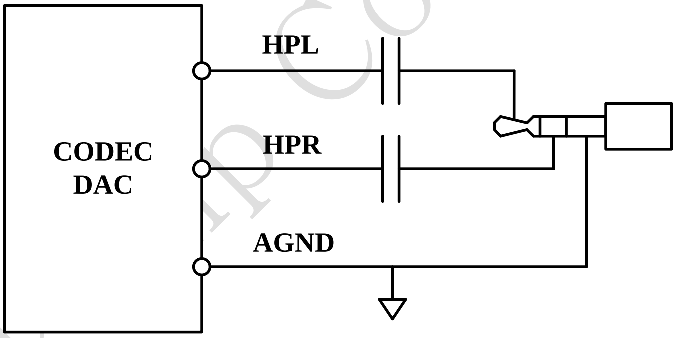

Fig.29-9DC-blocking capacitor

In the DC-coupled capless configuration, shown in following figure, the headphone ground is connected to a virtual ground, AOM. AOM is a DC output driver with a DC voltage of AVDD/2, that is, half of the analog supply. The requirement for DC-blocking capacitor is removed, which can save the cost.

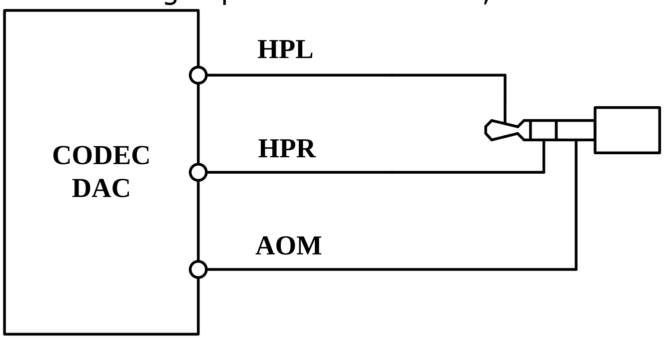

Fig.29-10DC-coupled capless

The headphone driver can choose mixer output or DAC output as input. It has a gain range from -39dB to +6dB with a tuning step of 1.5dB.

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.5*AVDD to 0.85* AVDD with a step of 0.05*AVDD.

29.4.3 Interface Relationship

In broadcasting application, the I2S/PCM1/2 controller is used as a transmitter and audio CODEC is used as a receiver. In recording application, the I2S/PCM1/2 controller is used as a receiver and audio CODEC is used as a transmitter. Either the I2S/PCM1/2 controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.
Fig.29-11 and Fig.29-12 illustrate the relationship between I2S interface and the parallel audio data in ADC and DAC channels.

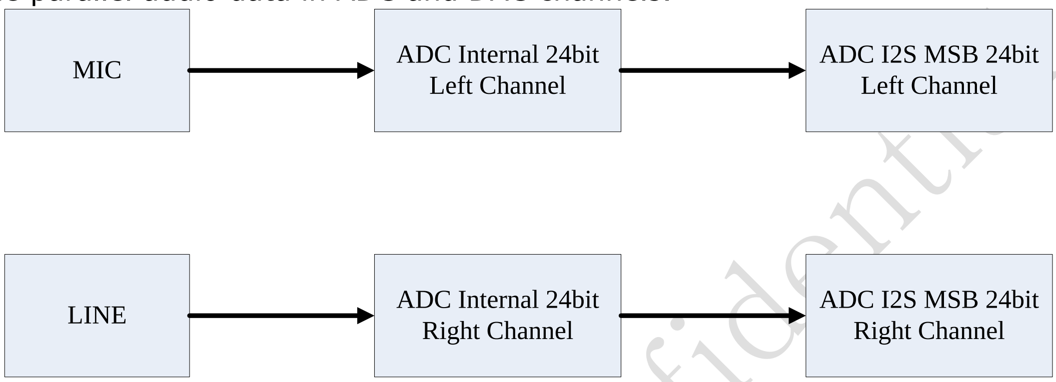

Fig.29-8 ADC Channels Relationship

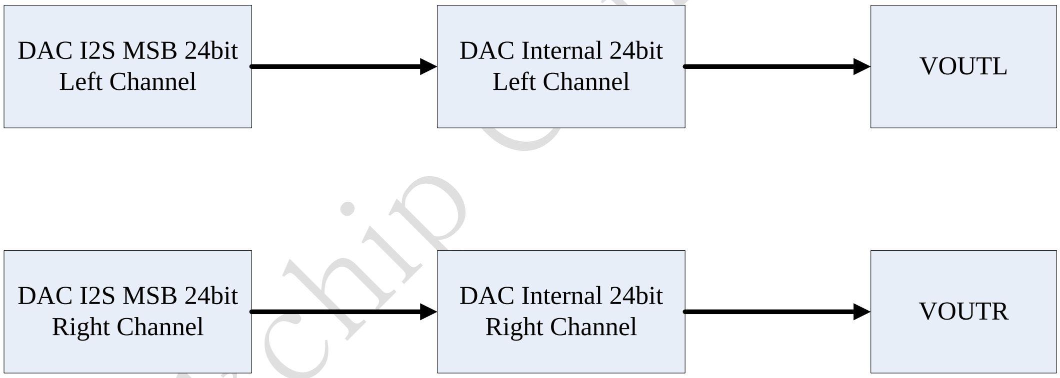

Fig.29-9 DAC Channels Relationship

29.5 Register description

29.5.1 Register Summary

Name	Offset	Size	Reset Value	Description
Codec_REG0	0x0000	W	0x00000003	Codec register 0
Codec_REG2	0x0008	W	0x00000050	Codec register 2
Codec_REG3	0x000c	W	0x0000000e	Codec register 3
Codec_REG4	0x0010	W	0x00000050	Codec register 4
Codec_REG5	0x0014	W	0x0000000e	Codec register 5
Codec_REG34	0x0088	W	0x00000000	Codec register 34
Codec_REG35	0x008c	W	0x00000000	Codec register 35
Codec_REG36	0x0090	W	0x00000044	Codec register 36

Name	Offset	Size	Reset Value	Description
Codec_REG37	0x0094	W	0x0000000c	Codec register 37
Codec_REG38	0x0098	W	0x0000000c	Codec register 38
Codec_REG39	0x009c	W	0x00000000	Codec register 39
Codec_REG40	0x00a0	W	0x00000000	Codec register 40
Codec_REG41	0x00a4	W	0x00000000	Codec register 41
Codec_REG42	0x00a8	W	0x00000000	Codec register 42
Codec_REG43	0x00ac	W	0x00000000	Codec register 43
Codec_REG44	0x00b0	W	0x00000000	Codec register 44
Codec_REG45	0x00b4	W	0x00000000	Codec register 45
Codec_REG46	0x00b8	W	0x00000000	Codec register 46
Codec_REG47	0x00bc	W	0x0000001e	Codec register 47
Codec_REG64	0x00c0	W	0x00000000	Codec register 64
Codec_REG65	0x00c4	W	0x00000046	Codec register 65
Codec_REG66	0x00c8	W	0x00000041	Codec register 66
Codec_REG67	0x00cc	W	0x0000002c	Codec register 67
Codec_REG68	0x00d0	W	0x00000000	Codec register 68
Codec_REG69	0x00d4	W	0x00000026	Codec register 69
Codec_REG70	0x00d8	W	0x00000040	Codec register 70
Codec_REG71	0x00dc	W	0x00000036	Codec register 71
Codec_REG72	0x00e0	W	0x00000020	Codec register 72
Codec_REG73	0x00e4	W	0x00000038	Codec register 73

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

29.5.2 Detail Register Description

Codec_REG0
Address: Operational Base + offset (0x0000)
Codec register 0

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	Power reset bypass 0: not 1: bypass
5:2	RO	0x0	reserved
1	RW	0x1	Codec digital core reset This reset only reset the codec data path. 0: reset 1: work
0	RW	0x1	Codec system reset This signal will reset the registers which control all the digital and analog part. 0: reset 1: work

Codec_REG2
Address: Operational Base + offset (0x0008)
Codec register 2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	ADC LRC Polarity 0: normal 0: reversal
6:5	RW	0x2	ADC Valid Word Length in one 1/2Frame 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
4:3	RW	0x2	ADC mode 11: PCM Mode 10: I2S Mode 01: Left Justified Mode 00: Right Justified Mode Note. Same word length in 1/2frame and valid data is not supported in Right Justified Mode. For example, 32/24 or 24/20 is supported, but 32/32 or 24/24 is not supported. (1/2frame length/valid data length)
2	RO	0x0	reserved
1	RW	0x0	ADC Left-Right SWAP 0: normal 1: swap
0	RW	0x0	ADC type 1: Mono 0: Stereo

Codec_REG3
Address: Operational Base + offset (0x000c)
Codec register 3

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	ADC and DAC I2S Mode Select 0: slave mode 1: master mode
3:2	RW	0x3	ADC 1/2Frame Word Length 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
1	RW	0x1	ADC Reset 0: reset 1: work
0	RW	0x0	ADC Bit Clock Polarity 0: normal 1: reversal

Codec_REG4
Address: Operational Base + offset (0x0010)
Codec register 4

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	DAC LRC Polarity 0: normal 1: reversal
6:5	RW	0x2	DAC Valid Word Length in one 1/2Frame 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
4:3	RW	0x2	DAC mode 11: PCM Mode 10: I2S Mode 01: Left Justified Mode 00: Right Justified Mode Note. Same word length in 1/2frame and valid data is not supported in Right Justified Mode. For example, 32/24 or 24/20 is supported, but 32/32 or 24/24 is not supported. (1/2frame length/valid data length)
2	RW	0x0	DAC Left-Right SWAP 0: normal 1: swap
1:0	RO	0x0	reserved

Codec_REG5
Address: Operational Base + offset (0x0014)
Codec register 5

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x3	DAC 1/2Frame Word Length 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
1	RW	0x1	DAC reset 0: reset 1: work
0	RW	0x0	DAC Bit Clock polarity 0: normal 1: reversal

Codec_REG34
Address: Operational Base + offset (0x0088)
Codec register 34

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	The enable signal of current source for ADC 0: Stop Working 1: Work

Bit	Attr	Reset Value	Description
6	RW	0x0	The enable signal of MIC bias voltage (MICBIAS) buffer 0: Stop Working 1: Work
5	RW	0x0	The enable signal of the ADCL input zero-crossing detection module: 0: Stop Working ,output 0 electrical level 1: Work
4	RW	0x0	The enable signal of the ADCR input zero-crossing detection module: 0: Stop Working ,output 0 electrical level 1: Work
3	RO	0x0	reserved
2:0	RW	0x0	The level range control signal of MIC bias voltage (MICBIAS) 000 .0*VREF 111 .7*VREF Step .1*VREF VREF = AVDD/2

Codec_REG35
Address: Operational Base + offset (0x008c)
Codec register 35

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	The enable signal of BST_L module 0: Stop Working 1: Work
5	RW	0x0	The gain control of BST_L module 1: 20dB 0: 0dB
4	RW	0x0	The mute signal of BST_L module 0: Mute 1: Work
3	RO	0x0	reserved
2	RW	0x0	The enable signal of BST_R module 0: Stop Working 1: Work
1	RW	0x0	The gain control of BST_R module 1: 20dB 0: 0dB
0	RW	0x0	The mute signal of BST_R module 0: Mute 1: Work

Codec_REG36
Address: Operational Base + offset (0x0090)
Codec register 36

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x1	The signal to select input of MUXINL module 00/11: don't select 10: select INL 01: select output of BST_L module
5	RW	0x0	The enable signal of ALCL module 0: Stop Working 1: Work
4	RW	0x0	The mute signal of ALCL module 0: Mute 1: Work
3:2	RW	0x1	The signal to select input of MUXINR module 00/11:don't select 10:Select INR 01:Select output of BST_R module
1	RW	0x0	The enable signal of ALCR module 0: Stop Working 1: Work
0	RW	0x0	The mute signal of ALCR module 0: Mute 1: Work

Codec_REG37
Address: Operational Base + offset (0x0094)
Codec register 37

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	The signal to select the input mode of BST_L module 1: Single-ended input 0: Full differential input
4:0	RW	0x0c	The gain control of ALC_L module 00000: -18dB 01100: 0dB 11111 : 28.5dB Step: 1.5dB

Codec_REG38
Address: Operational Base + offset (0x0098)
Codec register 38

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0c	The gain control of ALC_R module 00000: -18dB 01100: 0dB 11111: 28.5dB Step: 1.5dB

Codec_REG39
Address: Operational Base + offset (0x009c)

Codec register 39

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	The enable signal of reference Voltage buffer for left ADC PATH 0: Stop working 1: Work
6	RW	0x0	The enable signal of CLOCK for ADCL module 0: Set to logic "1" 1: Work
5	RW	0x0	The enable signal of Amplifier in ADCL module 0: Stop working all amplifier 1: Work
4	RW	0x0	The reset signal of different levels integrator in ADCL module 0: Work 1: Clear
3	RW	0x0	The enable signal of reference Voltage buffer for right ADC PATH 0: Stop working 1: Work
2	RW	0x0	The enable signal of CLOCK for ADCR module 0: Set to logic "1" 1: Work
1	RW	0x0	The enable signal of Amplifier in ADCR module 0: Stop working all amplifier 1: Work
0	RW	0x0	The reset signal of different levels integrator in ADCR module 0: Work 1: Clear

Codec_REG40

Address: Operational Base + offset (0x00a0)

Codec register 40

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	The enable signal of current source for CODEC DAC 0: Stop Working 1: Work
5	RW	0x0	The enable signal of reference Voltage buffer for left DAC PATH 0: Stop Working 1: Work
4	RW	0x0	The enable signal of zero-crossing detection module for VOUTL: 0: Stop Working ,output 0 electrical level 1: Work

Bit	Attr	Reset Value	Description
3	RW	0x0	The enable signal of module to detect earphone 0: Don't detect，output logic "0" 1: Detect
2	RO	0x0	reserved
1	RW	0x0	The enable signal of reference Voltage buffer for right DAC PATH 0: Stop working 1: Work
0	RW	0x0	The enable signal of zero-crossing detection module for VOUTR: 0: Stop Working ,output 0 electrical level 1: Work

Codec_REG41
Address: Operational Base + offset (0x00a4)
Codec register 41

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	The enable signal of high and low reference Voltage buffer for DACL module 0: stop working 1: Work
6	RW	0x0	The enable signal of CLOCK module for DACL 0: Set CLOCK to logic "1" 1: Work
5	RW	0x0	The enable signal of DACL module 0: Stop work 1: Work
4	RW	0x0	The Initial signal of DACL module 0: Initialization 1: Work
3	RW	0x0	The enable signal of high and low reference Voltage buffer for DACL module 0: Stop working 1: Work
2	RW	0x0	The power down signal of the ADCR input zero-crossing detection: 1: Power down ,output 0 electrical level 0: Work
1	RW	0x0	The enable signal of DACR module 0: Stop work 1: Work
0	RW	0x0	The Initial signal of DACR module 0: Initialization 1: Work

Codec_REG42
Address: Operational Base + offset (0x00a8)
Codec register 42

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	The enable signal of HPMIXL module 0: Stop work 1: Work
5	RW	0x0	The Initial1 signal of HPMIXL module 0: Initialization 1: Work
4	RW	0x0	The Initial2 signal of HPMIXL module 0: Initialization 1: Work
3	RO	0x0	reserved
2	RW	0x0	The enable signal of HPMIXR module 0: Stop work 1: Work
1	RW	0x0	The Initial1 signal of HPMIXR module 0: Initialization 1: Work
0	RW	0x0	The Initial2 signal of HPMIXR module 0: Initialization 1: Work

Codec_REG43
Address: Operational Base + offset (0x00ac)
Codec register 43

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	The bypass signal of HPMIXL module 1: Bypass HPMIXL 0: Don't bypass
6:4	RW	0x0	The signal to select input of HPMIXL module: [6]: select output of ALCL module 0: Don't select 1: Select [5]: select output of ALCR module 0: Don't select 1: Select [4]: select output of DACL module 0: Don't select 1: Select
3	RW	0x0	The bypass signal of HPMIXR module 1: Bypass HPMIXR 0: Don't bypass

Bit	Attr	Reset Value	Description
2:0	RW	0x0	The signal to select input of HPMIXR module: [2]: select output of ALCL module 0: Don't select 1: Select [1]: select output of ALCR module 0: Don't select 1: Select [0]: select output of DACR module 0: Don't select 1: Select

Codec_REG44
Address: Operational Base + offset (0x00b0)
Codec register 44

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	The enable signal of HPOUTL module 0: Stop working 1: Work
6	RW	0x0	The Initial signal of HPOUTL module 0: Initialization 1: Work
5	RW	0x0	The mute signal of HPOUTL module 0: Mute 1: Work
4	RW	0x0	The enable signal of HPOUTR module 0: Stop working 1: Work
3	RW	0x0	The Initial signal of HPOUTR module 0: Initialization 1: Work
2	RW	0x0	The mute signal of HPOUTR module 0: MUTE 1: Work
1	RW	0x0	The enable signal of HPVREF module 0: Stop working 1: Work
0	RW	0x0	The Initial signal of HPVREF module 0: Initialization 1: Work

Codec_REG45
Address: Operational Base + offset (0x00b4)
Codec register 45

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	The signal to select gain of HPOUTL module: 00000: -39dB 11010: 6dB 11111: 0dB Step: 1.5dB

Codec_REG46
Address: Operational Base + offset (0x00b8)
Codec register 46

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	The signal to select gain of HPOUTR module: 00000: -39dB 11010: 6dB 11111: 0dB Step: 1.5dB

Codec_REG47
Address: Operational Base + offset (0x00bc)
Codec register 47

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	The signal to select current to Precharge/Discharge [4]: Select 10uA 0: Select 1: Don't select [3]: Select current I0 0: Select 1: Don't select [2]: Select current 2* I0 0: Select 1: Don't select [1]: Select current 4*I0 0: Select 1: Don't select [0]: Select current 4*I0 0: Select 1: Don't select I0 is a reference current, the current can stack
4:0	RW	0x1e	Field0000 Abstract Field0000 Description

Codec_REG64
Address: Operational Base + offset (0x00c0)
Codec register 64

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	Choose the method to control the gain attack 0 : Normal way 1 : Jack way
5:4	RW	0x0	There are foure methods to generate the control signals 00: Normal way 01: Jack way 1 10: Jack way 2 11: Jack way 3 This register is used to according to the physical truth to choose the method to generate the control signals.
3:0	RW	0x0	AGC hold time before gain is increased in normal mode. 0000: 0ms 0001: 2ms 0010: 4ms 0011: 8ms 0100: 16ms 0101: 32ms 0110: 64ms 0111:128ms 1000:256ms 1001:512ms 1010: 1 s 1011~1111:0ms

Codec_REG65
Address: Operational Base + offset (0x00c4)
Codec register 65

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x4	Decay (gain ramp-up) time Normal MODE(reg_agc_mde =0) 0000:500us 0001:1ms 0010:2ms 0011:4ms 0100:8ms 0101:16ms 0110:32ms 0111:64ms 1000:128ms 1001:256ms 1010:512ms 1001~1111:512ms

Bit	Attr	Reset Value	Description
3:0	RW	0x6	Attack (gain ramp-down) Time Noraml MODE(reg_agc_mde =0) 0000:125us 0001:250us 0010:500us 0011:1ms 0100:2ms 0101:4ms 0110:8ms 0111:16ms 1000:32ms 1001:64ms 1010:128ms 1011~1111:125us Noraml MODE(reg_agc_mde =1) 0000:32us 0001:64us 0010:125us 0011:250us 0100:500us 0101:1ms 0110:2ms 0111:4ms 1000:8ms 1001:16ms 1010:32ms 1011~1111:32us

Codec_REG66
Address: Operational Base + offset (0x00c8)
Codec register 66

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	Determines the AGC mode of operation 0:AGC mode(normal mode) 1:Limiter mode
6	RW	0x1	AGC users zero cross enable 0:Disabled 1:Enabled, the AGC gain will update at zero cross enable
5	RW	0x0	When in the limiter mode, the low amplitude signal will recovery in two modes: 0:The gain will recovery to the value of the reg_pga_lvol 1:The gain will recovery to the gain at the moment that the mode changes from AGC to Limiter.
4	RW	0x0	When the amplitude of the signal is more than 87.5% of the Full scale, use this signal to control the fast decrement: 0:Disabled 1:Enabled

Bit	Attr	Reset Value	Description
3	RW	0x0	AGC noise gate function enable 0:Disabled 1:Enabled
2:0	RW	0x1	AGC noise gate threhold 000:-39dB 001:-45dB 010:-51dB 011:-57dB 100:-63dB 101:-69dB 110:-75dB 111:-81dB

Codec_REG67
Address: Operational Base + offset (0x00cc)
Codec register 67

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Left channel input PGA zero cross enable 0:Update gain when gain register changes. 1:Update gain on 1st zero cross after gain register write.
4:0	RW	0x0c	Left channel input PGA gain 00000:-18dB 00001:-16.5dB 00010:-15dB ...... n: (1.5xn-18)dB ...... 01100:0dB 01101:+1.5dB 01110:+3dB ...... 11111:+28.5dB

Codec_REG68
Address: Operational Base + offset (0x00d0)
Codec register 68

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Slow clock enabled used for the zero cross timeout.

Bit	Attr	Reset Value	Description
2:0	RW	0x0	Approximate sample rate 000:96kHz 001:48kHz 010:44.1kHz 011:32kHz 100:24kHz 101:16kHz 110:12kHz 111: 8kHz 110~111:reserved

Codec_REG69
Address: Operational Base + offset (0x00d4)
Codec register 69

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x26	agc_max_l The low 8 bits of the AGC maximum level

Codec_REG70
Address: Operational Base + offset (0x00d8)
Codec register 70

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x40	agc_max_h The high 8 bits of the AGC maximum level

Codec_REG71
Address: Operational Base + offset (0x00dc)
Codec register 71

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x36	agc_min_l The low 8 bits of the AGC minimum level

Codec_REG72
Address: Operational Base + offset (0x00e0)
Codec register 72

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x20	agc_min_h The high 8 bits of the AGC minimum lelel

Codec_REG73
Address: Operational Base + offset (0x00e4)
Codec register 73

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	agcf AGC function select 0: AGC function off 1: AGC function enable
5:3	RW	0x7	pga_maxg Set maximum gain of PGA 000:-13.5dB 001:- 7.5dB 010:- 1.5dB 011:+ 4.5dB 100:+10.5dB 101:+16.5dB 110:+22.5dB 111:+28.5dB
2:0	RW	0x0	pga_ming Set minimum gain of PGA 000:-18dB 001:-12dB 010:- 6dB 011: 0dB 100:+ 6dB 101:+12dB 110:+18dB 111:+24dB

29.6 Application Note