Chapter 25 USB Host 2.0

25.1 Overview

USB HOST2.0 supports Non_OTG Host functions and is fully compliant with USB2.0 specification, and support high-speed (480Mbps), full-speed (12Mbps), low-speed (1.5Mbps) transfer. It is optimized for point-to-point applications (no hub, direct connection to device).

25.1.1 Features

- Compliant with the USB2.0 Specification
- Operates in Non_OTG Host mode
- Operates in High-Speed, Full-Speed, Low-speed mode
- Support 16 channels in host mode
- Built-in one 840x35 bits FIFO
- Internal DMA with no scatter/gather function

25.2 Block Diagram

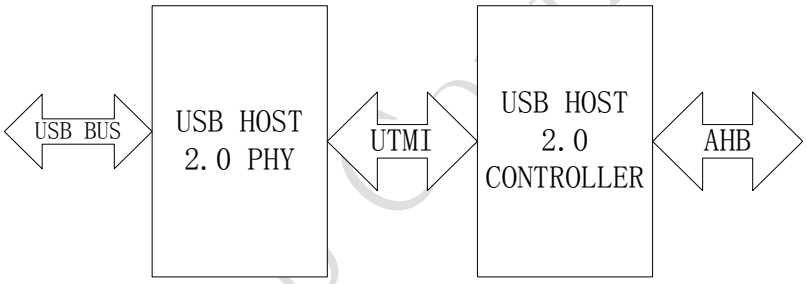

Fig. 25-1 USB HOST 2.0 Architecture

Fig.25-1 shows the architecture of USB HOST 2.0. It is broken up into two separate units: USB HOST 2.0 controller and USB HOST 2.0 PHY. The two units are interconnected with 16-bits UTMI interface.

25.3 USB Host2.0 Controller

Much the same as USB OTG with no Device Mode supported. See Chapter OTG for more information.

Note: There is another option for host controller: EHCI-OHCI Controller. Please refer to <DesignWare Cores USB 2.0 Host-AHB Controller > for details

25.4 USB Host2.0 PHY

Much the same as USB OTG with no Device Mode supported. See Chapter OTG for more information.

USB Host2.0 PHY doesn't support UART-DEBUG function.

25.5 Register Description

The Registers are much the same as OTG with no Device-Mode supported. The

registers of Device are not available. See Chapter OTG for more information.

25.6 Interface description

Table 25-1 USB HOST 2.0 Interface Description

Module Pin	Direction	Pad Name	pinmux
VSSA	AG	VSSA	-
VCCA3P3	AP	VCCA3P3	-
VCCCORE1P1	AP	VCCCORE1P1	-
USB1PN	A	USB0PN	-
USBRBIAS	A	USBRBIAS	-
USB1PP	A	USB0PP	-

***Note**: **A**—Analog pad ; **AP**—Analog power; **AG**—Analog ground ;**DP**—Digital power ;**DG**–Digital ground;*

25.7 Application Note

See Chapter OTG for more information.

25.7.1 Reset a port

CRU_SOFTRST4_CON contains HOST reset signal description. Please refer to "Chapter CRU" for more details.

25.7.2 Relative GRF Registers

GRF_UOC0_CON0 ~ GRF_UOC0_CON2 is OTG PHY register.
GRF_UOC0_CON3 is OTG Controller register.
Please refer to "Chapter GRF" for more details.