Chapter 24 HDMI Tx

24.1 Overview

HDMI TX is fully compliant with HDMI 1.4a specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMI TX consists of one HMDI transmitter controller and one HMDI transmitter PHY.

24.1.1 Features

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4a/b/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 a/b spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as additional feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- Library delivered to support all major EDA tools and detailed guide to integrate into pad ring/BGA bumps
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug
- 3.3V high speed I/O and 1.2V/1.0V core power supply

24.2 Block Diagram

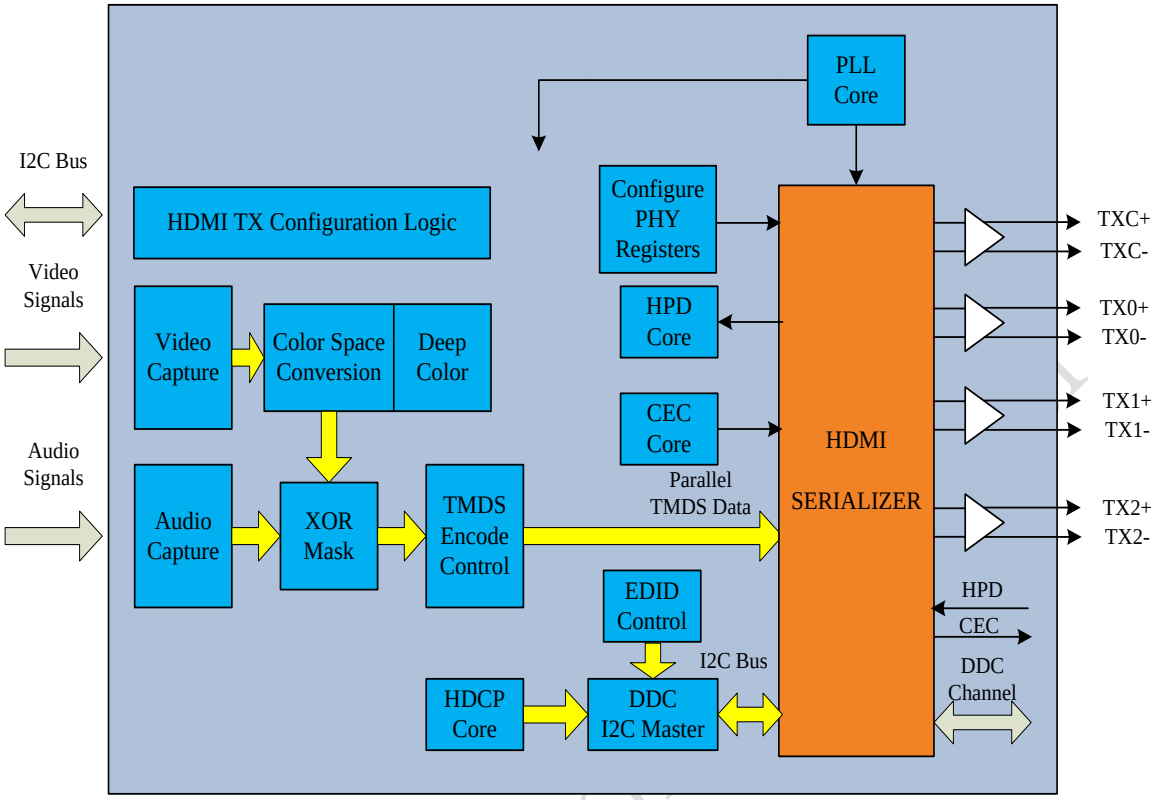

Fig. 24-1 HDMI TX Block Diagram

24.3 Function description

24.3.1 Video Data Processing

The video processing contain video format timings, pixel encodings(RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

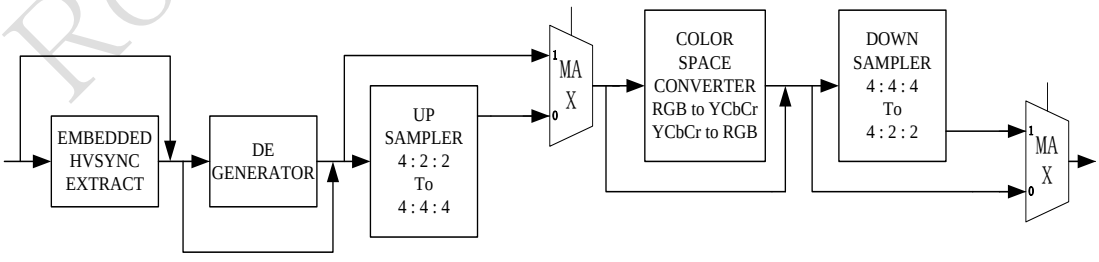

Fig. 24-2 HDMI Video Data Processing

The input video pixels can be encoded in either RGB, YCBCR 4:4:4 or YCBCR 4:2:2 formats by Color Space Conversion block.

The input Video data can have a pixel size of 24, 30, 36 or 48 bits. The deep

color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

The following interface timing diagram outlines the Video interface signal format. 24 bit data (we also support 36 bit data for deep color) in RGB can be captured by the rising edge of VCLK with 1ns setup time and 1ns hold time requirements. Control signals such DE and VSync/HSync/FSync going with the same timing relationship.

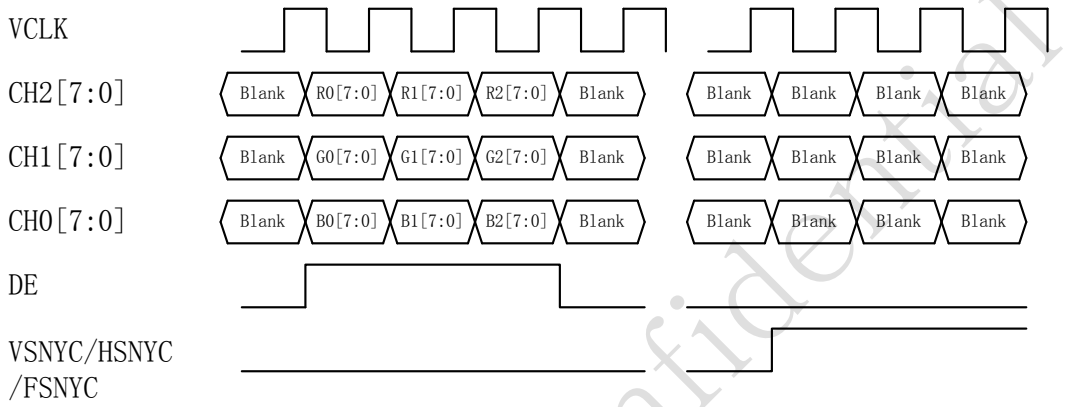

Fig. 24-3HDMI Video Processing Timing

6. Video Data Capture Logic

HDMI TX support input video data related format table is listed below.

Table 24-1HDMI Supported Input Video Formats

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
RGB	4:4:4	Separate	8	24
RGB	4:4:4	Separate	10	30
RGB	4:4:4	Separate	12	36
YCbCr	4:4:4	Separate	8	24
YCbCr	4:4:4	Separate	10	30
YCbCr	4:4:4	Separate	12	36
YCbCr	4:2:2	Separate	8	16
YCbCr	4:2:2	Separate	10	20
YCbCr	4:2:2	Separate	12	24
YCbCr	4:4:4	Embedded	8	24
YCbCr	4:4:4	Embedded	10	30
YCbCr	4:4:4	Embedded	12	36
YCbCr	4:2:2	Embedded	8	16
YCbCr	4:2:2	Embedded	10	20

YCbCr	4:2:2	Embedded	12	24

7. Embedded Sync Extraction Module

The module is used to extract Vsync and Hsync signals from input video data stream such as ITU656 format. With setting the relative registers, this functional module can extract correct video sync signals for later processblock using.

8. Data Enable (DE) Generator

HDMI Transmitter has DE signal generator by incoming HSYNCs, VSYNCs and Video clock. External DE is optional and selected by appropriate register settings. This feature is particularly useful when interfacing to MPEG decoders that do not provide a specific DE output signal.

9. Color Space Conversion

HDMI Transmitter Color space conversion (CSC) is available to interface for several MPEG decoders like with YCbCr-only outputs, and to provide full DVI backwards compatibility.

The function of this module is to perform color space conversion functionality as listed below.

(1). Convert RGB input Video data to YCbCr Video data.

(2). Convert YCbCr input Video data to RGB Video data.

(3). upsample for YCbCr 4:2:2 to YCbCr 4:4:4

(4). downsample for YCbCr 4:4:4 to YCbCr 4:2:2

24.3.2 Audio Data Processing

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks

The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.

The scheme of audio processing as shown in the figure below:

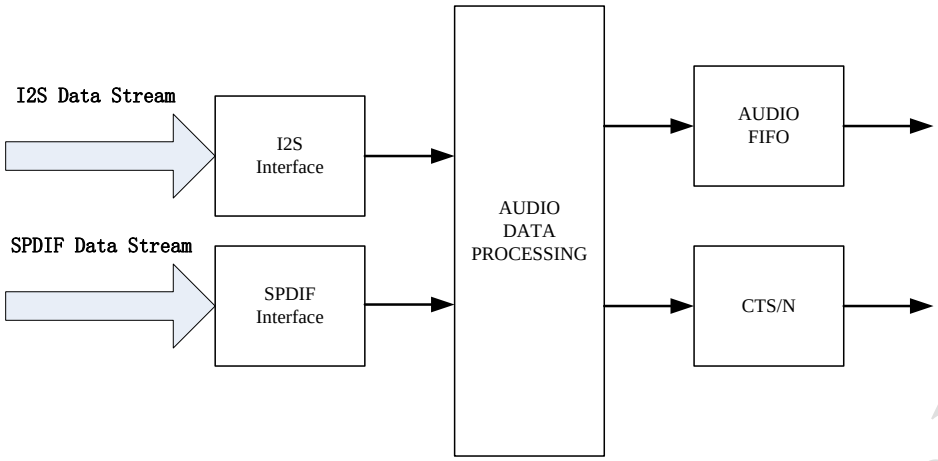

Fig. 24-4HDMI Audio Data Processing Diagram

1. I2S

The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link.Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table 24-2HDMI TX I2S 2Channel Audio Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1440x480i/1440x576i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 24-3HDMI TX I2S 8 Channel Audio Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
1440x480i/1440x576i	Yes	Yes	Yes	Yes	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2. SPDIF

The function of this module is to implement SPDIF audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. SPDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. SPDIF input supports audio sampling rates from 32 to 192 KHz. The following shows the SPDIF audio formats that are supported for each of the video formats

Table 24-4HDMI SPDIF Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	No	No
1440x480i/1440x576i	Yes	Yes	Yes	Yes	Yes	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

3. Audio Sample Clock Capture and Regeneration

Audio data being carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sinkthen re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be.

$$128 \cdot fS = fTMDS\_clock \cdot N / CTS.$$

The scheme of the Audio Sample Clock Capture and Regeneration as shown below:

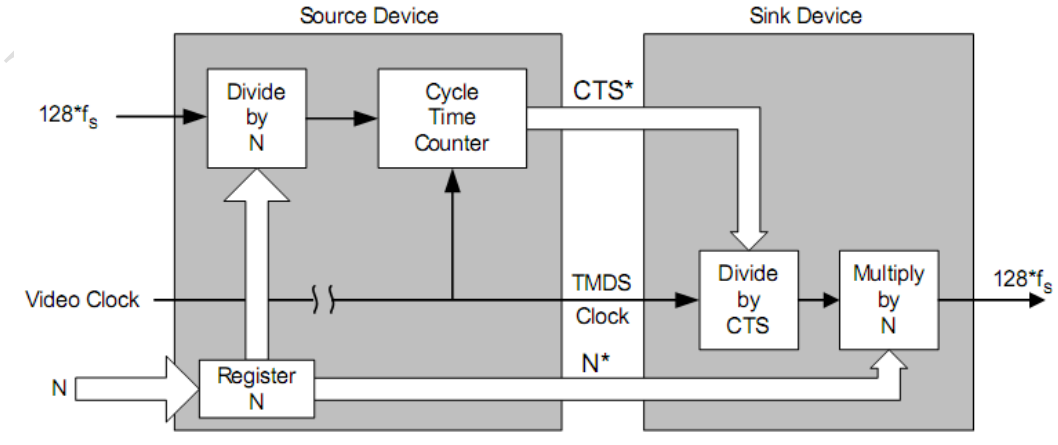

Fig. 24-5HDMI Audio Clock Regeneration Model

24.3.3 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HMDI TransmitterController has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

24.3.4 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

24.3.5 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

24.3.6 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

24.3.7 TMDS encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data.

HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

24.3.8 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

24.3.9 Optional Lipsync

HDMI sinks and repeaters can now declare audio/video latency information in their EDIDs. HDMI TX can read the audio/video latency information from HDMI sinks, than it may delay audio or video to compensate for latencies in downstream devices.

24.4 Register Description

24.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
HDMI_reg00	0x0000	B	0x67	Register00
HDMI_reg01	0x0004	B	0x01	Register01
HDMI_reg02	0x0008	B	0x30	Register02
HDMI_reg04	0x0010	B	0x08	Register04
HDMI_reg05	0x0014	B	0x00	Register05
HDMI_reg08	0x0020	B	0x00	Register08
HDMI_reg09	0x0024	B	0x00	Register09
HDMI_reg0a	0x0028	B	0x00	Register0a
HDMI_reg0b	0x002c	B	0x00	Register0b
HDMI_reg0c	0x0030	B	0x00	Register0c
HDMI_reg0d	0x0034	B	0x00	Register0d
HDMI_reg0e	0x0038	B	0x00	Register0e
HDMI_reg0f	0x003c	B	0x00	Register0f
HDMI_reg10	0x0040	B	0x00	Register10
HDMI_reg11	0x0044	B	0x00	Register11
HDMI_reg12	0x0048	B	0x00	Register12
HDMI_reg13	0x004c	B	0x00	Register13
HDMI_reg14	0x0050	B	0x00	Register14
HDMI_reg15	0x0054	B	0x00	Register15
HDMI_reg35	0x00d4	B	0x01	Register35
HDMI_reg37	0x00dc	B	0x00	Register37
HDMI_reg38	0x00e0	B	0x3c	Register38
HDMI_reg39	0x00e4	B	0x00	Register39
HDMI_reg3a	0x00e8	B	0x00	Register3a
HDMI_reg3f	0x00fc	B	0x00	Register3f
HDMI_reg40	0x0100	B	0x18	Register40
HDMI_reg41	0x0104	B	0x00	Register41
HDMI_reg45	0x0114	B	0x00	Register45
HDMI_reg46	0x0118	B	0x00	Register46
HDMI_reg47	0x011c	B	0x00	Register47
HDMI_reg4a	0x0128	B	0x00	Register4a
HDMI_reg4b	0x012c	B	0x40	Register4b
HDMI_reg4c	0x0130	B	0x00	Register4c
HDMI_reg4d	0x0134	B	0x00	Register4d
HDMI_reg4e	0x0138	B	0x00	Register4e
HDMI_reg4f	0x013c	B	0x00	Register4f
HDMI_reg50	0x0140	B	0x00	Register50
HDMI_reg52	0x0148	B	0x12	Register52
HDMI_reg53	0x014c	B	0x04	Register53
HDMI_reg57	0x015c	B	0x20	Register57
HDMI_reg58	0x0160	B	0x00	Register58
HDMI_reg63	0x018c	B	0x26	Register63
HDMI_reg65	0x0194	B	0x00	Register65
HDMI_reg66	0x0198	B	0x00	Register66
HDMI_reg67	0x019c	B	0x00	Register67
HDMI_reg68	0x01a0	B	0x00	Register68

Name	Offset	Size	Reset Value	Description
HDMI_reg69	0x01a4	B	0x00	Register69
HDMI_reg6a	0x01a8	B	0x00	Register6a
HDMI_reg6c	0x01b0	B	0x00	Register6c
HDMI_reg95	0x0254	B	0x00	Register95
HDMI_reg96	0x0258	B	0x00	Register96
HDMI_reg97	0x025c	B	0x00	Register97
HDMI_reg98	0x0260	B	0x03	Register98
HDMI_reg9c	0x0270	B	0x00	Register9c
HDMI_reg9e	0x0278	B	0x01	Register9e
HDMI_reg9f	0x027c	B	0x00	Register9f
HDMI_rega0	0x0280	B	0x00	Registera0
HDMI_rega1	0x0284	B	0x00	Registera1
HDMI_rega2	0x0288	B	0x00	Registera2
HDMI_rega3	0x028c	B	0x00	Registera3
HDMI_rega4	0x0290	B	0x00	Registera4
HDMI_rega5	0x0294	B	0x00	Registera5
HDMI_rega6	0x0298	B	0x00	Registera6
HDMI_rega7	0x029c	B	0x00	Registera7
HDMI_rega8	0x02a0	B	0x00	Registera8
HDMI_rega9	0x02a4	B	0x00	Registera9
HDMI_regaa	0x02a8	B	0x00	Registeraa
HDMI_regab	0x02ac	B	0x00	Registerab
HDMI_regac	0x02b0	B	0x00	Registerac
HDMI_regad	0x02b4	B	0x00	Registerad
HDMI_regae	0x02b8	B	0x00	Registerae
HDMI_regaf	0x02bc	B	0x00	Registeraf
HDMI_regb0	0x02c0	B	0x00	Registerb0
HDMI_regb1	0x02c4	B	0x00	Registerb1
HDMI_regb2	0x02c8	B	0x00	Registerb2
HDMI_regb3	0x02cc	B	0x00	Registerb3
HDMI_regb4	0x02d0	B	0x00	Registerb4
HDMI_regb5	0x02d4	B	0x00	Registerb5
HDMI_regb6	0x02d8	B	0x00	Registerb6
HDMI_regb7	0x02dc	B	0x00	Registerb7
HDMI_regb8	0x02e0	B	0x00	Registerb8
HDMI_regb9	0x02e4	B	0x00	Registerb9
HDMI_regba	0x02e8	B	0x00	Registerba
HDMI_regbb	0x02ec	B	0x00	Registerbb
HDMI_regbc	0x02f0	B	0x00	Registerbc
HDMI_regbd	0x02f4	B	0x00	Registerbd
HDMI_regbe	0x02f8	B	0x00	Registerbe
HDMI_regc0	0x0300	B	0xc0	Registerc0
HDMI_regc1	0x0304	B	0x00	Registerc1
HDMI_regc2	0x0308	B	0x78	Registerc2
HDMI_regc3	0x030c	B	0x00	Registerc3
HDMI_regc4	0x0310	B	0x00	Registerc4
HDMI_regc5	0x0314	B	0x00	Registerc5
HDMI_regc8	0x0320	B	0x00	Registerc8
HDMI_regc9	0x0324	B	0x50	Registerc9

Name	Offset	Size	Reset Value	Description
HDMI_regce	0x0338	B	0x01	Registerce
HDMI_regd0	0x0340	B	0x00	Registerd0
HDMI_regd1	0x0344	B	0x00	Registerd1
HDMI_regd2	0x0348	B	0x00	Registerd2
HDMI_regd3	0x034c	B	0x00	Registerd3
HDMI_regd4	0x0350	B	0x03	Registerd4
HDMI_regd5	0x0354	B	0x09	Registerd5
HDMI_regd6	0x0358	B	0x03	Registerd6
HDMI_regd7	0x035c	B	0x00	Registed7
HDMI_regd8	0x0360	B	0xff	Registerd8
HDMI_regd9	0x0364	B	0xff	Registerd9
HDMI_regda	0x0368	B	0x00	Registerda
HDMI_regdb	0x036c	B	0x00	Registerdb
HDMI_regdc	0x0370	B	0xd0	Registerdc
HDMI_regdd	0x0374	B	0x20	Registerdd
HDMI_regde	0x0378	B	0x00	Registerde
HDMI_rege0	0x0380	B	0x23	Registere0
HDMI_rege1	0x0384	B	0x0f	Registere1
HDMI_rege2	0x0388	B	0xaa	Registere2
HDMI_rege3	0x038c	B	0x0f	Registere3
HDMI_rege7	0x039c	B	0x1e	Registere7
HDMI_rege8	0x03a0	B	0x00	Registere8
HDMI_reged	0x03b4	B	0x03	Registered

24.4.2 Detail Register Description

HDMI_reg00

Address: Operational Base + offset (0x0000)

Register00

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6	RW	0x1	sw_reset_ana Soft reset for analog part 1'b0: reset 1'b1: not
5	RW	0x1	sw_reset_dig Soft reset for digital part 1'b0: reset 1'b1: not
4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	vclk_inv Vclk invert select 1'b0: not invert 1'b1: invert
2	RW	0x0	reserved
1	RW	0x1	pd_dig System power down for digital function 1'b0: not 1'b1: power down
0	RW	0x1	interrupt_polarity Interrupt polarity 1'b1: Active High 1'b0: Active low

HDMI_reg01
Address: Operational Base + offset (0x0004)
Register01

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:1	RW	0x0	input_video_fmt Input video format 3'b000: RGB and YCbCr 4:4:4 3'b101: DDR RGB 4:4:4 or YCbCr 4:4:4 3'b110: DDR YCbCr 4:2:2
0	RW	0x1	de_sel DE select 1'b0: internal DE 1'b1: external DE

HDMI_reg02
Address: Operational Base + offset (0x0008)
Register02

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:6	RW	0x0	video_output_fmt Video output format 2'b00: RGB 4:4:4 2'b01: YCbCr 4:4:4 2'b10: YCbCr 4:2:2
5:4	RW	0x3	data_width_422 Data width for 4:2:2 input 2'b00: 12 bits 2'b01: 10 bits 2'b11: 8 bits
3:1	RW	0x0	reserved
0	RW	0x0	Video_in_color_space Video input color space 1'b0: RGB 1'b1: YCbCr

HDMI_reg04
Address: Operational Base + offset (0x0010)
Register04

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x1	sof_sel After 1st SOF(the first edge of the Vsync) for external DE sample 1'b0: after SOF 1'b1: Not
2:1	RW	0x0	reserved
0	RW	0x0	csc_en CSC (Color Space Convert) enable. 1'b0: no CSC 1'b1: enable CSC

HDMI_reg05
Address: Operational Base + offset (0x0014)
Register05

Bit	Attr	Reset Value	Description
7	RW	0x0	clear_avmute Clear avmute

Bit	Attr	Reset Value	Description
6	RW	0x0	set_avmute Set avmute
5:2	RW	0x0	reserved
1	RW	0x0	audio_mute Audio mute
0	RW	0x0	video_black Video black

HDMI_reg08
Address: Operational Base + offset (0x0020)
Register08

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x0	vs_polarity VSYNC polarity 1'b0: Negative 1'b1: Positive
2	RW	0x0	hs_polarity HSYNC polarity 1'b0: Negative 1'b1: Positive
1	RW	0x0	interlace_progressiv_sel Interlace/Progressive 1'b0: Progressive 1'b1: Interlace
0	RW	0x0	ext_video_para_set_en External video parameter setting enable 1'b0: disable 1'b1: enable

HDMI_reg09
Address: Operational Base + offset (0x0024)
Register09

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_total_part1 External horizontal total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0a
Address: Operational Base + offset (0x0028)
Register0a

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	ext_hs_total_part2 External horizontal total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0b
Address: Operational Base + offset (0x002c)
Register0b

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_blank_part1 External horizontal blank part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0c
Address: Operational Base + offset (0x0030)
Register0c

Bit	Attr	Reset Value	Description
7:3	RW	0x0	reserved
2:0	RW	0x0	ext_hs_blank_part2 External horizontal blank part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0d
Address: Operational Base + offset (0x0034)
Register0d

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Ext_hsync_part1 External horizontal hsync part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0e

Address: Operational Base + offset (0x0038)
Register0e

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	Ext_hsync_part2 External horizontal hsync part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0f
Address: Operational Base + offset (0x003c)
Register0f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_sync_part1 External horizontal duration part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg10
Address: Operational Base + offset (0x0040)
Register10

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	ext_hs_sync_part2 External horizontal duration part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg11
Address: Operational Base + offset (0x0044)
Register11

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_vertical_total_part1 External vertical total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg12
Address: Operational Base + offset (0x0048)
Register12

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ext_vertical_total_part2 External vertical total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg13
Address: Operational Base + offset (0x004c)
Register13

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_blank External vertical blank. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg14
Address: Operational Base + offset (0x0050)
Register14

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_vsync External vertical vsync. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg15
Address: Operational Base + offset (0x0054)
Register15

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved
5:0	RW	0x00	ext_vertical_duration External vertical duration. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg35
Address: Operational Base + offset (0x00d4)
Register35

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7	RW	0x0	cts__sel CTS source select 1'b0: internal CTS 1'b1: external CTS
6:5	RW	0x0	reserved
4:3	RW	0x0	audio_type_sel Audio type select 2'b00: I2S 2'b01: S/PDIF
2	RW	0x0	mclk_sel MCLK select
1:0	RW	0x1	mclk_ratio MCLK ratio 2'b00: 128 fs 2'b01: 256 fs 2'b10: 384 fs 2'b11: 512 fs

HDMI_reg37
Address: Operational Base + offset (0x00dc)
Register37

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	sample_freq_sel Sampling frequency for I2S audio 4'b0011: 32 kHz 4'b0000: 44.1 kHz 4'b0010: 48 kHz 4'b1000: 88.2 kHz 4'b1010: 96 kHz 4'b1100: 176.4 kHz 4'b1110: 192 kHz

HDMI_reg38
Address: Operational Base + offset (0x00e0)
Register38

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved

Bit	Attr	Reset Value	Description
5:2	RW	0xf	i2s_sel I2S enable for the four I2S pins 4'b0001: I2S0 4'b0010: I2S1 4'b0100: I2S2 4'b1000: I2S3
1:0	RW	0x0	i2s_fmt I2S format 2'b00: standard I2S mode 2'b01: right-justified I2S mode 2'b10: left-justified I2S mode

HDMI_reg39
Address: Operational Base + offset (0x00e4)
Register39

Bit	Attr	Reset Value	Description
7:6	RW	0x0	audio_channel3_input_sel Audio channel3 input 2'b00: I2S3 2'b01: I2S2 2'b10: I2S1 2'b11: I2S0
5:4	RW	0x0	audio_channel2_input_sel Audio channel2 input 2'b00: I2S2 2'b01: I2S1 2'b10: I2S0 2'b11: I2S3
3:2	RW	0x0	audio_channel1_input_sel Audio channel1 input 2'b00: I2S1 2'b01: I2S0 2'b10: I2S3 2'b11: I2S2
1:0	RW	0x0	audio_channel0_input_sel Audio channel0 input 2'b00: I2S0 2'b01: I2S3 2'b10: I2S2 2'b11: I2S1

HDMI_reg3a
Address: Operational Base + offset (0x00e8)
Register3a

Bit	Attr	Reset Value	Description
7	RW	0x0	lr_swap_ch7_8 Left/Right data swap for ch7/8
6	RW	0x0	lr_swap_ch5_6 Left/Right data swap for ch5/6
5	RW	0x0	lr_swap_ch3_4 Left/Right data swap for ch3/4
4	RW	0x0	lr_swap_ch1_2 Left/Right data swap for ch1/2
3:0	RW	0x0	spdif_sample_freq S/PDIF sampling frequency 4'b0011: 32 kHz. 4'b0000: 44.1 kHz. 4'b0010: 48 kHz. 4'b1000: 88.2 kHz. 4'b1010: 96 kHz. 4'b1100: 176.4 kHz. 4'b1110: 192 kHz.

HDMI_reg3f
Address: Operational Base + offset (0x00fc)
Register3f

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	ncts_part1 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg40
Address: Operational Base + offset (0x0100)
Register40

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x18	ncts_part2 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg41
Address: Operational Base + offset (0x0104)
Register41

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ncts_part3 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg45
Address: Operational Base + offset (0x0114)
Register45

Bit	Attr	Reset Value	Description
7:4	RW	0x00	reserved
3:0	RW	0x00	cts_part3 When use external CTS (reg0x35[7]=1),then set these three regs. CTS = {reg45[3:0], reg46[7:0], reg47[7:0]}

HDMI_reg46
Address: Operational Base + offset (0x0118)
Register46

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cts_part3 When use external CTS (reg0x35[7]=1),then set these three regs. CTS = {reg45[3:0], reg46[7:0], reg47[7:0]}

HDMI_reg47

Address: Operational Base + offset (0x011c)
Register47

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cts_part3 When use external CTS (reg0x35[7]=1),then set these three regs. CTS = {reg45[3:0], reg46[7:0], reg47[7:0]}

HDMI_reg4a
Address: Operational Base + offset (0x0128)
Register4a

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1	RO	0x0	ddc_sda_bus_statue DDC SDA bus status
0	RO	0x0	ddc_scl_bus_statue DDC SCL bus status

HDMI_reg4b
Address: Operational Base + offset (0x012c)
Register4b

Bit	Attr	Reset Value	Description
7:0	RW	0x40	ddc_bus_access_freq_lsb DDC bus access frequency (LSB)

HDMI_reg4c
Address: Operational Base + offset (0x0130)
Register4c

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ddc_bus_access_freq_msb DDC bus access frequency (MSB)

HDMI_reg4d
Address: Operational Base + offset (0x0134)
Register4d

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_segment_pointer EDID segment pointer

HDMI_reg4e

Address: Operational Base + offset (0x0138)
Register4e

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_word_addr EDID word address

HDMI_reg4f
Address: Operational Base + offset (0x013c)
Register4f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_fifo_rd_addr EDID FIFO read address

HDMI_reg50
Address: Operational Base + offset (0x0140)
Register50

Bit	Attr	Reset Value	Description
7:0	RO	0x00	edid_rd_access_window EDID reading access window

HDMI_reg52
Address: Operational Base + offset (0x0148)
Register52

Bit	Attr	Reset Value	Description
7	RW	0x0	authentication_start Authentication start
6	RW	0x0	bksv_not_in_blacklist BKSV is not in the blacklist
5	RW	0x0	bksv_in_blacklist BKSV is in the blacklist
4	RW	0x1	encypte_en current frame encypted en 1'b0: current frame should not be encrypted 1'b1: current frame should be encrypted
3	RW	0x0	authentication_stop Authentication Stop
2	RW	0x0	advanced_mode_sel 1'b0: do not use advanced cipher mode 1'b1: use advanced cipher mode

Bit	Attr	Reset Value	Description
1	RW	0x1	mode_sel mode selection 1'b0: DVI mode 1'b1: HDMI mode
0	RW	0x0	hdcp_reset HDCP reset

HDMI_reg53
Address: Operational Base + offset (0x014c)
Register53

Bit	Attr	Reset Value	Description
7	RW	0x0	disable_127_chk Disable 127 check
6	RW	0x0	skip_bksv_blacklist_chk Skip BKSV blacklist check
5	RW	0x0	pj_chk_en Enable Pj check
4	RW	0x0	disable_dev_num_check Disable device number check
3	RW	0x1	dly_ri_chk Delay Ri check by one clock
2	RW	0x0	use_preset Use preset An value
1:0	RW	0x0	key_comb Key combination

HDMI_reg57
Address: Operational Base + offset (0x015c)
Register57

Bit	Attr	Reset Value	Description
7	RW	0x0	Authenticated_en 1'b0: Authenticated 1'b0: Not authenticated
6	RW	0x0	av_encrypte_en AV content is encrypted enable 1'b0: AV content is not encrypted 1'b1: AV content is encrypted

Bit	Attr	Reset Value	Description
5	RW	0x1	reserved
4	RW	0x0	HDCP_work 1'b0: HDCP is working 1'b1: HDCP is not working
3	RW	0x0	advanced_cipher_en advanced cipher enable 1'b0: Advanced cipher is not enabled 1'b1: Advanced cipher is enabled
2:0	RW	0x0	reserved

HDMI_reg58
Address: Operational Base + offset (0x0160)
Register58

Bit	Attr	Reset Value	Description
7:0	RW	0x00	rx_bcaps_value RX Bcaps value

HDMI_reg63
Address: Operational Base + offset (0x018c)
Register63

Bit	Attr	Reset Value	Description
7:5	RW	0x00	reserved
4:0	RW	0x06	timer_100ms Registers for timer 100ms

HDMI_reg65
Address: Operational Base + offset (0x0194)
Register65

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x0	ddc_channel_no_ack DDC channels no acknowledge
2	RW	0x0	pj_mismatch Pj mismatch
1	RW	0x0	ri_mismatch Ri mismatch
0	RW	0x0	bksv_wrong Bksv is wrong

HDMI_reg66
Address: Operational Base + offset (0x0198)
Register66

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg67
Address: Operational Base + offset (0x019c)
Register67

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg68
Address: Operational Base + offset (0x01a0)
Register68

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg69
Address: Operational Base + offset (0x01a4)
Register69

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg6a
Address: Operational Base + offset (0x01a8)
Register6a

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg6c
Address: Operational Base + offset (0x01b0)
Register6c

Bit	Attr	Reset Value	Description
7:0	RW	0x00	seed_an An seed for generate An

HDMI_reg95
Address: Operational Base + offset (0x0254)
Register95

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_wr_byte_addr HDCP KEY FIFO first write byte num address

HDMI_reg96
Address: Operational Base + offset (0x0258)

Register96

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_rd_byte_addr HDCP KEY FIFO first read byte num address

HDMI_reg97

Address: Operational Base + offset (0x025c)

Register97

Bit	Attr	Reset Value	Description
7:2	RO	0x0	reserved
1	RW	0x0	hdcp_fifo_rd_addr8 HDCP KEY FIFO first read byte num address[8]
0	RW	0x0	hdcp_fifo_wr_addr8 HDCP KEY FIFO first write byte num address[8]

HDMI_reg98

Address: Operational Base + offset (0x0260)

Register98

Bit	Attr	Reset Value	Description
7:0	RW	0x03	hdcp_fifo_wr_rd_addr HDCP KEY FIFO write or read point address

HDMI_reg9c

Address: Operational Base + offset (0x0270)

Register9c

Bit	Attr	Reset Value	Description
7	RW	0x0	general_control_packet General control packet 1'b1:enable 1'b0:disable
6	RW	0x0	mpeg_source_frame_packet MPEG source InfoFrame packet 1'b1:enable 1'b0:disable

Bit	Attr	Reset Value	Description
5	RW	0x0	source_descriptor_frame_packet Source product descriptor InfoFrame packet 1'b1:enable 1'b0:disable
4	RW	0x0	vendor_specific_frame_packet Vendor specific InfoFrame packet 1'b1:enable 1'b0:disable
3	RW	0x0	gamut_metadata_packet Gamut metadata packet 1'b1:enable 1'b0:disable
2	RW	0x0	isrc1_packet ISRC1 packet 1'b1:enable 1'b0:disable
1	RW	0x0	acp_packet ACP packet 1'b1:enable 1'b0:disable
0	RW	0x0	generic_packet Generic packet 1'b1:enable 1'b0:disable

HDMI_reg9e

Address: Operational Base + offset (0x0278)

Register9e

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	auto_checksum_frame Auto checksum for InfoFrame 1'b1:enable 1'b0:disable It enables checksum calculation for any InfoFrame packets by hardware.

HDMI_reg9f
Address: Operational Base + offset (0x027c)
Register9f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	packet_offset packet offset register for 0xa0~0xbe 8'h0: Generic packet 8'h1: ACP packet 8'h2: ISRC1 packet 8'h3: ISRC2 packet 8'h4: Gamut metadata packet 8'h5: Vendor specific InfoFrame 8'h6: AVI InfoFrame 8'h7: Source product descriptor InfoFrame packet 8'h8: Audio InfoFrame packet 8'h9: MPEG source InfoFrame

HDMI_rega0
Address: Operational Base + offset (0x0280)
Registera0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega1
Address: Operational Base + offset (0x0284)
Registera1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega2
Address: Operational Base + offset (0x0288)
Registera2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega3
Address: Operational Base + offset (0x028c)
Registera3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega4
Address: Operational Base + offset (0x0290)
Registera4

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega5
Address: Operational Base + offset (0x0294)
Registera5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega6
Address: Operational Base + offset (0x0298)
Registera6

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega7
Address: Operational Base + offset (0x029c)
Registera7

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega8
Address: Operational Base + offset (0x02a0)
Registera8

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega9
Address: Operational Base + offset (0x02a4)
Registera9

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaa
Address: Operational Base + offset (0x02a8)
Registeraa

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regab
Address: Operational Base + offset (0x02ac)
Registerab

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regac
Address: Operational Base + offset (0x02b0)
Registerac

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regad
Address: Operational Base + offset (0x02b4)
Registerad

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regae
Address: Operational Base + offset (0x02b8)
Registerae

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaf
Address: Operational Base + offset (0x02bc)
Registeraf

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb0
Address: Operational Base + offset (0x02c0)
Registerb0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb1
Address: Operational Base + offset (0x02c4)
Registerb1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb2
Address: Operational Base + offset (0x02c8)
Registerb2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb3
Address: Operational Base + offset (0x02cc)
Registerb3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb4
Address: Operational Base + offset (0x02d0)
Registerb4

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb5
Address: Operational Base + offset (0x02d4)
Registerb5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb6
Address: Operational Base + offset (0x02d8)
Registerb6

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb7
Address: Operational Base + offset (0x02dc)
Registerb7

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb8
Address: Operational Base + offset (0x02e0)
Registerb8

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb9
Address: Operational Base + offset (0x02e4)
Registerb9

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regba
Address: Operational Base + offset (0x02e8)
Registerba

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbb
Address: Operational Base + offset (0x02ec)
Registerbb

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbc
Address: Operational Base + offset (0x02f0)
Registerbc

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbd
Address: Operational Base + offset (0x02f4)
Registerbd

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbe
Address: Operational Base + offset (0x02f8)
Registerbe

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regc0
Address: Operational Base + offset (0x0300)
Registerc0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:0	RW	0x00	mask_int Mask for Interrupt 1'b0: masked 1'b1: not mask [5] Interrupt for active Vsync edge [2] Interrupt for EDID Ready

HDMI_regc1
Address: Operational Base + offset (0x0304)
Registerc1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	int_statu Interrupt status [5] Interrupt for active Vsync edge This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] Interrupt for EDID Ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.

HDMI_regc2
Address: Operational Base + offset (0x0308)
Registerc2

Bit	Attr	Reset Value	Description
7:3	RW	0x0f	int_mask Mask for interrupt: 1'b0:masked 1'b1:not masked [7] for HDCP error [6] for bksv fifo ready [5] for bksv update [4] for authentication success [3] for ready to start authentication
2:0	RW	0x0	reserved

HDMI_regc3
Address: Operational Base + offset (0x030c)
Registerc3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:3	RW	0x00	int_status Interrupt status [7] HDCP error Interrupt This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] bksv fifo ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] bksv update This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] authentication success This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [3] ready to start authentication This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.
2:0	RW	0x0	reserved

HDMI_regc4
Address: Operational Base + offset (0x0310)
Registerc4

Bit	Attr	Reset Value	Description
7	RW	0x00	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	int_mask Mask for interrupt: 1'b0:masked 1'b1:not masked [6] for HDCP authentication M0 ready [5] for first frame arrive [4] for HDCP An ready [3] [2] for HDCP encrypted [1] for HDCP not encrypted (av mute) [0] for HDCP not encrypted (no av mute)

HDMI_regc5

Address: Operational Base + offset (0x0314)

Registerc5

Bit	Attr	Reset Value	Description
7	RW	0x00	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	int_status_group3 Interrupt status Group3 This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] HDCP authentication M0 ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] irst frame arrive This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] HDCP An ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] HDCP encrypted This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [1] HDCP not encrypted (av mute) This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [0] HDCP not encrypted (no av mute) This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.

HDMI_regc8

Address: Operational Base + offset (0x0320)

Registerc8

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7	RO	0x0	hot_plug_pin_status Hot plug pin status 1'b1: Plug in 1'b0: Plug out
6	RO	0x0	reserved
5	RW	0x1	Mask_hpd_int Mask for hot plug detect(HPG) interrupt 1'b0：masked 1'b1：not mask
4:2	RW	0x4	reserved
1	RW	0x0	Int_hpd Interrupt for hot plug detect(HPD) This bit will active when the mask for this bit to be set 1.When interrupt occurs,this bit will be equal to 1. Clear interrupt：write 1 to this bit.
0	RW	0x0	reserved

HDMI_regc9
Address: Operational Base + offset (0x0324)
Registerc9

Bit	Attr	Reset Value	Description
7:6	RW	0x1	video_bist_mode Video BIST mode 2'b00: normal color bar. 2'b01: special color bar. 2'b10: black
5	RW	0x0	flush_en Flush enable. After enable it the screen will flush from color bar to black again and again. 1'b1: enable 1'b0: disable
4	RW	0x1	disable_colorbar_bist_test Disable color bar BIST test 1'b1: disable 1'b0: enable
3:0	RW	0x0	reserved

HDMI_regce

Address: Operational Base + offset (0x0338)
Registerce

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	tmds_channel_sync The synchronization for TMDS channels The synchronization for TMDS channels is automatic after Reset the HDMI. But you can synchronization for TMDS channels manually. The operation for this function is: first send 0 to this bit, then send 1, and keep 1 into this bit.

HDMI_regd0
Address: Operational Base + offset (0x0340)
Registerd0

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6	RW	0x0	modify_start_bit_timing_hisense_tv Modify the start bit timing for Hisense TV 1'b1: Modify the start bit timing for Hisense TV 1'b0: Not modify
5	RW	0x0	reject_rec_cec_broadcast_message Reject receive CEC broadcast message 1'b1: Reject receive CEC broadcast message 1'b0: Not reject
4:3	RW	0x0	reserved
2	RW	0x0	CEC_bus_free_time_cnt_en Enable count CEC bus free time 1'b1: Enable count CEC bus free time 1'b0: Not enable
1	RW	0x0	forbid_receive_cec_message Forbid receive CEC message 1'b1: Forbid receive CEC message 1'b0: Not forbid
0	RW	0x0	start_transmit_cec_message Start transmit CEC message 1'b1: Start transmit CEC message 1'b0: Not start

HDMI_regd1
Address: Operational Base + offset (0x0344)
Registerd1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_rx_tx_data_in_fifo CEC RX/TX data in FIFO

HDMI_regd2
Address: Operational Base + offset (0x0348)
Registerd2

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	wr_cec_tx_data_addr Point address for write CEC TX data

HDMI_regd3
Address: Operational Base + offset (0x034c)
Registerd3

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	cec_rx_data_addr Point address for CEC RX data

HDMI_regd4
Address: Operational Base + offset (0x0350)
Registerd4

Bit	Attr	Reset Value	Description
7:0	RW	0x03	cec_clk_freq CEC working clock frequency register1

HDMI_regd5
Address: Operational Base + offset (0x0354)
Registerd5

Bit	Attr	Reset Value	Description
7:0	RW	0x09	cec_work_clk_freq CEC working clock frequency register1

HDMI_regd6
Address: Operational Base + offset (0x0358)
Registerd6

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	tx_block_length Length of TX blocks

HDMI_regd7
Address: Operational Base + offset (0x035c)
Registed7

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	rx_block_length Length of RX blocks

HDMI_regd8
Address: Operational Base + offset (0x0360)
Registerd8

Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_tx_int_mask Mask for CEC TX Interrupts 1'b0: masked 1'b1: not mask [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regd9
Address: Operational Base + offset (0x0364)
Registerd9

Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_rx_int_mask Mask for CEC RX Interrupts 1'b0: masked 1'b1: not mask [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

HDMI_regda
Address: Operational Base + offset (0x0368)
Registerda

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC TX Interrupts [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regdb
Address: Operational Base + offset (0x036c)
Registerdb

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC RX Interrupts [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

HDMI_regdc
Address: Operational Base + offset (0x0370)
Registerdc

Bit	Attr	Reset Value	Description
7:0	RW	0xd0	signal_free_time_l Signal free time length_L

HDMI_regdd
Address: Operational Base + offset (0x0374)
Registerdd

Bit	Attr	Reset Value	Description
7:0	RW	0x20	signal_free_time_h Signal free time length_H

HDMI_regde
Address: Operational Base + offset (0x0378)
Registerde

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	dev_addr Device logic address

HDMI_rege0
Address: Operational Base + offset (0x0380)
Registere0

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4	RW	0x1	TMDS_clk_sel 1'b0: select TMDS clock from PLL; 1'b1: select TMDS clock generated by serializer
3	RW	0x0	TMDS_phase_sel 1'b0: select default phase for TMDS clock; 1'b1: select synchronized phase for TMDS clock with regard to TMDS data
2	RW	0x0	hdmi_band_gap_pd HDMI Band gap power down. 1:Active
1	RW	0x0	hdmi_pll_pd HDMI PLL power down. 1:Active
0	RW	0x0	tmds_channel_pd TMDS channel power down. 1:Active

HDMI_rege1
Address: Operational Base + offset (0x0384)
Registere1

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x1	clk_channel_driver_en Clock channel driver enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
2:0	RW	0x7	data_channels_driver_en Three data channels driver enable [2]-ch2 [1]-ch1 [0]-ch0 1'b0: disable 1'b1: enable

HDMI_rege2
Address: Operational Base + offset (0x0388)
Registere2

Bit	Attr	Reset Value	Description
7:4	RW	0xa	clk_driver_strength Clock channel main-driver strength 0000~1111: the strength from low to high
3:0	RW	0xa	data_driver_strength Three data channels main-driver strength 0000~1111: the strength from low to high

HDMI_rege3
Address: Operational Base + offset (0x038c)
Registere3

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:4	RW	0x0	pre_emphasis_strength Pre-emphasis strength 000~111: the strength from 0 to high
3:2	RW	0x3	clk_driver_strength Clock channel pre-driver strength Slew rate from low to high 00~11: the strength from low to high
1:0	RW	0x3	data_driver_strength Three data channels pre-driver strength Slew rate from low to high 00~11: the strength from low to high

HDMI_rege7

Address: Operational Base + offset (0x039c)
Registere7

Bit	Attr	Reset Value	Description
7:0	RW	0x78	feedback_dividing_ratio_part1 The value of feedback dividing ratio

HDMI_rege8
Address: Operational Base + offset (0x03a0)
Registere8

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x0	feedback_dividing_ratio_part2 The value of feedback dividing ratio

HDMI_reged
Address: Operational Base + offset (0x03b4)
Registered

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x0c	pre_dividing_ratio The value of pre-dividing ratio

Note1: There are some bits of registers have not description in the registers table above, are reserved for other using, please keep it into default value.

24.5 Interface Description

24.5.1 Video Input Source

In RKaudi, the HDMI TX video source comes from VOP.

24.5.2 Audio Input Source

In RKaudi, the HDMI TX audio source comes from I2S_8CH.

24.6 ApplicationNotes

This chapter describes how to bring up HDMI transmitter in your system. As shown few examples below, these introduce the basically HDMI transmitter application, likes, the Hot Plug Detect, EDID read back, multiple audio format input and different video resolution displaying.

You can easily configure these functions with proper registers value setting by HDMI TX APB BUS.

24.6.1 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Just do the step, reset the HDMI TX.

24.6.2 Hot Plug Detection

Hot Plug Detect is a special feature for HDMI transmitter spying the state on the HDMI port.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The following is a step by step instruction for detecting the hot plug in and out.

Hot Plug in Steps:
Step1: Se nd 0 x63 to register 0x00.
Step2: Plug HDMI receiver in.
Step3: Check the interrupt from signal pin_int.
If the pin_int shows high, that means the HDMI transmitter interrupt have generated.
Step4: Check the interrupt.
Read the bit1 o f the register 0 xc8. If bit1=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. The n s end the 1'b1 to bit1 of register 0xc8to clean up the hot plug interrupt.
Step5: Check if really HDMI receiver plug in.
Read the bit7 of the register 0xc8. If bit7=1'b1 that means hot plug in was really happen, otherwise there is ma y be a glitch o n the HPD port.

Hot Plug out Steps:
Step1: HDMI transmitter at working state.
Step2: Plug HDMI receiver out.
Step3: Check the interrupt from signal pin_int.
If the pin_int shows high, that means the HDMI transmitter interrupt have generated.
Step4: Check the interrupt.
Read the bit1 of the register 0xc8. If bit1=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. The n s end the 1'b1 to bit1 of register 0xc8to clean up the hot plug interrupt.
Step5: Check if really HDMI receiver plug out.
Read the bit7 of the register 0xc8. If bit7=1'b0 that means hot plug out was really happen, otherwise there is ma y be a glitch o n the HPD port.

24.6.3 Reading EDID

Read EDID is a function that can make the HDMI transmitter to read the HDMI receiver's Extended Display Identification Data (EDID) in order to discover the HDMI receiver's configuration and capabilities. HDMI transmitter can choose the appropriate audio and video format for playing and displaying by the HDMI receiver through the use of the EDID. Besides, HDMI transmitter support the reading Enhanced Extended Display Identification Data (E-EDID) if HDMI receiver have this enhanced structure.

The following describes how to read E-EDID through HDMI transmitter. The total

E-EDID is 512bytes data, which is divided into 2 segments. Each segment has 256bytes data. The Read E-EDID function is only read 128bytes data from HDMI receiver at each time. So, you must read 4 times that can read total 512bytes data back.

Prepare read E-EDID512bytes Steps:
Step1: Send 0 x63 to register 0x00.
System power down mode.
Step2: HDMI transmitter detected Hot Plug in.
Step3: Define DDC clock (SCL) frequency Fscl = 100K.
Fscl = Freg_clk/(4*X). X={register 0x4c, register 0x4b}.
Note Freg_clk is the frequency o f the tmds clock.
Assume the tmds clock is 148.5MHz.
Send 0 x73 to register 0x4b, Send 0x01 to register 0x4c.
Step4: Enable EDID Ready interrupt.
Send 0 x04 to register 0xc0
Read E-EDIDsegment 0x00 256bytes Steps:
Step1: Set EDID FIFO initial address.
Send 0x00 to register 0x4f
Step2: Set EDID first word address, read first 128bytes.
Send 0x00 to register 0x4e
Step3: Set EDID segment address.
Send 0x00 to register 0x4d
Step4: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 o f register 0xc1. If bit2 = 1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step5: Read first 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
    Read data from register 0x50.
Step6: Set EDID FIFO initial address again.
Send 0x00 to register 0x4f
Step7: Set EDID first word address, read last 128bytes.
Send 0x80 to register 0x4e
Step8: Set EDID segment address.
Send 0x00 to register 0x4d
Step9: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step10: Read last 128bytes EDID data from EDID FIFO.
    for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.
Read E-EDIDsegment 0x01 256bytes Steps:
Step1: Set EDID FIFO initial address.
Send 0x00 to register 0x4f
Step2: Set EDID first word address, read first 128bytes.
Send 0x00 to register 0x4e
Step3: Set EDID segment address.
Send 0x01 to register 0x4d
Step4: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 =1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.

Step5: Read first 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.
Step6: Set EDID FIFO initial address again.
Send 0x00 to register 0x4f
Step7: Set EDID first word address, read last 128bytes.
Send 0x80 to register 0x4e
Step8: Set EDID segment address.
Send 0x01 to register 0x4d
Step9: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 =1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step10: Read last 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.

Note: The segment address must be sent at each time when read 128bytes E-EDID data.

24.6.4 Audio input configuration

HDMI transmitteraudio support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 48K.

The following describes how to configure audio input format into I2S input with 2 channels and the sample rate is 44.1K.

Audio input requirement:

SD0 input (2 Channels I2S input)
WS (fs) = 44.1 KHz
SCK = 64fs
MCLK = 256fs

Configure Audio Input Format Steps:

Ste p1: Select I2S input.
Send 0 x01 to register 0x35
Step2: Select SD0 input.
Send 0 x04 to register 0x38
Step3: Select N/CTS for sample rate = 44.1 KHz.
Send 0 x18 to register 0x40
Send 0x80 to register 0x41

The following describes how to configure audio input format into I2S input with 8 channels and the sample rate is 44.1K.

Audio input requirement:

SD[3 :0] input (8 C ha nnels I2S input)
WS (fs) = 44.1 KHz
SCK = 64fs
MCLK = 256fs

Configure Audio Input Format Steps :

Step1: Select I2S input.
Send 0x01 to register 0x35
Step2: Select SD[3:0] input.
Send 0x3c to register 0x38
Send 0x00 to register 0x39
Step3: Select N/CTS for sample rate = 44.1 KHz.
Send 0x18 to register 0x40
Send 0x80 to register 0x41

24.6.5 Video input configuration

HDMI transmitter support RGB/YCbCr 24/30/36bit video input with different resolution. The default video format is RGB24bit input at resolution of 1080P@60. The following describes how to configure video input format into RGB24bit input at resolution of 480P@60, 720P@60 or 1080P@60.

VOP dclk cannot get invert.

Video input requirement:

24bit RGB 4:4:4 Source.
Resolution is 480P@60, 720P@60 or 1080P@60.

Configure Video Input Format Steps:

Step1: Select configure for video format.
Send 0x06 to register 0x9f
Step2: Configure the AVI info to HDMI RX.
Send 0x82 to register 0xa0 //HB0
Send 0x02 to register 0xa1 //HB1
Send 0x0d to register 0xa2 //HB3
Send 0x00 to register 0xa3 //PB0: checksum is auto set, needn't set this register
Send 0x00 to register 0xa4 //PB1
Send 0x08 to register 0xa5 //PB2
Send 0x70 to register 0xa6 //PB3
Send 0x10 to register 0xa7 //PB4: VID 1920*1080P@60
Send 0x40 to register 0xa8 //PB5
Note: Select correct VID for displaying.
Send 0x02 to register 0xa7 for 720*480P@60.
Send 0x04 to register 0xa7 for 1280*720P@60.
Send 0x05 to register 0xa7 for 1920*1080I@60.
Send 0x10 to register 0xa7 for 1920*1080P@60.
Send 0x11 to register 0xa7 for 720*576P@50.
Send 0x13 to register 0xa7 for 1280*720P@50.
Send 0x14 to register 0xa7 for 1920*1080I@50.
Send 0 x1 f to register 0xa7 for 1920*1080P@50.

The detail configuration for AVI information, please refer to the HDMI specification (8.2.1) and CEA-861-D (6.3).

24.6.6 Low Power Mode

HDMI Transmitter can be configured into Low Power Mode at special customer works mode. The following is a step by step instruction to describe how to configure our HDMI Transmitter into this mode.

Low Power Enter Steps:

Step1:HDMI Transmitter working.
Step2: Low Power analog module.
Send 0x00 to register 0xe1.//Drive disable
Send 0x17 to register 0xe0.
Step3: Assign pin_vclk = 1'b0 or 1'b1.

Low Power Quit Steps:

Step1: Reset system by pin_rst_n.
Ste p2: Wait Hot Plug.
Step3: Read EDID.
Step4: Active vclk through p in_vclk
Step5: Bring up analog module.
Send 0x15 to register 0xe0. //PLL power on
Send 0x14 to register 0xe0. //TX power on
Send 0x10 to register 0xe0. //BG power on
Send 0 x0f to register 0xe1. //driver enable
Step6: Configuration mode reg at addr 0x00 if needed.
Step7: Configuration Video format if needed.
Step8: Configuration Audio format if needed.
Stap9: Configuration mode reg, power on digital part and select tmds_clk for configuration.
Send 0 x61 to register 0x00.
Stap10: Synchronize analog module.
Send 0x00 to register 0xce.
Send 0x01 to register 0xce.

24.6.7 CEC OPERATION

The CEC line is used for high-level user control of HDMI-connected devices.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

The following is a step by step instruction for CEC TX operations and CEC RXoperations.

CEC TX steps

(Send the Command : Standby (0x36) for example)
Step1: Set logic address for CEC (logic address = 1).
Send 0x01 to register 0xde.
Step2: Configure the divide numbers for internal reference clock.
Send 0 x03 to register 0xd4 and 0x09 to register 0 xd5. See Note1 for details.
Step3: Configure the value for signal free time counter.
Send 0xd0 to register 0xdc and 0x20 to register 0xdd. See Note2 for details.
Step4: Configure point address for write CEC TX data.
Send 0x00 to register 0xd2.
Step5: Configure TX data FIFO (the Command o f Standby).
Send 0 x01 to register 0xd1, then, send 0x36 to register 0xd1.
The data 0x01 is for the Header Block, in which the high 4bits is for the initiator, the low 4bits is for the destination. The data 0x36 is for the Data Block, it indicate the command for standby.
Step6: Configure TX data length of this packet. The length is 2.

Send 0x02 to register 0xd6.
Step7: Enable count CEC b us free time.
Send 0x04 to register 0xd0.
Step8: Waiting 16.8ms+4 us for CEC bus free.
I f Interrupt happened for CEC line free time not satisfied. You should change to receive coming data from opposite. After this you can do CEC TX steps again.
(Note that the time for 16.8ms+4us should be compute by MCU itself)
Step9: Begin TX.
Send 0x05 to register 0xd0.
Step10: Waiting and c he ck interrupt o f C EC TX do ne.
Waiting the interrupt, the n, read the value of register 0xda, if the value is 0x08 that means CEC command was transmitted successfully. At last, send 0 x08 to register 0xda to clear up this interrupt.

CEC RX steps:

Step1: Set logic address for CEC (logic address = 1).
Send 0x01 to register 0xde.
Step2: Configure the divide numbers for internal reference clock. See Note1 for details.
Send 0 x03 to register 0xd4 and 0x09 to re gis ter 0 xd5.
Step3: Configure the point address fo r CEC RX data.
Send 0x00 to register 0xd3.
Step4: Waiting CEC TX send CEC packet to o ur HDMI Transmitter, then check interrupt of CEC.Read the value of register 0xdb, if the value is 0x80, thatmeans CEC command was received successfully. Then send 0x80 to register 0xdb to clear up this interrupt.
Step5: Read the RX packet le ngth.
Read the value of the register 0xd7.
Step6: Read the received CEC packet.
Read the value of the register 0 xd1 according to the RX packet length. If the length is 2, please read twice from the register 0xd1.

***Note1**: The system clock (Default value Fsys = 20MHz from pin_sys_clk), registe r 0xd4 and 0xd5 are used to configure the CEC logic to generate a reference clock (Fref=0.5 MHz, Tref = 2us), which is us e d to control t he CEC signal's generation. The following is the formula for generating reference clock 0.5MHz.*
Fref = Fsys / ((register 0xd4 + 1)(register 0xd5 + 1)). Under the default 20MHz system clock, the values of register 0xd4 and 0xd5 are 0x03 and 0x09.*
***Note2**: Before attempting to transmit or re-transmit a frame, a device shall ensure that the CEC line has be e n inactive for a number of bit periods . For example , the signal free time is 7*2.4ms=16.8ms (the bit time is 2.4 ms). According to the 16.8ms/2us = {register 0xdd, register 0xdc}, so the register 0xdd=0x20 and register 0xdc= 0xd0.*

24.6.8 HDCP OPERATION

HDCP is designed to protect the transmission of Audiovisual Content between an HDCP Transmitter and an HDCP Receiver. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

The following is a step by step instruction for HDCP operation.

HDCP operation steps（skip BKSV black list check）:
Example Condition:Video Format : 1920x1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.
Send 0x61 to register 0x00.

Step2: Write HDCP transmitter's Akey to the chip.**See Note1 for details.**

```
for(i =0; i <= 39 ; i = i+ 1 )
   begin
   hdcp_wdata_temp = akey[i];
    for ( j=0 ; j < 7   ; j = j + 1 )
      begin
      Send hdcp_wdata_temp[7:0] to register 0x98;
      hdcp_wdata_temp = hdcp_wdata_temp >>8;
      end
   end
```

Step3: Write HDCP transmitter's AKSV1 to the chip.**See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv1
for (i = 0, i<5, i = i + 1)
begin
     Send hdcp_wdata_temp[7:0] to register 0x98;
     hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step4: Write HDCP transmitter's AKSV2 to the chip.**See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i<5, i = i + 1)
begin
     Send hdcp_wdata_temp[7:0] to register 0x98;
     hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01,that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency.**See Note2 for details.**

Send 0x73 to register 0x4b.

Send 0x01 to register 0x4c.

Step7: Configure the HDCP function.

Send 0x77 to register 0x53.

Step8: Open the mask for HDCP interrupt.

Send 0xff to register 0xc2.

Send 0xff to register 0xc4.

Step9: Start the HDCP authentication.

Send 0x96 to register 0x52.

Step10: Checking HDCP interrupt.

Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authenticationwas successfully finished.

HDCP operation steps（not skip BKSV black list check）:

Example Condition: Video Format : 1920x1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.

Send 0x01 to register 0x00.

Step2: Write HDCP transmitter's Akey to the chip.**See Note1 for details.**

```
for(i =0; i <= 39 ; i = i+ 1 )
   begin
   hdcp_wdata_temp = akey[i];
    for ( j=0 ; j < 7   ; j = j + 1 )
      begin
      Send hdcp_wdata_temp[7:0] to register 0x98;
```

```
        hdcp_wdata_temp = hdcp_wdata_temp >>8;
        end
    end
```

Step3: Write HDCP transmitter's AKSV1 to the chip.**See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv1
for (i = 0, i<5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step4: Write HDCP transmitter's AKSV2 to the chip.**See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i<5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01,that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency.**See Note2 for details.**

Send 0x73 to register 0x4b.

Send 0x01 to register 0x4c.

Step7: Configure the HDCP function.

Send 0x37 to register 0x53(do not skip the BKSV blacklist check).

Step8: Open the mask for HDCP interrupt.

Send 0xff to register 0xc2.

Send 0xff to register 0xc4.

Step9: Start the HDCP authentication.

Send 0x96 to register 0x52.

Step10: Check the BKSV.

Wait for INT from registerc3 bit5(bksv_update),than read register66~register6a for BKSV values to check whether the BKSV is in the revocation list. If the BKSV is not in the revocation list, write 1 to register52 bit6(bksv_pass) , and authentication will continue. Else if the BKSV is in the revocation list, write 1 to register52 bit5(bksv_fail), and authentication will stop.

Step11: Checking HDCP interrupt.

Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authenticationwas successfully finished.

Note1: For HDCP's akey and KSV write, use the TEST KEYS in HDCP specification for example

```
akey[0]=56'h4da4588f131e69;
akey[1]=56'h1f823558e65009;
akey[2]=56'h8a6a47abb9980d;
akey[3]=56'hf3181b52cbc5ca;
akey[4]=56'hfb147f6896d8b4;
akey[5]=56'he08bc978488f81;
akey[6]=56'ha0d064c8112c41;
akey[7]=56'hb39d5a28242044;
akey[8]=56'hb928b2bdad566b;
akey[9]=56'h91a47b4a6ce4f6;
```

```
akey[10] =56'h5600f8205e9d58;
akey[11] =56'h8c7fb706ee3fa0;
akey[12] =56'hc02d8c9d7cbc28;
akey[13] =56'h561261e54b9f05;
akey[14] =56'h74f0de8ccac1cb;
akey[15] =56'h3bb8f60efcdb6a;
akey[16] =56'ha02bbb16b22fd7;
akey[17] =56'h482f8e46785498;
akey[18] =56'h66ae2562274738;
akey[19] =56'h3d4952a323ddf2;
akey[20] =56'he2d231767b3a54;
akey[21] =56'h4d581aede66125;
akey[22] =56'h326082bf7b22f7;
akey[23] =56'hf61b463530ce6b;
akey[24] =56'h360409f0d7976b;
akey[25] =56'ha1e105618d49f9;
akey[26] =56'hc98e9dd1053406;
akey[27] =56'h20c36794426190;
akey[28] =56'h964451ceac4fc3;
akey[29] =56'h3e904504e18c8a;
akey[30] =56'h290010579c2dfc;
akey[31] =56'hd7943b69e5b180;
akey[32] =56'h54c7ea5bdd7b43;
akey[33] =56'h74fb5887c790ba;
akey[34] =56'h935cfa364e1de0;
akey[35] =56'h03075e159a11ae;
akey[36] =56'h05d3408a78fb01;
akey[37] =56'h0059a5d7a04db3;
akey[38] =56'h373b634a2c9e40;
akey[39] =56'h2573bbb4562041;

pre_ksv1 = 40'hb70361f714;
pre_ksv2 = 40'hb70361f714;
```

Note2: For DDC frequency configuration

In the HDCP specification, the frequency value of DDC(F_{ddc}) support only up to 100Kbps, and now we select the TMDS clock as the reference clock of DDC , and under the condition of 1920x1080p@59.94/60Hz, the frequency of TMDS(F_{TMDS}) is 148.5MHz. Pay attention, internally we use the 4 times of DDC frequency to generate the SCL. So

X = F_{TMDS}/F_{ddc}/4 = 'h173, So the values of register 0x4b and 0x4c are 0x73 and 0x01.

24.6.9 NOMAL OPERATION EXAMPLE AT 1080P

After the description of HDMI Transmitter configuration above, the following example shows an entire configuration for HDMI Transmitter works on the 1080P mode.

Audio input requirement:

SD0 input (2 Channels I2S input)
WS (fs) = 48 KHz
SCK = 64fs
MCLK = 256fs

Video input requirement:

24bit RGB 4:4:4 Source.
Resolution is 1080P@60.

Setup Steps:

Step1: Power on HDMI Transmitter.
Step2: Configure the input signals.
Assign pin_test_en = 1'b0.

Step3: Reset HDMI Transmitter.
Assign 0 to the signal pin_rst_n and then assign 1.
Step4: System power down.
Send 0x63 to register 0x00.
Step5: Detect Hot Plug In.
Step6: Read EDID.
Step7: Configure video input format.
Step8: Configure audio input format.
Step9: Assign video and audio source to HDMI Transmitter.
Step10: System power on.
Send 0x61 to register 0x00.
Step11: Now, HDMI Transmitter is ready to go. Start your operation.

24.7 Electrical Specification

HDMI Transmitter contains tunable source termination and pre-emphasis to enable high speed operation. The Transmitter meets the AC specifications below across all operating conditions specified. Rise and fall times are defined as the signal transition time between 20% and 80% of the nominal swing voltage (Vswing) of the device under test. The Transmitter intra-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1, between the true and complement signals of a given differential pair. This time difference is measured at the midpoint on the single-ended signal swing of the true and complement signals. The Transmitter inter-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1.

Table 24-5Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	$mV_{p.p}$
T_A	Ambient Temperature (with power applied)	0	25	70	℃

Table 24-6Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
$V_{CC}^{1.2}$	Supply Voltage 3.3V	-0.3		4.0	V
$V_1^{1.2}$	Input Voltage	-0.3		V_{CC}+0.3	V
$V_0^{1.2}$	Output Voltage	-0.3		V_{CC}+0.3	V
$V_J^{1.2}$	Junction Temperature (with power applied)			125	℃

Table 24-7Transmitter DC Characteristics at TP1

Item	Value
Single-ended high level output voltage, V_H	AV_{cc}-10mV< V_H < AV_{cc}+10mV when

	sink <= 165Mhz
	AV_{cc}-200mV< V_H < AV_{cc}+10mV when sink >165Mhz
Single-ended low level output voltage, V_L	(AV_{cc} – 600mV) < V_L < (AV_{cc} – 400mV) when sink <=165Mhz
	(AV_{cc} – 700mV) < V_L < (AV_{cc} – 400mV) when sink > 165Mhz
Single-ended output swing voltage, V_{swing}	400mV < V_{swing}< 600mV
Single-ended standby (off) output voltage, V_{OFF}	AV_{cc}+.10mV
Single-ended standby (off) output current, I_{OFF}	| I_{OFF}|< 10uA

Table 24-8Transmitter AC Characteristics at TP1

Item	Value
Risetime/falltime (20%-80%)	75psec< Risetime/falltime < 0.4 T_{bit}
Overshoot, max	15% of full differential amplitude (V_{swing}*2)
Undershoot, max	25% of full differential amplitudee (V_{swing}*2)
Intra-Pair Skew at Transmitter Connector, max	0.15 T_{bit}
Inter-Pair Skew at Transmitter Connector, max	0.20 T_{pixel}
TMDS Differential Clock Jitter, max	0.25 T_{bit}
Clock duty cycle	40% to 60%

Table 24-9Programmable Output Resistance and Output Equalization Level

Item	Value
Output Equalization level	10% to 60%
Termination Resistance	50ohm and 75 ohms selectable with fine steps
OutputSwingRanges	4 different levels

24.7.1 CONTROL SIGNAL - DDC

DDC (Display Data Channel) control signals follow the I2C Bus specifications. More details to be filled out from I2C specs.

Item	Value
High Voltage Level (Vih)	-3.0V < Vih < 3.8V
Low Voltage Level (Vil)	-0.5V < Vil < 1.5V
SCL clock frequency	100KHz (max)
Rise time	< 1000ns
Fall time	< 300ns
Capacitive load on bus line	400pF

24.7.2 CONTROL SIGNAL - HPD

HPD (Hot Plug Detect) signal is used by the source to read the sink's E-DID. The sink needs to meet the following requirements for reliable detection.

For Sink

Item	Value

High Voltage Level (Vih)	2.4V < Vih < 5.3V
Low Voltage Level (Vil)	0V < Vil < 0.4V

For Source

Item	Value
High Voltage Level (Voh)	2.0V < Voh < 5.3V
Low Voltage Level (Vol)	0V < Vol < 0.8V