Chapter 21 Camera Interface (CIF)

21.1 Overview

The Camera interface, receives the data from Camera or CCIR656 encoder, and transfers the data into system main memory by AXI bus.

The features of camera interface are as follow:

- Support YCbCr422 input
- Support Raw8bit input
- Support CCIR656(PAL/NTSC) input
- Support JPEG input
- Support YCbCr422/420 output
- Support UYVY/VYUY/YUYV/YVYU configurable
- Support up to 8192x8192 resolution source
- Support picture in picture
- Support arbitrary size window crop
- Support error/terminate interrupt and combined interrupt output
- Support clk/vsync/href polarity configurable
- Support one frame stop/ping-pong mode

21.2 Block Diagram

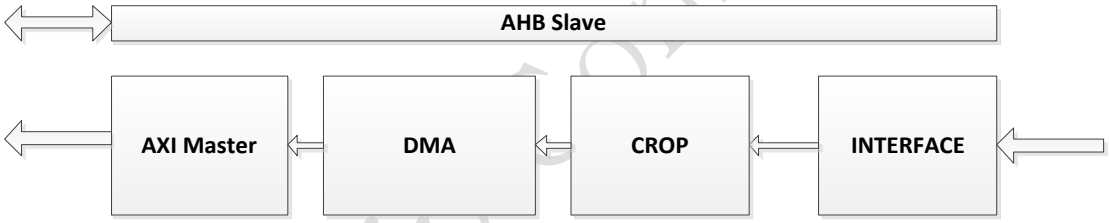

Fig. 21-1CIF block diagram

The CIF comprises with:

- AHB Slave
  Host configure the registers via the AHB Slave
- AXI Master
  Transmit the data to chip memory via the AXI Master
- INTERFACE
  Translate the input video data into the requisite data format
- CROP
  Bypass or crop the source video data to a smaller size destination
- DMA
  Control the operation of AXI Master

21.3 Function description

This chapter is used to illustrate the operational behavior of how CIF works. If YUV422 or ccir656 signal is received from external devices, CIF translate it into YUV422/420 data, and separate the data to Y and UV data, then store them to different memory via AXI bus separately. But if raw data is received, there are not any translations happened, the 8 data is considered as 16bit data and write directly to memory.

21.3.1 Support Vsync high active or low active

- Vsync Low active as below

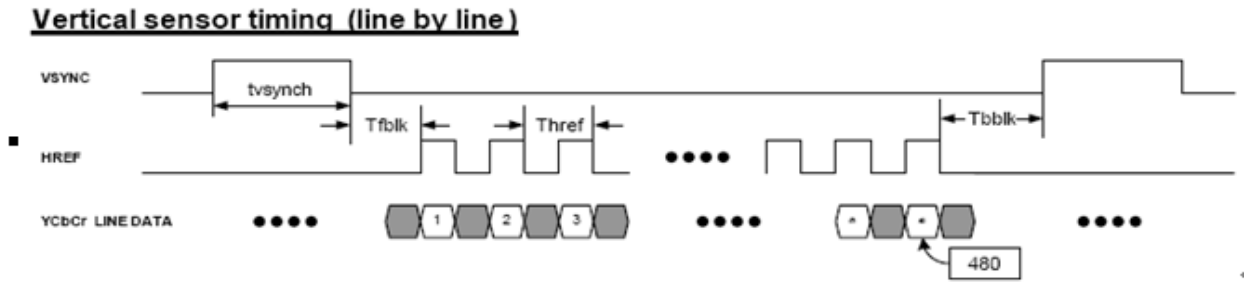

Fig. 21-2 Timing diagram for CIF when vsync low active

- Vsync High active

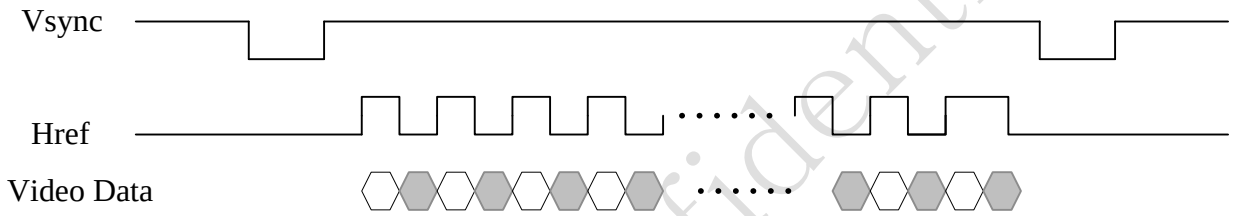

Fig. 21-3Timing diagram for CIF when vsync high active

21.3.2 Support href high active or low active

- Href high active

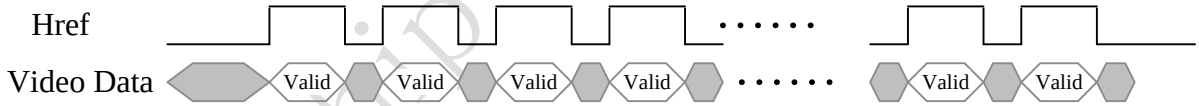

Fig. 21-4Timing diagram for CIF when href high active

- Href Low active

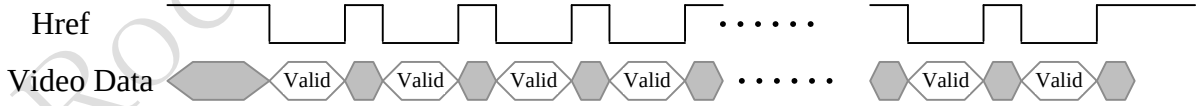

Fig. 21-5Timing diagram for CIF when href low active

- Y first

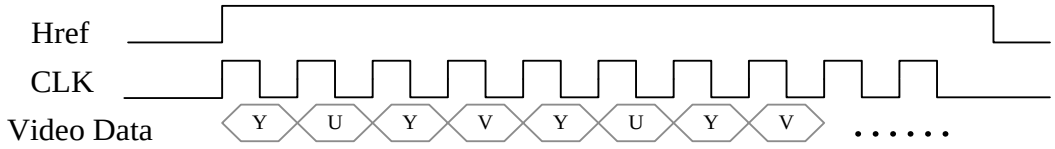

Fig. 21-6Timing diagram for CIF when Y data first

- U first

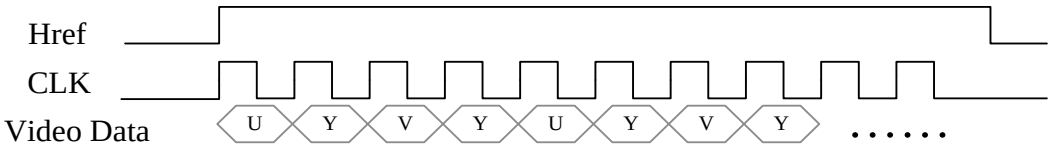

Fig. 21-7Timing diagram for CIF when U data first

21.3.3 Support CCIR656 (NTSC and PAL)

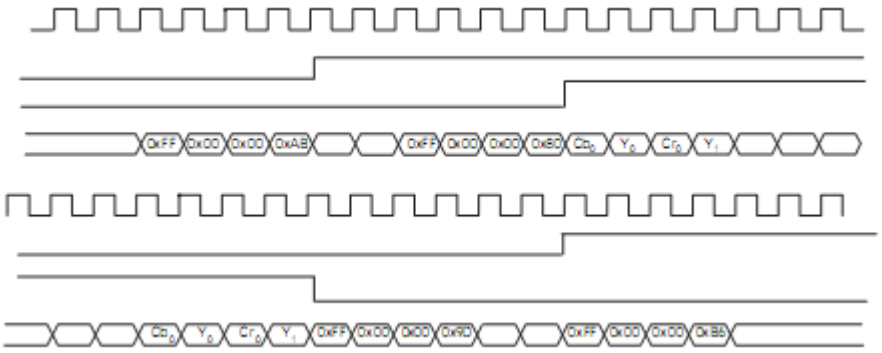

Fig. 21-8CCIR656 timing

21.3.4 Support Raw data(8-bit) or JPEG

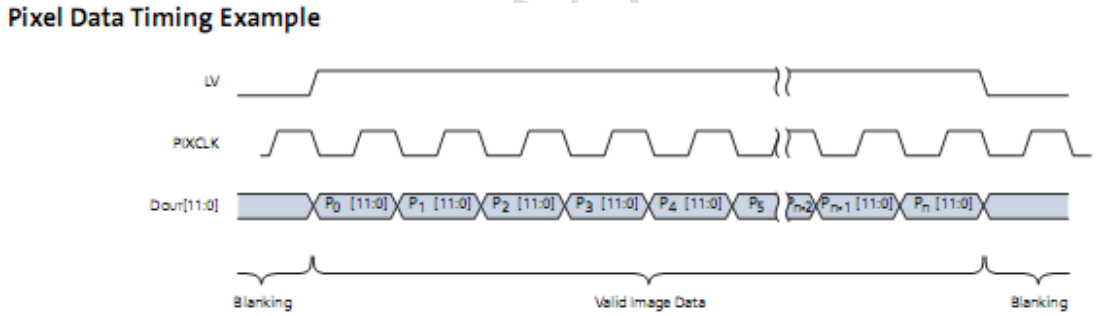

Fig. 21-9Raw Data or JPEG Timing

CIF module can work in three modes: one frame stop mode, ping-pong mode.

One frame stop mode

In this mode, configure the parameter WORK_MODE to one frame stop mode. After one frame captured, CIF will automatic stop. After capturing, the image Y, UV data will be stored at main memory location defined by CIF_FRM0_ADDR_Y, FRM0_ADDR_UV separately.

Ping-Pong mode

After one frame(F1) captured, CIF will start to capture the next frame(F2) automatically, and host must assign new address pointer of frame1 and clear the frame1 status, thus CIF will capture the third frame automatically(by new F1 address) without any stop and so on for the following frames. But if host did not update the frame buffer address, the CIF will cover the pre-frame data stored in the memory with the following frame data.

Storage

Difference between the YUV mode and raw mode is that in the YUV mode or ccir656 mode, data will be storage in the Y data buffer and UV data buffer; but in the raw or jpeg mode, RGB data will be storage in the same buffer. In addition, in the yuv mode, the width of Y, U or V data is a byte in memory; in Raw or JPEGE mode, the width is a halfword no matter the data source is 8 bit.

CROP

The parameter START_Y and START_X defines the coordinate of crop start point.And the frame size after cropping is following the value of SET_WIDTH and SET_HEIGHT.

21.4 Register description

21.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
CIF_CIF_CTRL	0x0000	W	0x00007000	CIF control
CIF_CIF_INTEN	0x0004	W	0x00000000	CIF interrupt enable
CIF_CIF_INTSTAT	0x0008	W	0x00000000	CIF interrupt status
CIF_CIF_FOR	0x000c	W	0x00000000	CIF format
CIF_CIF_FRM0_ADDR_Y	0x0014	W	0x00000000	CIF frame0 y address
CIF_CIF_FRM0_ADDR_UV	0x0018	W	0x00000000	CIF frame0 uv address
CIF_CIF_FRM1_ADDR_Y	0x001c	W	0x00000000	CIF frame1 y address
CIF_CIF_FRM1_ADDR_UV	0x0020	W	0x00000000	CIF frame1 uv address
CIF_CIF_VIR_LINE_WIDTH	0x0024	W	0x00000000	CIF virtual line width
CIF_CIF_SET_SIZE	0x0028	W	0x01e002d0	CIF frame set size
CIF_CIF_CROP	0x0044	W	0x00000000	CIF crop start point
CIF_CIF_SCL_CTRL	0x0048	W	0x00000000	CIF scale control
CIF_CIF_FIFO_ENTRY	0x0054	W	0x00000000	CIF FIFO entry
CIF_CIF_FRAME_STATUS	0x0060	W	0x00000000	CIF frame status
CIF_CIF_CUR_DST	0x0064	W	0x00000000	CIF current destination address
CIF_CIF_LAST_LINE	0x0068	W	0x00000000	CIF last frame line number
CIF_CIF_LAST_PIX	0x006c	W	0x00000000	CIF last line pixel number

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

21.4.2 Detail Register Description

CIF_CIF_CTRL
Address: Operational Base + offset (0x0000)
CIF control

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x7	AXI_BURST_TYPE axi master burst type 0-15 : burst1~16
11:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:1	RW	0x0	WORK_MODE Working Mode 00-one frame stop mode 01-ping-pong mode 02-line loop mode 03-reserved
0	RW	0x0	CAP_EN capture enable 0-disable 1-enable

CIF_CIF_INTEN

Address: Operational Base + offset (0x0004)

CIF interrupt enable

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	BUS_ERR_EN bus error axi master or ahb slave response error 0-disable 1-enable
5:4	RO	0x0	reserved
3	RW	0x0	PIX_ERR_EN pixel err interrupt enable the pixel number of last line not equal to the set height 0-disable 1-enable
2	RW	0x0	LINE_ERR_EN line err interrupt enable the line number of last frame not equal to the set height 0-disable 1-enable
1	RW	0x0	LINE_END_EN line end interrupt enable 0-disable 1-enable
0	RW	0x0	FRAME_END_EN frame end interrupt enable after dma transfer the frame data 0-disable 1-enable

CIF_CIF_INTSTAT

Address: Operational Base + offset (0x0008)

CIF interrupt status

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	W1C	0x0	BUS_ERR bus error axi master or ahb slave response error 0-no interrupt 1-interrupt
5:4	RO	0x0	reserved
3	W1C	0x0	PIX_ERR pixel err interrupt the pixel number of last line not equal to the set height 0-no interrupt 1-interrupt
2	W1C	0x0	LINE_ERR line err interrupt the line number of last frame not equal to the set height 0-no interrupt 1-interrupt
1	W1C	0x0	LINE_END line end interrupt enable 0-no interrupt 1-interrupt
0	W1C	0x0	FRAME_END frame end interrupt after dma transfer the frame data 0-no interrupt 1-interrupt

CIF_CIF_FOR
Address: Operational Base + offset (0x000c)
CIF format

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	UV_STORE_ORDER UV storage order 0 - UVUV 1 - VUVU
18	RW	0x0	RAW_END raw data endian 0 - little end 1 - big end
17	RW	0x0	OUT_420_ORDER output 420 order 00 - UV in the even line 01 - UV in the odd line Note: The first line is even line(line 0).
16	RW	0x0	OUTPUT_420 output 420 or 422 0 - output is 422 1 - output is 420
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:11	RW	0x0	RAW_WIDTH raw data width must be 2'b00.
10	RW	0x0	JPEG_MODE JPEG mode 0 - other mode 1 - mode1
9	RW	0x0	FIELD_ORDER ccir input order 0-odd field first 1-even field first
8	RW	0x0	IN_420_ORDER 420 input order 00 - UV in the even line 01 - UV in the odd line Note: The first line is even line(line 0).
7	RW	0x0	INPUT_420 input 420 or 422 0 - 422 1 - 420
6:5	RW	0x0	YUV_IN_ORDER YUV input order 00 - UYVY 01 - YVYU 10 - VYUY 11 - YUYV
4:2	RW	0x0	INPUT_MODE input mode 000 - YUV 010 - PAL 011 - NTSC 100 - RAW 101 - JPEG 110 - MIPI Other - invalid
1	RW	0x0	HREF_POL href input polarity 0-high active 1-low active
0	RW	0x0	VSYNC_POL vsync input polarity 0-;ow active 1-high active

CIF_CIF_FRM0_ADDR_Y

Address: Operational Base + offset (0x0014)

CIF frame0 y address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_Y frame0 y address

CIF_CIF_FRM0_ADDR_UV
Address: Operational Base + offset (0x0018)
CIF frame0 uv address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_UV frame0 uv address

CIF_CIF_FRM1_ADDR_Y
Address: Operational Base + offset (0x001c)
CIF frame1 y address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_Y frame1 y address

CIF_CIF_FRM1_ADDR_UV
Address: Operational Base + offset (0x0020)
CIF frame1 uv address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_UV frame1 uv address

CIF_CIF_VIR_LINE_WIDTH
Address: Operational Base + offset (0x0024)
CIF virtual line width

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	VIR_LINE_WIDTH virtual line width

CIF_CIF_SET_SIZE
Address: Operational Base + offset (0x0028)
CIF frame set size

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x01e0	SET_HEIGHT set height
15:13	RO	0x0	reserved
12:0	RW	0x02d0	SET_WIDTH set width

CIF_CIF_CROP
Address: Operational Base + offset (0x0044)
CIF crop start point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	START_Y start y point
15:13	RO	0x0	reserved
12:0	RW	0x0000	START_X start x point

CIF_CIF_SCL_CTRL
Address: Operational Base + offset (0x0048)
CIF scale control

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	RAW_16B_BP raw 16 bit bypass 0-no bypass 1-bypass
4	RW	0x0	YUV_16B_BP YUV 16 bit bypass 0-no bypass 1-bypass
3:0	RO	0x0	reserved

CIF_CIF_FIFO_ENTRY
Address: Operational Base + offset (0x0054)
CIF FIFO entry

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:8	RW	0x00	UV_FIFO_ENTRY valid UV double word in FIFO write 0 clear
7	RO	0x0	reserved
6:0	RO	0x00	Y_FIFO_ENTRY valid Y double word in FIFO write 0 clear

CIF_CIF_FRAME_STATUS
Address: Operational Base + offset (0x0060)
CIF frame status

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	FRAME_NUM complete frame number write 0 to clear
15:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	F1_STS frame 0 status 0- frame 1 not ready 1- frame 1 ready write 0 clear
0	RO	0x0	F0_STS frame 0 status 0- frame 0 not ready 1- frame 0 ready write 0 clear

CIF_CIF_CUR_DST
Address: Operational Base + offset (0x0064)
CIF current destination address

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CUR_DST current destination address maybe not the current, because the clock synchronization.

CIF_CIF_LAST_LINE
Address: Operational Base + offset (0x0068)
CIF last frame line number

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	LAST_LINE_NUM line number of last frame

CIF_CIF_LAST_PIX
Address: Operational Base + offset (0x006c)
CIF last line pixel number

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RO	0x0000	LAST_PIX_NUM pixel number of last line

21.5 Interface description

Module Pin	Direction	Pad Name	IOMUX Setting
cif_clkout	O	TS0clk_CIFclkout	GRF_CIFD_IOMUX1[6]==1'b0
cif_clkin	I	TS0valid_CIFclkin	GRF_CIFD_IOMUX1[4]==1'b0
cif_href	I	TS0err_CIFhref	GRF_CIFD_IOMUX1[2]==1'b0
cif_vsync	I	TS0sync_CIFvsync	GRF_CIFD_IOMUX1[0]==1'b0
cif_data0	I	TS0d0_CIFd0	GRF_CIFD_IOMUX[0]==1'b0
cif_data1	I	TS0d1_CIFd1	GRF_CIFD_IOMUX[2]==1'b0

cif_data2	I	TS0d2_CIFd2	GRF_CIFD_IOMUX[4]==1'b0
cif_data3	I	TS0d3_CIFd3	GRF_CIFD_IOMUX[6]==1'b0
cif_data4	I	TS0d4_CIFd4	GRF_CIFD_IOMUX[8]==1'b0
cif_data5	I	TS0d5_CIFd5	GRF_CIFD_IOMUX[10]==1'b0
cif_data6	I	TS0d6_CIFd6	GRF_CIFD_IOMUX[12]==1'b0
cif_data7	I	TS0d7_CIFd7	GRF_CIFD_IOMUX[14]==1'b0

21.6 Application Notes

The biggest configuration requirement of all operations is the CAP_EN bit must be set after all the mode selection is ready.The configuration order of the input/output data format, YUV order, the address,frame size/width, AXI burst length and other options do not need to care.

There are many debug registers to make it easy to read the internal operation information of CIF. The valid pixel number of scale result in FIFO can be known by read CIF_CIF_SCL_VALID_NUM.The line number of last frame and the pixel number of last line can be also known by read the CIF_CIF_LAST_LINE and CIF_CIF_LAST_PIX.