Chapter 5 General register file(GRF)

5.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control.

5.1.1 Features

The function of general register file is：

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

5.2 GRF Register Description

5.2.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO0A_IOMUX	0x00a8	W	0x00000000	GPIO0A iomux control
GRF_GPIO0B_IOMUX	0x00ac	W	0x00000000	GPIO0B iomux control
GRF_GPIO0C_IOMUX	0x00b0	W	0x00000000	GPIO0C iomux control
GRF_GPIO0D_IOMUX	0x00b4	W	0x00000000	GPIO0D iomux control
GRF_GPIO1A_IOMUX	0x00b8	W	0x00000c00	GPIO1A iomux control
GRF_GPIO1B_IOMUX	0x00bc	W	0x00000030	GPIO1B iomux control
GRF_GPIO1C_IOMUX	0x00c0	W	0x00000000	GPIO1C iomux control
GRF_GPIO1D_IOMUX	0x00c4	W	0x00000000	GPIO1D iomux control
GRF_GPIO2A_IOMUX	0x00c8	W	0x00000000	GPIO2A iomux control
GRF_GPIO2B_IOMUX	0x00cc	W	0x00000000	GPIO2B iomux control
GRF_GPIO2C_IOMUX	0x00d0	W	0x00000000	GPIO2C iomux control
GRF_GPIO2D_IOMUX	0x00d4	W	0x00000000	GPIO2D iomux control
GRF_GPIO3A_IOMUX	0x00d8	W	0x00000000	GPIO3A iomux control
GRF_GPIO3B_IOMUX	0x00dc	W	0x00000000	GPIO3B iomux control
GRF_GPIO3C_IOMUX	0x00e0	W	0x00000000	GPIO3D iomux control
GRF_GPIO3D_IOMUX	0x00e4	W	0x00000000	GPIO3D iomux control
GRF_GPIO2C_IOMUX 2	0x00e8	W	0x00000000	GPIO2C iomux control
GRF_CIF_IOMUX	0x00ec	W	0x00000000	CIF iomux control
GRF_CIF_IOMUX1	0x00f0	W	0x00000000	CIF iomux control register1
GRF_GPIO_DS	0x0100	W	0x00000000	GPIO DS control
GRF_GPIO0L_PULL	0x0118	W	0x00000000	GPIO0A / GPIO0B pull up/down control
GRF_GPIO0H_PULL	0x011c	W	0x00000000	GPIO0C / GPIO0D pull up/down control
GRF_GPIO1L_PULL	0x0120	W	0x00000000	GPIO0A / GPIO0B pull up/down control
GRF_GPIO1H_PULL	0x0124	W	0x00000000	GPIO1C / GPIO1D pull up/down control

Name	Offset	Size	Reset Value	Description
GRF_GPIO2L_PULL	0x0128	W	0x00000000	GPIO2A / GPIO2B pull up/down control
GRF_GPIO2H_PULL	0x012c	W	0x00000000	GPIO2C / GPIO2D pull up/down control
GRF_GPIO3L_PULL	0x0130	W	0x00000000	GPIO3A / GPIO3B pull up/down control
GRF_GPIO3H_PULL	0x0134	W	0x00000000	GPIO3C / GPIO3D pull up/down control
GRF_ACODEC_CON	0x013c	W	0x00000020	SoC control register
GRF_SOC_CON0	0x0140	W	0x00000120	SoC control register
GRF_SOC_CON1	0x0144	W	0x00000000	SoC control register
GRF_SOC_CON2	0x0148	W	0x00000084	SoC control register
GRF_SOC_STATUS0	0x014c	W	0x00000000	SoC status register
GRF_LVDS_CON0	0x0150	W	0x00000000	LVDS control register
GRF_DMAC_CON0	0x015c	W	0x00000000	DMAC control register
GRF_DMAC_CON1	0x0160	W	0x00000000	DMAC control register
GRF_DMAC_CON2	0x0164	W	0x00000010	DMAC control register
GRF_MAC_CON0	0x0168	W	0x00000810	GMAC control register0
GRF_MAC_CON1	0x016c	W	0x00004040	GMAC control register1
GRF_TVE_CON	0x0170	W	0x00000000	TV encoder control register
GRF_UOC0_CON0	0x017c	W	0x00000000	OTG control register
GRF_UOC1_CON1	0x0184	W	0x00000000	usb host control register
GRF_UOC1_CON2	0x0188	W	0x0000c820	UOC1 control register 2
GRF_UOC1_CON3	0x018c	W	0x00000b40	UOC1 control register 3
GRF_UOC1_CON4	0x0190	W	0x0000001c	USB HOST 2.0 control register
GRF_UOC1_CON5	0x0194	W	0x00000000	USB HOST 2.0 control register
GRF_DDRC_STAT	0x019c	W	0x00000000	DDRC status
GRF_SOC_STATUS1	0x01a4	W	0x00000000	SoC status register
GRF_CPU_CON0	0x01a8	W	0x00002002	CPU control register
GRF_CPU_CON1	0x01ac	W	0x00000000	CPU control register
GRF_CPU_CON2	0x01b0	W	0x0000003f	CPU control register
GRF_CPU_CON3	0x01b4	W	0x00002aaa	CPU control register
GRF_CPU_STATUS0	0x01c0	W	0x00000000	CPU status register
GRF_CPU_STATUS1	0x01c4	W	0x00000000	CPU status register
GRF_OS_REG0	0x01c8	W	0x00000000	software OS register
GRF_OS_REG1	0x01cc	W	0x00000000	software OS register
GRF_OS_REG2	0x01d0	W	0x00000000	software OS register
GRF_OS_REG3	0x01d4	W	0x00000000	software OS register
GRF_OS_REG4	0x01d8	W	0x00000000	software OS register
GRF_OS_REG5	0x01dc	W	0x00000000	software OS register
GRF_OS_REG6	0x01e0	W	0x00000000	software OS register
GRF_OS_REG7	0x01e4	W	0x00000000	software OS register
GRF_PVTM_CON0	0x0200	W	0x00000000	PVTM control register
GRF_PVTM_CON1	0x0204	W	0x00000000	PVTM control register
GRF_PVTM_CON2	0x0208	W	0x00000000	PVTM control register
GRF_PVTM_CON3	0x020c	W	0x00000000	PVTM control register
GRF_PVTM_STATUS0	0x0210	W	0x00000000	PVTM status register0

Name	Offset	Size	Reset Value	Description
GRF_PVTM_STATUS1	0x0214	W	0x00000000	PVTM status register1
GRF_PVTM_STATUS2	0x0218	W	0x00000000	PVTM status register2
GRF_PVTM_STATUS3	0x021c	W	0x00000000	PVTM status register3
GRF_DFI_WRNUM	0x0220	W	0x00000000	DFI write number register
GRF_DFI_RDNUM	0x0224	W	0x00000000	DFI read number register
GRF_DFI_ACTNUM	0x0228	W	0x00000000	DFI active number register
GRF_DFI_TIMERVAL	0x022c	W	0x00000000	DFI work time
GRF_NIF_FIFO0	0x0230	W	0x00000000	NIF status register
GRF_NIF_FIFO1	0x0234	W	0x00000000	NIF status register
GRF_NIF_FIFO2	0x0238	W	0x00000000	NIF status register
GRF_NIF_FIFO3	0x023c	W	0x00000000	NIF status register
GRF_USBPHY0_CON0	0x0280	W	0x00008618	usbphy control register
GRF_USBPHY0_CON1	0x0284	W	0x0000e007	usbphy control register
GRF_USBPHY0_CON2	0x0288	W	0x000082aa	usbphy control register
GRF_USBPHY0_CON3	0x028c	W	0x00000200	usbphy control register
GRF_USBPHY0_CON4	0x0290	W	0x00000002	usbphy control register
GRF_USBPHY0_CON5	0x0294	W	0x00000000	usbphy control register
GRF_USBPHY0_CON6	0x0298	W	0x00000004	usbphy control register
GRF_USBPHY0_CON7	0x029c	W	0x000068c0	usbphy control register
GRF_USBPHY1_CON0	0x02a0	W	0x00008618	usbphy control register
GRF_USBPHY1_CON1	0x02a4	W	0x0000e007	usbphy control register
GRF_USBPHY1_CON2	0x02a8	W	0x000082aa	usbphy control register
GRF_USBPHY1_CON3	0x02ac	W	0x00000200	usbphy control register
GRF_USBPHY1_CON4	0x02b0	W	0x00000002	usbphy control register
GRF_USBPHY1_CON5	0x02b4	W	0x00000000	usbphy control register
GRF_USBPHY1_CON6	0x02b8	W	0x00000004	usbphy control register
GRF_USBPHY1_CON7	0x02bc	W	0x000068c0	usbphy control register
GRF_UOC_STATUS0	0x02c0	W	0x00000000	SoC status register 0
GRF_CHIP_TAG	0x0300	W	0x0000293c	chip tag register
GRF_MMC_DET_CNT	0x0304	W	0x0000fdb9	mmc0 detect filter counter register
GRF_EFUSE_PRG_EN	0x037c	W	0x00000000	efuse program register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.2.2 Detailed Register Description

GRF_GPIO0A_IOMUX
Address: Operational Base + offset (0x00a8)
GPIO0A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio0a7_sel GPIO0A[7] iomux select 01: i2c3_sda 10: hdmi_ddcsda 00: gpio
13:12	RW	0x0	gpio0a6_sel GPIO0A[6] iomux select 01: i2c3_scl 10: hdmi_ddcscl 00: gpio
11:8	RO	0x0	reserved
7:6	RW	0x0	gpio0a3_sel GPIO0A[3] iomux select 01: i2c1_sda 10: mmc1_cmd 00: gpio
5	RO	0x0	reserved
4	RW	0x0	gpio0a2_sel GPIO0A[2] iomux select 1: i2c1_scl 0: gpio
3	RO	0x0	reserved
2	RW	0x0	gpio0a1_sel GPIO0A[1] iomux select 1: i2c0_sda 0: gpio
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio0a0_sel GPIO0A[0] iomux select 1: i2c0_scl 0: gpio

GRF_GPIO0B_IOMUX
Address: Operational Base + offset (0x00ac)
GPIO0B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	gpio0b7_sel GPIO0B[7] iomux select 1: hdmi_hotplugin 0: gpio
13:12	RW	0x0	gpio0b6_sel GPIO0B[6] iomux select 01:i2s_sdi 10: spi_csn0 00: gpio
11:10	RW	0x0	gpio0b5_sel GPIO0B[5] iomux select 01:i2s_sdo 10: spi_rxd 00: gpio
9	RO	0x0	reserved
8	RW	0x0	gpio0b4_sel GPIO0B[4] iomux select 1: i2s_lrcktx 0: gpio
7:6	RW	0x0	gpio0b3_sel GPIO0B[3] iomux select 01:i2s_lrckrx 10: spi_txd 00: gpio
5:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio0b1_sel GPIO0B[1] iomux select 01:i2s_sclk 10: spi_clk 00: gpio
1	RO	0x0	reserved
0	RW	0x0	gpio0b0_sel GPIO0B[0] iomux select 1: i2s_mclk 0: gpio

GRF_GPIO0C_IOMUX
Address: Operational Base + offset (0x00b0)
GPIO0C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	gpio0c7_sel GPIO0C[7] iomux select 1: nand_cs1 0: gpio
13:9	RO	0x0	reserved
8	RW	0x0	gpio0c4_sel GPIO0C[4] iomux select 1: hdmi_cecsda 0: gpio
7:4	RO	0x0	reserved
3:2	RW	0x0	gpio0c1_sel GPIO0C[1] iomux select 01: sc_io 10: uart0_rstn 00: gpio
1:0	RO	0x0	reserved

GRF_GPIO0D_IOMUX
Address: Operational Base + offset (0x00b4)

GPIO0D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	gpio0d6_sel GPIO0D[6] iomux select 1: mmc1_pwren 0: gpio
11:9	RO	0x0	reserved
8	RW	0x0	gpio0d4_sel GPIO0D[4] iomux select 1:pwm_2 0: gpio
7	RO	0x0	reserved
6	RW	0x0	gpio0d3_sel GPIO0D[3] iomux select 1: pwm_1 0: gpio
5	RO	0x0	reserved
4	RW	0x0	gpio0d2_sel GPIO0D[2] iomux select 1: pwm_0 0: gpio
3	RO	0x0	reserved
2	RW	0x0	gpio0d1_sel GPIO0D[1] iomux select 1: uart2_ctsn 0: gpio
1:0	RW	0x0	gpio0d0_sel GPIO0D[0] iomux select 01: uart2_rtsn 10: pmic_sleep 00: gpio

GRF_GPIO1A_IOMUX

Address: Operational Base + offset (0x00b8)

GPIO1A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	gpio1a7_sel GPIO1A[7] iomux select 1: mmc0_wrprt 0: gpio
13:12	RO	0x0	reserved
11:10	RW	0x3	gpio1a5_sel GPIO1A[5] iomux select 01: i2s_sdi 10: sdmmc_data3 00: gpio
9:8	RW	0x0	gpio1a4_sel GPIO1A[4] iomux select 01: i2s_sdo 10: sdmmc_data2 00: gpio
7	RO	0x0	reserved
6	RW	0x0	gpio1a3_sel GPIO1A[3] iomux select 1: i2s_lrcktx 0: gpio
5:4	RW	0x0	gpio1a2_sel GPIO1A[2] iomux select 01: i2s_lrckrx 10: sdmmc_data1 00: gpio
3:2	RW	0x0	gpio1a1_sel GPIO1A[1] iomux select 01: i2s_sclk 10: sdmmc_data0 11: pmic_sleep 00: gpio

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio1a0_sel GPIO1A[0] iomux select 01: i2s_mclk 10: sdmmc_clkout 11: xin32k 00: gpio

GRF_GPIO1B_IOMUX

Address: Operational Base + offset (0x00bc)

GPIO1B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	gpio1b7_sel GPIO1B[7] iomux select 1: mmc0_cmd 0: gpio
13	RO	0x0	reserved
12	RW	0x0	gpio1b6_sel GPIO1B[6] iomux select 1: mmc0_pwren 0: gpio
11:9	RO	0x0	reserved
8	RW	0x0	gpio1b4_sel GPIO1B[4] iomux select 1: spi_csn1 0: gpio
7:6	RW	0x0	gpio1b3_sel GPIO1B[3] iomux select 01: spi_csn0 10: uart1_rtsn 00: gpio
5:4	RW	0x3	gpio1b2_sel GPIO1B[2] iomux select 01: spi_rxd 10: uart1_sin 00: gpio

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio1b1_sel GPIO1B[1] iomux select 01: spi_txd 10: uart1_sout 00: gpio
1:0	RW	0x0	gpio1b0_sel GPIO1B[0] iomux select 01: spi_clk 10: uart1_ctsn 00: gpio

GRF_GPIO1C_IOMUX
Address: Operational Base + offset (0x00c0)
GPIO1C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1c7_sel GPIO1C[7] iomux select 01: nand_cs3 10:emmc_rstnout 00: gpio
13:12	RW	0x0	gpio1c6_sel GPIO1C[6] iomux select 01: nand_cs2 10: emmc_cmd 00: gpio
11:10	RW	0x0	gpio1c5_sel GPIO1C[5] iomux select 10: jtag_tms when sdmmc0_detectn is invalid 01: mmc0_d3 00: gpio
9:8	RW	0x0	gpio1c4_sel GPIO1C[4] iomux select 10: jtag_tck when sdmmc0_detectn is invalid 01: mmc0_d2 00: gpio

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio1c3_sel GPIO1C[3] iomux select 01: mmc0_d1 10: uart2_rx 00: gpio
5:4	RW	0x0	gpio0c2_sel GPIO0C[2] iomux select 01:mmc0_d0 10: uart2_tx 00:gpio
3	RO	0x0	reserved
2	RW	0x0	gpio1c1_sel GPIO1C[1] iomux select 1: mmc0_detn 0: gpio
1	RO	0x0	reserved
0	RW	0x0	gpio1c0_sel GPIO1C[0] iomux select 1: mmc0_clkout 0: gpio

GRF_GPIO1D_IOMUX
Address: Operational Base + offset (0x00c4)
GPIO1D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1d7_sel GPIO1D[7] iomux select 01: nand_d7 10: emmc_d7 11: spi_csn1 00: gpio

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1d6_sel GPIO1D[6] iomux select 01: nand_d6 10: emmc_d6 11: spi_csn0 00: gpio
11:10	RW	0x0	gpio1d5_sel GPIO1D[5] iomux select 01: nand_d5 10: emmc_d5 11: spi_txd1 00: gpio
9:8	RW	0x0	gpio1d4_sel GPIO1D[4] iomux select 01: nand_d4 10: emmc_d4 11: spi_rxd1 00: gpio
7:6	RW	0x0	gpio1d3_sel GPIO1D[3] iomux select 01:nand_d3 10: emmc_d3 11: sfc_d3 00: gpio
5:4	RW	0x0	gpio1d2_sel GPIO1D[2] iomux select 01: nand_d2 10 : emmc_d2 11: sfc_d2 00: gpio
3:2	RW	0x0	gpio1d1_sel GPIO1D[1] iomux select 01: nand_d1 10: emmc_d1 11: sfc_d1 00: gpio
1:0	RW	0x0	gpio1d0_sel GPIO1D[0] iomux select 01: nand_d0 10: emmc_d0 11: sfc_d0 00: gpio

GRF_GPIO2A_IOMUX
Address: Operational Base + offset (0x00c8)
GPIO2A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2a7_sel GPIO2A[7] iomux select 01: nand_dqs 10: emmc_clkout 00: gpio
13	RO	0x0	reserved
12	RW	0x0	gpio2a6_sel GPIO2A[6] iomux select 1: nand_cs0 0: gpio
11:10	RW	0x0	gpio2a5_sel GPIO2A[5] iomux select 01: nand_wp 10: emmc_pwren 00: gpio
9:8	RW	0x0	gpio2a4_sel GPIO2A[4] iomux select 01: nand_rdy 10: emmc_cmd 11: sfc_clk 00: gpio
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] iomux select 01: nand_rdn 10: sfc_csn1 00: gpio
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] iomux select 01:nand_wrn 10: sfc_csn0 00: gpio
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] iomux select 01:nand_cle 00: gpio

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] iomux select 01: nand_ale 10: spi_clk 00: gpio

GRF_GPIO2B_IOMUX

Address: Operational Base + offset (0x00cc)

GPIO2B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2b7_sel GPIO2B[7] iomux select 01: lcdc0_d13 10: ebc_sdce5 11: gmac_rxer 00: gpio
13:12	RW	0x0	gpio2b6_sel GPIO2B[6] iomux select 01: lcdc0_d12 10: ebc_sdce4 11: gmac_clk 00: gpio
11:10	RW	0x0	gpio2b5_sel GPIO2B[5] iomux select 01:lcdc0_d11 10: ebc_sdce3 11: gmac_txen 00: gpio
9:8	RW	0x0	gpio2b4_sel GPIO2B[4] iomux select 01: lcdc0_d10 10: ebc_sdce2 11: gmac_mdio 00: gpio

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2b3_sel GPIO2B[3] iomux select 01: lcdc0_den 10: ebc_gdclk 11: gmac_rxclk 00: gpio
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] iomux select 01: lcdc0_vsync 10: ebc_sdoe 11: gmac_crs 00: gpio
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] iomux select 01: lcdc0_hsync 10: ebc_sdle 11: gmac_txclk 00: gpio
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] iomux select 01: lcdc0_dclk 10: ebc_sdclk 11: gmac_rxdv 00: gpio

GRF_GPIO2C_IOMUX

Address: Operational Base + offset (0x00d0)

GPIO2C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:6	RW	0x0	gpio2c3_sel GPIO2C[3] iomux select 01: lcdc0_d17 10: ebc_gdpwr0 11: gmac_txd0 00: gpio

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio2c2_sel GPIO2C[2] iomux select 01: lcdc0_d16 10: ebc_gdsp 11: gmac_txd1 00: gpio
3:2	RW	0x0	gpio2c1_sel GPIO2C[1] iomux select 01: lcdc0_d15 10: ebc_gdoe 11: gmac_rxd0 00: gpio
1:0	RW	0x0	gpio2c0_sel GPIO2C[0] iomux select 01:lcdc0_d14 10: ebc_vcom 11: gmac_rxd1 00: gpio

GRF_GPIO2D_IOMUX
Address: Operational Base + offset (0x00d4)
GPIO2D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:12	RW	0x0	gpio2d0_sel GPIO2D[0] iomux select 001: lcdc0_d22 010: ebc_gdpwr1 011: gps_clk 100: gmac_col 000: gpio
11:10	RW	0x0	gpio2d5_sel GPIO2D[5] iomux select 01: sc_det 10: uart0_ctsn 00: gpio

Bit	Attr	Reset Value	Description
9:8	RO	0x0	reserved
7:6	RW	0x0	gpio2d3_sel GPIO2D[3] iomux select 01: sc_clk 10: uart0_sin 00: gpio
5:4	RW	0x0	gpio2d2_sel GPIO2D[2] iomux select 01: sc_rst 10: uart0_sout 00: gpio
3:2	RW	0x0	gpio2d1_sel GPIO2D[1] iomux select 01: lcdc0_d23 10: ebc_gdpwr2 11: gmac_mdc 00: gpio
1:0	RO	0x0	reserved

GRF_GPIO3A_IOMUX
Address: Operational Base + offset (0x00d8)
GPIO3A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_GPIO3B_IOMUX
Address: Operational Base + offset (0x00dc)
GPIO3B iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	RW	0x0	gpio3a3_sel GPIO3A[3] iomux select 1: testclk_out 0: gpio
5:0	RO	0x0	reserved

GRF_GPIO3C_IOMUX
Address: Operational Base + offset (0x00e0)
GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] iomux select 1: otg_drvvbus 0: gpio
1:0	RO	0x0	reserved

GRF_GPIO3D_IOMUX
Address: Operational Base + offset (0x00e4)

GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	RW	0x0	gpio3d3_sel GPIO3D[3] iomux select 1: spdif_tx 0: gpio
5	RO	0x0	reserved
4	RW	0x0	gpio3d2_sel GPIO3D[2] iomux select 1: pwm_irin 0: gpio
3:0	RO	0x0	reserved

GRF_GPIO2C_IOMUX2

Address: Operational Base + offset (0x00e8)

GPIO2C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio2c7_sel GPIO2C[7] iomux select 001: lcdc0_d21 010: ebc_border1 011: gps_mag 100: gmac_txd3 000: gpio
11	RO	0x0	reserved
10:8	RW	0x0	gpio2c6_sel GPIO2C[6] iomux select 001: lcdc0_d20 010: ebc_border0 011: gps_sign 100: gmac_txd2 000: gpio
7	RO	0x0	reserved
6:4	RW	0x0	gpio2c5_sel GPIO2C[5] iomux select 001: lcdc0_d19 010: ebc_sdshr 011: i2c2_scl 100: gmac_rxd2 000: gpio
3	RO	0x0	reserved
2:0	RW	0x0	gpio2c4_sel GPIO2C[4] iomux select 001: lcdc0_d18 010: ebc_gdrl 011: i2c2_sda 100: gmac_rxd3 000: gpio

GRF_CIF_IOMUX
Address: Operational Base + offset (0x00ec)
CIF iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	cifd7_sel cif_d7 iomux select 1: ts_d7 0: cif_d7
13	RO	0x0	reserved
12	RW	0x0	cifd6_sel cif_d6 iomux select 1: ts_d6 0: cif_d6
11	RO	0x0	reserved
10	RW	0x0	cifd5_sel cif_d5 iomux select 1: ts_d5 0: cif_d5
9	RO	0x0	reserved
8	RW	0x0	cifd4_sel cif_4 iomux select 1: ts_d4 0: cif_d4
7	RO	0x0	reserved
6	RW	0x0	cifd3_sel cif_d3 iomux select 1: ts_d3 0: cif_d3
5	RO	0x0	reserved
4	RW	0x0	cifd2_sel cif_d2 iomux select 1: ts_d2 0: cif_d2
3	RO	0x0	reserved
2	RW	0x0	cifd1_sel cif_d1 iomux select 1: ts_d1 0: cif_d1
1	RO	0x0	reserved
0	RW	0x0	cifd0_sel cif_d0 iomux select 1: ts_d0 0: cif_d0

GRF_CIF_IOMUX1

Address: Operational Base + offset (0x00f0)

CIF iomux control register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	RW	0x0	cif_clkout_sel cif_clkout iomux select 1: ts_clk 0: cif_clkout
5	RO	0x0	reserved
4	RW	0x0	cif_clkin_sel cif_clkin iomux select 1: ts_valid 0: cif_clkin
3	RO	0x0	reserved
2	RW	0x0	cif_href_sel cif_href iomux select 1: ts_error 0: cif_href
1	RO	0x0	reserved
0	RW	0x0	cif_vsync_sel cif_vsync iomux select 1: ts_sync 0: cif_vsync

GRF_GPIO_DS

Address: Operational Base + offset (0x0100)

GPIO DS control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:10	RW	0x0	gpio_0c4_ds driver strength setting 00: 2.6mA ~ 6.8mA 01: 5.1mA ~ 14mA 10: 7.7mA ~ 20mA 11: 10mA ~ 27mA
9:8	RW	0x0	gpio_0b7_ds driver strength setting 00: 2.6mA ~ 6.8mA 01: 5.1mA ~ 14mA 10: 7.7mA ~ 20mA 11: 10mA ~ 27mA
7:6	RW	0x0	gpio_0a7_ds driver strength setting 00: 2.6mA ~ 6.8mA 01: 5.1mA ~ 14mA 10: 7.7mA ~ 20mA 11: 10mA ~ 27mA
5:4	RW	0x0	gpio_0a6_ds driver strength setting 00: 2.6mA ~ 6.8mA 01: 5.1mA ~ 14mA 10: 7.7mA ~ 20mA 11: 10mA ~ 27mA
3	RW	0x0	gpio_0c4_sl slew rata: 0:slow 1:fast
2	RW	0x0	gpio_0b7_sl slew rata: 0:slow 1:fast
1	RW	0x0	gpio_0a7_sl slew rata: 0:slow 1:fast

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio_0a6_sl slew rata: 0:slow 1:fast

GRF_GPIO0L_PULL
Address: Operational Base + offset (0x0118)
GPIO0A / GPIO0B pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0b_pull GPIO0B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO0B[0] pull up/down control bit9 - GPIO0B[1] pull up/down control bit10 - GPIO0B[2] pull up/down control ... bit15 - GPIO0B[7] pull up/down control
7:0	RW	0x00	gpio0a_pull GPIO0A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO0A[0] pull up/down control bit1 - GPIO0A[1] pull up/down control bit2 - GPIO0A[2] pull up/down control ... bit7 - GPIO0A[7] pull up/down control

GRF_GPIO0H_PULL
Address: Operational Base + offset (0x011c)
GPIO0C / GPIO0D pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0d_pull GPIO0D pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO0D[0] pull up/down control bit9 - GPIO0D[1] pull up/down control bit10 - GPIO0D[2] pull up/down control ... bit15 - GPIO0D[7] pull up/down control
7:0	RW	0x00	gpio0c_pull GPIO0C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO0C[0] pull up/down control bit1 - GPIO0C[1] pull up/down control bit2 - GPIO0C[2] pull up/down control ... bit7 - GPIO0C[7] pull up/down control

GRF_GPIO1L_PULL
Address: Operational Base + offset (0x0120)
GPIO0A / GPIO0B pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio1b_pull GPIO1B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO1B[0] pull up/down control bit9 - GPIO1B[1] pull up/down control bit10 - GPIO1B[2] pull up/down control ... bit15 - GPIO1B[7] pull up/down control
7:0	RW	0x00	gpio1a_pull GPIO1A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO1A[0] pull up/down control bit1 - GPIO1A[1] pull up/down control bit2 - GPIO1A[2] pull up/down control ... bit7 - GPIO1A[7] pull up/down control

GRF_GPIO1H_PULL

Address: Operational Base + offset (0x0124)

GPIO1C / GPIO1D pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio1d_pull GPIO1d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO1D[0] pull up/down control bit9 - GPIO1D[1] pull up/down control bit10 - GPIO1D[2] pull up/down control ... bit15 - GPIO1D[7] pull up/down control
7:0	RW	0x00	gpio1c_pull GPIO1C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO1C[0] pull up/down control bit1 - GPIO1C[1] pull up/down control bit2 - GPIO1C[2] pull up/down control ... bit7 - GPIO1C[7] pull up/down control

GRF_GPIO2L_PULL

Address: Operational Base + offset (0x0128)

GPIO2A / GPIO2B pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio2b_pull GPIO2B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO2B[0] pull up/down control bit9 - GPIO2B[1] pull up/down control bit10 - GPIO2B[2] pull up/down control ... bit15 - GPIO2B[7] pull up/down control
7:0	RW	0x00	gpio2a_pull GPIO2A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO2A[0] pull up/down control bit1 - GPIO2A[1] pull up/down control bit2 - GPIO2A[2] pull up/down control ... bit7 - GPIO2A[7] pull up/down control

GRF_GPIO2H_PULL

Address: Operational Base + offset (0x012c)

GPIO2C / GPIO2D pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio2d_pull GPIO2d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO2D[0] pull up/down control bit9 - GPIO2D[1] pull up/down control bit10 - GPIO2D[2] pull up/down control ... bit15 - GPIO2D[7] pull up/down control
7:0	RW	0x00	gpio2c_pull GPIO2C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO2C[0] pull up/down control bit1 - GPIO2C[1] pull up/down control bit2 - GPIO2C[2] pull up/down control ... bit7 - GPIO2C[7] pull up/down control

GRF_GPIO3L_PULL

Address: Operational Base + offset (0x0130)

GPIO3A / GPIO3B pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio3b_pull GPIO3B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO3B[0] pull up/down control bit9 - GPIO3B[1] pull up/down control bit10 - GPIO3B[2] pull up/down control ... bit15 - GPIO3B[7] pull up/down control
7:0	RW	0x00	gpio3a_pull GPIO3A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO3A[0] pull up/down control bit1 - GPIO3A[1] pull up/down control bit2 - GPIO3A[2] pull up/down control ... bit7 - GPIO3A[7] pull up/down control

GRF_GPIO3H_PULL

Address: Operational Base + offset (0x0134)

GPIO3C / GPIO3D pull up/down control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio3d_pull GPIO3d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit8 - GPIO3D[0] pull up/down control bit9 - GPIO3D[1] pull up/down control bit10 - GPIO3D[2] pull up/down control ... bit15 - GPIO3D[7] pull up/down control
7:0	RW	0x00	gpio3c_pull GPIO3C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 0: pull up/down enable, PAD type will decide to be up or down ,not related with this value 1: pull up/down disable bit0 - GPIO3C[0] pull up/down control bit1 - GPIO3C[1] pull up/down control bit2 - GPIO3C[2] pull up/down control ... bit7 - GPIO3C[7] pull up/down control

GRF_ACODEC_CON

Address: Operational Base + offset (0x013c)

SoC control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit 0~bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:6	RO	0x0	reserved
5:4	RW	0x2	acodec_detectn_debounce_sel acodec_detectn debounce time select 00:5ms 01:15ms 10:35ms 11:50ms
3	RW	0x0	acodec_detectn_fall_int_en acodec detectn negedge interrupt enable 0: interrupt disable 1: interrupt enable
2	RW	0x0	acodec_detectn_rise_int_en acodec detectn posedge interrupt enable 0: interrupt disable 1: interrupt enable
1	RW	0x0	acodec_detectn_fall_int_pd acodec detectn negedge interrupt pending bit wirte 1 to it, it will be cleared.
0	RW	0x0	acodec_detectn_rise_int_pd acodec detectn posedge interrupt pending bit wirte 1 to it, it will be cleared.

GRF_SOC_CON0

Address: Operational Base + offset (0x0140)

SoC control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit 0~bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	hdmiphy_dclk_sel 1'b0: dclk from lcdc 1'b1: dclk from cru
14	RW	0x0	ddr_16bit_en When 16bit ddr is used , this bit should be 1.
13	RW	0x0	msch4_mainpartialpop 0:16bit ddr 1:8bit ddr
12	RW	0x0	soc_remap remap bit control When soc_remap = 1, the bootrom is mapped to address 0x10100000 and internal memory is mapped to address 0x0.
11	RW	0x0	acodec_ad2da_loop acodec loopback enable 0 : acodec loopback disable 1: acodec loopback enable
10	RW	0x0	acodec_sel 0: i2s_sdi from gpio is selected 1: i2s_sdi from acodec is selected
9	RO	0x0	reserved
8	RW	0x1	force_jtag this bit is used to force iomux to jtag. 0: disable 1: enable
7	RW	0x0	mobile_ddr_sel this bit is used to tell ddr monitor the type of ddr used. 0: DDR2/DDR3 1: LPDDR2/LPDDR3
6	RW	0x0	dfi_eff_stat_en dfi monitor start to work. 1: dfi monitor works. 0: dfi monitor stops.

Bit	Attr	Reset Value	Description
5:4	RW	0x2	sd_detectn_debounce_sel sd_detectn debounce time select 00:5ms 01:15ms 10:35ms 11:50ms
3	RW	0x0	sd_detectn_fall_int_en SD detectn negedge interrupt enable 0: interrupt disable 1: interrupt enable
2	RW	0x0	sd_detectn_rise_int_en SD detectn posedge interrupt enable 0: interrupt disable 1: interrupt enable
1	RW	0x0	sd_detectn_fall_int_pd SD detectn negedge interrupt pending bit wirte 1 to it, it will be cleared.
0	RW	0x0	sd_detectn_rise_int_pd SD detectn posedge interrupt pending bit wirte 1 to it, it will be cleared.

GRF_SOC_CON1

Address: Operational Base + offset (0x0144)

SoC control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit 0~bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	hevc_vpu_sel hevc vpu select 0: select vpu 1: select hevc
14	RW	0x0	mipi_phy_lane3_enable MIPI phy enalbe lane3 in TTL mode 0: not TTL mode 1: TTL mode

Bit	Attr	Reset Value	Description
13	RW	0x0	mipi_phy_lane2_enable MIPI phy enalbe lane2 in TTL mode 0: not TTL mode 1: TTL mode
12	RW	0x0	mipi_lane1_enable MIPI phy enalbe lane1 in TTL mode 0: not TTL mode 1: TTL mode
11	RW	0x0	mipi_phy_lane0_enable MIPI phy enalbe lane0 in TTL mode 0: not TTL mode 1: TTL mode
10	RW	0x0	vpu_sel vdpu vepu clock select 0: select vepu aclk as vpu main clock 1: select vdpu aclk as vpu main clock
9:8	RO	0x0	reserved
7	RW	0x0	mipi_phy_enableck MIPI phy enalbe ck in TTL mode 0: not TTL mode 1: TTL mode
6	RW	0x0	emmc_iomux_sel emmc iomux select 0: select 3026 sdmmc iomux 1: select new iomux
5	RW	0x0	i2s_iomux_sel i2s iomux select 0: select 3026 sdmmc iomux 1: select new iomux
4:3	RW	0x0	spi_iomux_sel spi iomux select 00: select 3026 sdmmc iomux 01: select new iomux1 10: select new iomux2
2:0	RO	0x0	reserved

GRF_SOC_CON2
Address: Operational Base + offset (0x0148)
SoC control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	crypto_pwr_idlereq NOC idle request, high valid.
14	RW	0x0	msch_pwr_idlereq NOC idle request, high valid.
13	RW	0x0	core_pwr_idlereq NOC idle request, high valid.
12	RW	0x0	peri_pwr_idlereq NOC idle request, high valid.
11	RW	0x0	vio_pwr_idlereq NOC idle request, high valid.
10	RW	0x0	vpu_pwr_idlereq NOC idle request, high valid.
9	RW	0x0	gpu_pwr_idlereq NOC idle request, high valid.
8	RW	0x0	sys_pwr_idlereq NOC idle request, high valid.
7	RW	0x1	msch4_mainddr3 When DDR3 is used , software should configure this bit to 1.
6:4	RO	0x0	reserved
3	RW	0x0	usb_host_sel usb host select 0: select ehci usb host 1: select old usb host
2	RW	0x1	ddrphy_low_power_en ddrphy low power enable 1'b0: ddrphy into low-power 1'b1: normal
1	RW	0x0	upctl_c_sysreq software config enter DDR self-refresh by lowpower interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh

Bit	Attr	Reset Value	Description
0	RW	0x0	upctl_c_active_in ddr clock active in. External signal from system that flags if a hardware low power request can be accepted or should always be denied. 0: may be accepted 1: will be denied

GRF_SOC_STATUS0

Address: Operational Base + offset (0x014c)

SoC status register

Bit	Attr	Reset Value	Description
31	RO	0x0	acodec_hpdet The flag indicates whether has the headset to be inserted. 1: having headset to be inserted. 0:don't have.
30	RO	0x0	reserved
29	RO	0x0	crypto_pwr_idle NOC idle state. "1" indicates idle.
28	RO	0x0	msch_pwr_idle NOC idle state. "1" indicates idle.
27	RO	0x0	sys_pwr_idle NOC idle state. "1" indicates idle.
26	RO	0x0	gpu_pwr_idle NOC idle state. "1" indicates idle.
25	RO	0x0	vpu_pwr_idle NOC idle state. "1" indicates idle.
24	RO	0x0	vio_pwr_idle NOC idle state. "1" indicates idle.
23	RO	0x0	peri_pwr_idle NOC idle state. "1" indicates idle.
22	RO	0x0	core_pwr_idle NOC idle state. "1" indicates idle.
21	RO	0x0	crypto_pwr_idleack NOC idle acknowledge. high valid.
20	RO	0x0	msch_pwr_idleack NOC idle acknowledge. high valid.
19	RO	0x0	sys_pwr_idleack NOC idle acknowledge. high valid.
18	RO	0x0	gpu_pwr_idleack NOC idle acknowledge. high valid.
17	RO	0x0	vpu_pwr_idleack NOC idle acknowledge. high valid.
16	RO	0x0	vio_pwr_idleack NOC idle acknowledge. high valid.
15	RO	0x0	peri_pwr_idleack NOC idle acknowledge. high valid.
14	RO	0x0	core_pwr_idleack NOC idle acknowledge. high valid.

Bit	Attr	Reset Value	Description
13	RO	0x0	host20_iddig host2.0 iddig state. it will always be "0".
12:11	RO	0x0	host20_linestate host 2.0 linestate status This bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 2'b11: SE1 (D+ high, D- high) 2'b10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 2'b01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 2'b00: SE0 (D+ low, D- low) During normal high-speed packet transfers, the line indicates a high-speed J state.
10	RO	0x0	host20_bvalid host 2.0 bvalid status B-Device Session Valid Indicator Function: This controller signal is output from the USB 2.0 Session Valid comparator and indicates whether the session for a B-device is valid. 1: The session for the B-device is valid. 0: The session for the B-device is not valid.
9	RO	0x0	host20_vbusvalid host 2.0 vbus valid status VBUS Valid Indicator Function: This controller signal is output from the USB 2.0 VBUS Valid comparator and indicates whether the VBUS output is at a valid level. 1: The VBUS output is valid. 0: The VBUS output is not valid.
8	RO	0x0	otg0_iddig otg iddig status 0: indicate otg work as host 1: indicate otg work as device

Bit	Attr	Reset Value	Description
7:6	RO	0x0	otg_linestate otg linestate status This bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 2'b11: SE1 (D+ high, D- high) 2'b10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 2'b01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 2'b00: SE0 (D+ low, D- low) During normal high-speed packet transfers, the line indicates a high-speed J state.
5	RO	0x0	otg_bvalid otg bvalid status B-Device Session Valid Indicator Function: This controller signal is output from the USB 2.0 Session Valid comparator and indicates whether the session for a B-device is valid. 1: The session for the B-device is valid. 0: The session for the B-device is not valid.
4	RO	0x0	otg_vbusvalid otg vbus valid status VBUS Valid Indicator Function: This controller signal is output from the USB 2.0 VBUS Valid comparator and indicates whether the VBUS output is at a valid level. 1: The VBUS output is valid. 0: The VBUS output is not valid.
3:0	RO	0x0	pll_lock Pll lock status :generalpll_lock, codecpll_lock,armpll_lock,ddrpll_lock 1: pll is lock 0: pll is unlock

GRF_LVDS_CON0

Address: Operational Base + offset (0x0150)

LVDS control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0 ~ bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13	RW	0x0	mipi_phy_lane3_forcexmode MIPI phy lane3 force x mode 0: disable 1: enable
12	RW	0x0	mipi_phy_lane2_forcexmode MIPI phy lane2 force x mode 0: disable 1: enable
11	RW	0x0	mipi_phy_lane1_forcexmode MIPI phy lane1 force x mode 0: disable 1: enable
10	RW	0x0	mipi_phy_lane0_forcexmode MIPI phy lane0 force x mode 0: disable 1: enable
9	RW	0x0	mipi_dsi_forcexmode MIPI phy force x mode 0: disable 1: enable
8	RW	0x0	mipi_phy_lane0_turndisable MIPI phy lane0 turndisable
7	RW	0x0	mipi_phy_ttl_mode MIPI phy work in TTL mode 0: disable 1: enable
6	RW	0x0	lvds_mode work in lvds mode 0: disable 1: enable
5	RW	0x0	mipi_ctrl_dpicoloorm MIPI controller dpi colorm 0: disable 1: enable

Bit	Attr	Reset Value	Description
4	RW	0x0	mipi_ctrl_dpishutdown MIPI controller dpi shut down 0: disable 1: enable
3	RW	0x0	lvds_msbsel LVDS lane input format 0: MSB is on D0 1: MSB is on D7
2:1	RW	0x0	lvds_select LVDS output format 00: 8bit mode format-1 01: 8bit mode format-2 10: 8bit mode format-3 11: 6bit mode
0	RW	0x0	ebc_mac_sel LVDS data from ebc or mac or lvds selection 1'b0 : lvds 1'b1 : ebc

GRF_DMAC_CON0

Address: Operational Base + offset (0x015c)

DMAC control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:1	RO	0x0	reserved
0	RW	0x0	dmac_boot_from_pc DMAC boot_from_pc input control Controls the location in which the DMAC executes its initial instruction, after it exits from reset : 0= DMAC waits for an instruction from APB interface 1= DMAC manager thread executes the instruction that is located at the address that boot_addr[31:0] provided.

GRF_DMAC_CON1

Address: Operational Base + offset (0x0160)

DMAC control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	dmac_boot_addr dmac_boot_addr[27:12] DMAC boot_addr[27:12] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

GRF_DMAC_CON2

Address: Operational Base + offset (0x0164)

DMAC control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x1	dmac_drtype DMAC type of acknowledgement or request for peripheral signals: 00 : single level request 01 ： burst level request 10 ： acknowledging a flush request 11 ： reserved
3:0	RW	0x0	dmac_boot_addr dmac_boot_addr[31:28] DMAC boot_addr[31:28] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

GRF_MAC_CON0
Address: Operational Base + offset (0x0168)
GMAC control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	rxclk_dly_ena_gmac RGMII RX clock delayline enable 1'b1: enable 1'b0: disable
14	RW	0x0	txclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
13:7	RW	0x10	clk_rx_dl_cfg_gmac RGMII RX clock delayline value
6:0	RW	0x10	clk_tx_dl_cfg_gmac RGMII TX clock delayline value

GRF_MAC_CON1
Address: Operational Base + offset (0x016c)

GMAC control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x1	rmii_mode RMII mode selection 1'b1: RMII mode
13:12	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
11	RW	0x0	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
10	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
9	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
8:6	RW	0x1	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
5:0	RO	0x0	reserved

GRF_TVE_CON

Address: Operational Base + offset (0x0170)

TV encoder control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:7	RW	0x00	gain gain
6	RW	0x0	enctr2 enctr2
5	RW	0x0	enctr1 enctr1
4	RW	0x0	enctr0 enctr0
3	RW	0x0	ensc0 ensc0
2	RW	0x0	endac endac
1	RW	0x0	envbg envbg
0	RW	0x0	enextref enextref

GRF_UOC0_CON0
Address: Operational Base + offset (0x017c)
OTG control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit 0 ~ bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	otg0_bvalid_irq_pd otg0 bvalid interrupt pending bit write 1 to this bit , it will be cleared.
14	RW	0x0	otg0_bvalid_irq_en otg0 bvalid interrupt enable 1: interrupt enable 0: interrupt disable
13	RW	0x0	otg0_linestate_irq_pd otg0 linestate interrupt pending write 1 to this bit , it will be cleared.
12	RW	0x0	otg0_linestate_irq_en otg0 linestate change interrupt enable 1: interrupt enable 0: interrupt disable
11	RO	0x0	reserved
10	RW	0x0	iddig_status control software iddig value 0:host 1:device
9	RW	0x0	iddig_sft_sel 0 : iddig to otg controller select usbphy output 1: iddig to otg controller select grf_uoc0_con5[10]
8	RW	0x0	utmi_dmpulldown 0: DM 15 KOhm pull down disabled 1: DM 15 Kohm pull down enable
7	RW	0x0	utmi_dppulldown 0: DP 15 KOhm pull down disabled 1: DP 15 Kohm pull down enable
6	RW	0x0	utmi_termselect USB Termination Select 1: Full-speed terminations are enabled. 0: High-speed terminations are enabled.

Bit	Attr	Reset Value	Description
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 11: Sends an LS packet on an FS bus or receives an LS packet. 10: LS Transceiver 01: FS Transceiver 00: HS Transceiver
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 00 while OPMODE[1:0] is set to 11, USB PHY behavior is undefined. 10: Disable bit stuffing and NRZI encoding 01: Non-Driving 00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1: Normal operating mode 0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 0: software control usb phy disable 1 : software control usb phy enable

GRF_UOC1_CON1
Address: Operational Base + offset (0x0184)
usb host control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	usbphy1_vdm_src_en open dm voltage source
11	RW	0x0	usbphy1_vdp_src_en open dp voltage source

Bit	Attr	Reset Value	Description
10	RW	0x0	usbphy1_rdm_pdwn_en open dm pull down resistor
9	RW	0x0	usbphy1_idp_src_en open dp source current
8	RW	0x0	usbphy1_idm_sink_en open dm sink current enable
7	RW	0x0	usbphy1_idp_sink_en open dp sink current enable
6:0	RO	0x0	reserved

GRF_UOC1_CON2
Address: Operational Base + offset (0x0188)
UOC1 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	usbhost0_incr4_en USB HOST0 incr4_en bit control
14	RW	0x1	usbhost0_incr16_en USB HOST0 incr16_en bit control
13	RW	0x0	usbhost0_hubsetup_min USB HOST0 hubsetup_min bit control
12	RW	0x0	usbhost0_app_start_clk USB HOST0 app_start_clk bit control
11:6	RW	0x20	usbhost0_fladj_val_common USB HOST0 fladj_val_common bit control
5:0	RW	0x20	usbhost0_fladj USB HOST0 fladj bit control

GRF_UOC1_CON3
Address: Operational Base + offset (0x018c)
UOC1 control register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
14	RW	0x0	usbhost0_ohci_cntsel USB HOST0 ohci_cntsel bit control
13	RW	0x0	usbhost0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
12	RO	0x0	reserved
11	RW	0x1	usbhost0_word_if USB HOST0 word_if bit control
10	RW	0x0	usbhost0_sim_mode USB HOST0 sim_mode bit control
9	RW	0x1	usbhost0_incrx_en USB HOST0 incrx_en bit control
8	RW	0x1	usbhost0_incr8_en USB HOST0 incr8_en bit control
7	RO	0x0	reserved
6	RW	0x1	usbhost0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit conrol
5:1	RO	0x0	reserved
0	RW	0x0	usbhost0_autoppd_on_overcur USB HOST0 autoppd_on_overcur bit control

GRF_UOC1_CON4

Address: Operational Base + offset (0x0190)

USB HOST 2.0 control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbphy_commonon USBPHY common on
14	RO	0x0	reserved
13	RW	0x0	bypasssel0 Transmitter Digital Bypass mode Enable. When 1, otg used as a uart port.
12	RW	0x0	bypassdmen0 DM0 Transmitter Digital Bypass Enable. high valid.
11	RW	0x0	host20disable when 1, host 2.0 phy disable
10	RW	0x0	otgphydisable when 1, otgphy is disabled.
9:8	RO	0x0	reserved
7:6	RW	0x0	utmihost_scaledown_mode utmihost scaledown mode
5	RW	0x0	utmiotg_idpullup Analog ID Input Sample Enable Function: This controller signal controls ID line sampling. 1: ID pin sampling is enabled, and the IDDIG output is valid. 0: ID pin sampling is disabled, and the IDDIG output is not valid.
4	RW	0x1	utmiotg_dppulldown D+ Pull-Down Resistor Enable
3	RW	0x1	utmiotg_dmpulldown D- Pull-Down Resistor Enable
2	RW	0x1	utmiotg_drvvbus Drive VBUS 1: The VBUS Valid comparator is enabled. 0: The VBUS Valid comparator is disabled.
1	RW	0x0	utmisrp_chrgvbus VBUS Input Charge Enable
0	RW	0x0	utmisrp_dischrgvbus VBUS Input Discharge Enable

GRF_UOC1_CON5
Address: Operational Base + offset (0x0194)
USB HOST 2.0 control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit 0 ~ bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	otg1_linestate_irq_pd otg1 linestate interrupt pending write 1 to this bit , it will be cleared.
14	RW	0x0	otg1_linestate_irq_en otg1 linestate interrupt enable
13:9	RO	0x0	reserved
8	RW	0x0	utmi_dmpulldown 0: DM 15 KOhm pull down disabled 1: DM 15 Kohm pull down enable
7	RW	0x0	utmi_dppulldown 0: DP 15 KOhm pull down disabled 1: DP 15 Kohm pull down enable
6	RW	0x0	utmi_termselect USB Termination Select 1: Full-speed terminations are enabled. 0: High-speed terminations are enabled.
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 11: Sends an LS packet on an FS bus or receives an LS packet. 10: LS Transceiver 01: FS Transceiver 00: HS Transceiver

Bit	Attr	Reset Value	Description
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 00 while OPMODE[1:0] is set to 11, USB PHY behavior is undefined. 10: Disable bit stuffing and NRZI encoding 01: Non-Driving 00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1: Normal operating mode 0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 0: software control usb phy disable 1 : software control usb phy enable

GRF_DDRC_STAT

Address: Operational Base + offset (0x019c)

DDRC status

Bit	Attr	Reset Value	Description
31:21	RW	0x000	gpu_idle gpu idle staus
20	RW	0x0	ddrupctl_c_active confirm that system external to PCTL can accept a Low-power request. high valid.
19	RW	0x0	upctl_c_sysack PCTL low-power request status response. high valid.
18:16	RO	0x0	ddrupctl_stat Current state of the protocol controller 3'b000 = Init_mem 3'b001 = Config 3'b010 = Config_req 3'b011 = Access 3'b100 = Access_req 3'b101 = Low_power 3'b110 = Low_power_entry_req 3'b111 = Low_power_exit_req
15:0	RO	0x0000	ddrupctl_bbflags Bank busy indication NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.

GRF_SOC_STATUS1
Address: Operational Base + offset (0x01a4)
SoC status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RO	0x0	mipi_ctrl_edpihalt
9	RO	0x0	mipi_ctrl_shutdown
8	RO	0x0	mipi_ctrl_rstz
7	RO	0x0	mipi_ctrl_forcepll
6	RO	0x0	gmac_portselect
5:0	RO	0x00	timer_en_status bit 0 : timer 0 enable status bit 1 : timer 1 enable status 1 means timer is enabled.

GRF_CPU_CON0
Address: Operational Base + offset (0x01a8)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0 ~ bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	l2_data_latency select L2 data ram write latency: 0: new design 1: old design
14	RO	0x0	reserved
13	RW	0x1	deviceen_dap Enabling access to the connected debug device or memory system 0: disable 1: enable

Bit	Attr	Reset Value	Description
12	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset. high valid.
11:8	RW	0x0	l1rstdisable Disable automatic data cache, instruction cache and TLB invalidate at reset. 4bits coresponding 4 cores. high valid.
7:3	RO	0x0	reserved
2:0	RW	0x2	ema_mem_ctrl memory EMA signal control

GRF_CPU_CON1
Address: Operational Base + offset (0x01ac)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0 ~ bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	cfgte_a7 Controls processor state for exception handling (TE bit) at reset.
7:4	RW	0x0	vinithi_a7 Cortex-A7 vinithi bit control. location of the exception vectors at reset. Sampled during reset. 0= 0x0000_0000 1= 0xffff_0000
3:0	RW	0x0	cfgend_a7 One bit for each processor. 0 = Little-endian 1 = Big-endian

GRF_CPU_CON2
Address: Operational Base + offset (0x01b0)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	wirte_enable bit0 ~ bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8	RW	0x0	cfgsdisable Disables write access to some secure GIC registers. When CFGSDISABLE is asserted, the GIC prevents writes to any register locations that control the operating state of an LSPI 1'b0: enable 1'b1: disable
7	RW	0x0	evento_clear Event output. evento is active when one SEV instruction is executed. this bit used to clear evento signal. 1'b0: un-clear 1'b1: clear
6	RW	0x0	eventi Event input for processor wake-up from WFE state. This pin must be asserted for at least one CLKIN clock cycle. When this signal is asserted, it acts as a WFE wake-up event to all the processors in the multiprocessor device.
5	RW	0x1	dbgselfaddrv Debug self-address offset valid 1'b0: unvalid 1'b1: valid
4	RW	0x1	dbgromaddrv Debug ROM physical address valid: 1'b0: unvalid 1'b1: valid
3	RW	0x1	spniden Secure privileged non-invasive debug enable
2	RW	0x1	niden Non-invasive debug enable

Bit	Attr	Reset Value	Description
1	RW	0x1	spiden Secure privileged invasive debug enable
0	RW	0x1	dbgen Debug enable

GRF_CPU_CON3
Address: Operational Base + offset (0x01b4)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0 ~ bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_CPU_STATUS0
Address: Operational Base + offset (0x01c0)
CPU status register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:3	RO	0x0	smpnamp_a7 Signals AMP or SMP mode for each Cortex-A7 processor. 0 Asymmetric. 1 Symmetric.
2	RO	0x0	jtagnsw_dap coresight jtagnsw signal status 1: JTAG is selected. 0: SWD is selected.
1	RO	0x0	jtagtop_dap coresight jtagtop signal status "1" means jtag state machine is in one of the top four modes: test-logic-reset, run-test/idle, select-DR-scan, select-IR-scan.
0	RO	0x0	evento_rising_edge evento signal rising edge status

GRF_CPU_STATUS1
Address: Operational Base + offset (0x01c4)
CPU status register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:5	RO	0x0	core_wfi_status core WFI status, 4bit coresponding 4 cores.
4:1	RO	0x0	core_wfe_status core WFE status, 4bit coresponding 4 cores.
0	RO	0x0	l2c_wfi_status L2 WFI status.

GRF_OS_REG0
Address: Operational Base + offset (0x01c8)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG1
Address: Operational Base + offset (0x01cc)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG2
Address: Operational Base + offset (0x01d0)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG3
Address: Operational Base + offset (0x01d4)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG4
Address: Operational Base + offset (0x01d8)
software OS register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG5
Address: Operational Base + offset (0x01dc)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG6
Address: Operational Base + offset (0x01e0)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_OS_REG7
Address: Operational Base + offset (0x01e4)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg software OS register

GRF_PVTM_CON0
Address: Operational Base + offset (0x0200)
PVTM control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	pvtm_func_osc_en func PVT monitor oscilator enable 1'b1: enable 1'b0: disable
12	RW	0x0	pvtm_func_start func PVT monitor start control
11:10	RO	0x0	reserved
9	RW	0x0	pvtm_gpu_osc_en pd_gpu PVT monitor oscilator enable 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_gpu_start pd_gpu PVT monitor start control
7:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en pd_core PVT monitor oscilator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start pd_core PVT monitor start control

GRF_PVTM_CON1
Address: Operational Base + offset (0x0204)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_cal_cnt pd_core pvtm calculator counter

GRF_PVTM_CON2
Address: Operational Base + offset (0x0208)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_cal_cnt pd_gpu pvtm calculator counter

GRF_PVTM_CON3
Address: Operational Base + offset (0x020c)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_func_cal_cnt func pvtm calculator counter

GRF_PVTM_STATUS0
Address: Operational Base + offset (0x0210)
PVTM status register0

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	pvtm_func_freq_done func pvtm frequency calculate done stutus
1	RO	0x0	pvtm_core_freq_done pd_core pvtm frequency calculate done stutus
0	RO	0x0	pvtm_gpu_freq_done pd_gpu pvtm frequency calculate done stutus

GRF_PVTM_STATUS1
Address: Operational Base + offset (0x0214)
PVTM status register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_freq_cnt pd_core pvtm frequency count

GRF_PVTM_STATUS2
Address: Operational Base + offset (0x0218)
PVTM status register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_freq_cnt pd_gpu pvtm frequency count

GRF_PVTM_STATUS3
Address: Operational Base + offset (0x021c)
PVTM status register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_freq_cnt pd_gpu pvtm frequency count

GRF_DFI_WRNUM
Address: Operational Base + offset (0x0220)
DFI write number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_wr_num the total number of write operation on DFI interface.

GRF_DFI_RDNUM
Address: Operational Base + offset (0x0224)
DFI read number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_rd_num the total number of read operation on DFI interface.

GRF_DFI_ACTNUM
Address: Operational Base + offset (0x0228)
DFI active number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_act_num the total number of active operation on DFI interface.

GRF_DFI_TIMERVAL
Address: Operational Base + offset (0x022c)
DFI work time

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_timer_val the total time for DFI monitor works.

GRF_NIF_FIFO0
Address: Operational Base + offset (0x0230)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo0 status for msch4 signals. It will not be cleared by system reset. bit 10 ~ bit 0 : msch4_n_acol[10:0] bit 11 ~ bit 13 : msch4_n_abank[2:0] bit 14 ~ bit 29 : msch4_n_arow[15:0] bit 31 ~ bit 30 : msch4_n_arank_sel[1:0]

GRF_NIF_FIFO1
Address: Operational Base + offset (0x0234)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo1 status for msch4 signals. It will not be cleared by system reset. bit 10 ~ bit 0 : msch4_n_acol[10:0] bit 11 ~ bit 13 : msch4_n_abank[2:0] bit 14 ~ bit 29 : msch4_n_arow[15:0] bit 31 ~ bit 30 : msch4_n_arank_sel[1:0]

GRF_NIF_FIFO2
Address: Operational Base + offset (0x0238)
NIF status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo2 status for msch4 signals. It will not be cleared by system reset. bit 10 ~ bit 0 : msch4_n_acol[10:0] bit 11 ~ bit 13 : msch4_n_abank[2:0] bit 14 ~ bit 29 : msch4_n_arow[15:0] bit 31 ~ bit 30 : msch4_n_arank_sel[1:0]

GRF_NIF_FIFO3

Address: Operational Base + offset (0x023c)

NIF status register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo3 status for msch4 signals. It will not be cleared by system reset. bit 10 ~ bit 0 : msch4_n_acol[10:0] bit 11 ~ bit 13 : msch4_n_abank[2:0] bit 14 ~ bit 29 : msch4_n_arow[15:0] bit 31 ~ bit 30 : msch4_n_arank_sel[1:0]

GRF_USBPHY0_CON0

Address: Operational Base + offset (0x0280)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x4	squel_trigger_con bit 2 ~ bit 0 of squel_trigger_con. 0000:112.5mV 1001:162.5mV 1011:175mV 1100:150mV(default) 1110:125mV

Bit	Attr	Reset Value	Description
12:11	RW	0x0	non_driving Registers for non-driving state control. non-driving state is controlled by op-mode by default, when bit[11] is configured with "1", user can control non-driving state trough bit[12].
10:8	RW	0x6	tx_clk_phase_con USB Tx Clock phase configure, 000 represent the earliest phase , and 111 the latest, single step delay is 256ps
7:5	RW	0x0	rx_clk_phase_con USB Rx Clock phase configure,000 represent the earliest phase , and 111 the latest, single step delay is 256ps
4:3	RW	0x3	fls_eye_height FS/LS eye height configure , 00 represent the largest slew rate , 11 represent the smallest slew rate
2:0	RW	0x0	hs_eye_diag_adjust HS eye diagram adjust, open HS pre-emphasize function to increase HS slew rate, only used when large cap loading is attached. 001:open pre-emphasize in sof or eop state 010: open pre-emphasize in chirp state 100: open pre-emphasize in non-chirp state 111: always open pre-emphasize other combinations : reserved

GRF_USBPHY0_CON1
Address: Operational Base + offset (0x0284)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:13	RW	0x7	hs_eye_height bit2 ~ bit 0 of hs_eye_height. HS eye height tuning ,more zeros represent bigger eye, more ones represent smaller eye
12:3	RO	0x0	reserved
2	RW	0x1	current_comp_en Enable current compensation, active high.
1	RW	0x1	res_comp_en Enable resistance compensation, active high.
0	RW	0x1	squel_trigger_con bit 3 of squel_trigger_con. 0000:112.5mV 1001:162.5mV 1011:175mV 1100:150mV(default) 1110:125mV

GRF_USBPHY0_CON2

Address: Operational Base + offset (0x0288)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	odt_compensation bit 0 of odt_compensation. ODT Compensation voltage reference 000:200mV 001:187.5mV(default) 010:225mV 110:175mV 111:162.5mV
14:13	RW	0x0	voltage_tolerance_adjust 5V tolerance detection reference adjust, 11 represent the highest trigger point, keeping the default value is greatly appreciated
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	auto_compensation_bypass auto compensation bypass , "11" will bypass current and ODT compensation, customers can set the driver strength and current manually. For larger HS eye height, customer can give more "0" for hs_eye_height; For larger HS/FS/LS slew rate , give more "1" for hfs_driver_strength.
9:5	RW	0x15	hfs_driver_strength HS/FS driver strength tuning , "11111" represent the largest slew rate and "10000" represents the smallest slew rate
4:0	RW	0x0a	hs_eye_height bit7 ~ bit 3 of hs_eye_height. HS eye height tuning ,more zeros represent bigger eye, more ones represent smaller eye

GRF_USBPHY0_CON3

Address: Operational Base + offset (0x028c)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	vol_toleran_det_con 5V tolerance detection function controlling bit trough registers, only active when bit[65] is set "1".
13:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x1	odt_auto_refresh A port ODT auto refresh bypass, active low, this register should only be used when auto_compensation_bypass were set to "11". In bypass mode , customer can configure driver strength through hfs_driver_strength.
8	RW	0x0	bg_out_voltage_adjust BG output voltage reference adjust, keeping the default value is greatly appreciated.
7:5	RW	0x0	compen_current_ref compensation current tuning reference 000:200mV(default) 001:187.5mV 010:225mV 110:175mV 111:162.5mV
4:2	RW	0x0	bias_current_ref bias current tuning reference 000:400mV(default) 001:362.5mV 010:350mV 101:425mV 111:450mV
1:0	RW	0x0	odt_compensation bit 2 ~ bit 1 of odt_compensation. ODT Compensation voltage reference 000:200mV 001:187.5mV(default) 010:225mV 110:175mV 111:162.5mV

GRF_USBPHY0_CON4

Address: Operational Base + offset (0x0290)

usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1	RW	0x1	bypass_5v_tolerance_det Bypass 5V tolerance detection function, active high
0	RO	0x0	reserved

GRF_USBPHY0_CON5
Address: Operational Base + offset (0x0294)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_USBPHY0_CON6
Address: Operational Base + offset (0x0298)
usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x0	session_end_con session_end reference tuning
12:10	RW	0x0	b_session_con B_sessionvalid reference tuning
9:7	RW	0x0	a_session_con A_sessionvalid reference tuning
6	RW	0x0	force_vbus_valid force output vbus_valid asserted, active high
5	RW	0x0	force_session_end_val force output session_end asserted, active high
4	RW	0x0	force_b_session_val force output B_sessionvalid asserted, active high
3	RW	0x0	force_a_session_val force output A_sessionvalid asserted, active high
2	RW	0x1	turn_off_diff_receiver Turn off differential receiver in suspend mode to save power, active low.
1:0	RO	0x0	reserved

GRF_USBPHY0_CON7

Address: Operational Base + offset (0x029c)

usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:11	RW	0xd	host_discon_con HOST disconnect detection trigger point configure, only used in HOST mode 0000: 575mV 0001: 600mV 1001:625mV 1101:650mV(default)
10:8	RO	0x0	reserved
7	RW	0x1	bypass_squelch_trigger bypass squelch trigger point auto configure in chirp modes , active high
6	RW	0x1	half_bit_pre_empha_en half bit pre-emphasize enable, active high. "1" represent half bit pre-emphasis , "0" for full bit
5:3	RO	0x0	reserved
2:0	RW	0x0	vbus_valid_con vbus_valid reference tuning

GRF_USBPHY1_CON0

Address: Operational Base + offset (0x02a0)

usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x4	squel_trigger_con bit 2 ~ bit 0 of squel_trigger_con. 0000:112.5mV 1001:162.5mV 1011:175mV 1100:150mV(default) 1110:125mV
12:11	RW	0x0	non_driving Registers for non-driving state control. non-driving state is controlled by op-mode by default, when bit[11] is configured with "1", user can control non-driving state trough bit[12].
10:8	RW	0x6	tx_clk_phase_con USB Tx Clock phase configure, 000 represent the earliest phase , and 111 the latest, single step delay is 256ps
7:5	RW	0x0	rx_clk_phase_con USB Rx Clock phase configure,000 represent the earliest phase , and 111 the latest, single step delay is 256ps
4:3	RW	0x3	fls_eye_height FS/LS eye height configure , 00 represent the largest slew rate , 11 represent the smallest slew rate
2:0	RW	0x0	hs_eye_diag_adjust HS eye diagram adjust, open HS pre-emphasize function to increase HS slew rate, only used when large cap loading is attached. 001:open pre-emphasize in sof or eop state 010: open pre-emphasize in chirp state 100: open pre-emphasize in non-chirp state 111: always open pre-emphasize other combinations : reserved

GRF_USBPHY1_CON1
Address: Operational Base + offset (0x02a4)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x7	hs_eye_height bit2 ~ bit 0 of hs_eye_height. HS eye height tuning ,more zeros represent bigger eye, more ones represent smaller eye
12:3	RO	0x0	reserved
2	RW	0x1	current_comp_en Enable current compensation, active high.
1	RW	0x1	res_comp_en Enable resistance compensation, active high.
0	RW	0x1	squel_trigger_con bit 3 of squel_trigger_con. 0000:112.5mV 1001:162.5mV 1011:175mV 1100:150mV(default) 1110:125mV

GRF_USBPHY1_CON2
Address: Operational Base + offset (0x02a8)
usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	odt_compensation bit 0 of odt_compensation. ODT Compensation voltage reference 000:200mV 001:187.5mV(default) 010:225mV 110:175mV 111:162.5mV
14:13	RW	0x0	voltage_tolerance_adjust 5V tolerance detection reference adjust, 11 represent the highest trigger point, keeping the default value is greatly appreciated
12	RO	0x0	reserved
11:10	RW	0x0	auto_compensation_bypass auto compensation bypass , "11" will bypass current and ODT compensation, customers can set the driver strength and current manually. For larger HS eye height, customer can give more "0" for hs_eye_height; For larger HS/FS/LS slew rate , give more "1" for hfs_driver_strength.
9:5	RW	0x15	hfs_driver_strength HS/FS driver strength tuning , "11111" represent the largest slew rate and "10000" represents the smallest slew rate
4:0	RW	0x0a	hs_eye_height bit7 ~ bit 3 of hs_eye_height. HS eye height tuning ,more zeros represent bigger eye, more ones represent smaller eye

GRF_USBPHY1_CON3

Address: Operational Base + offset (0x02ac)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	vol_toleran_det_con 5V tolerance detection function controlling bit trough registers, only active when bit[65] is set "1".
13:10	RO	0x0	reserved
9	RW	0x1	odt_auto_refresh A port ODT auto refresh bypass, active low, this register should only be used when auto_compensation_bypass were set to "11". In bypass mode , customer can configure driver strength through hfs_driver_strength.
8	RW	0x0	bg_out_voltage_adjust BG output voltage reference adjust, keeping the default value is greatly appreciated.
7:5	RW	0x0	compen_current_ref compensation current tuning reference 000:200mV(default) 001:187.5mV 010:225mV 110:175mV 111:162.5mV
4:2	RW	0x0	bias_current_ref bias current tuning reference 000:400mV(default) 001:362.5mV 010:350mV 101:425mV 111:450mV

Bit	Attr	Reset Value	Description
1:0	RW	0x0	odt_compensation bit 2 ~ bit 1 of odt_compensation. ODT Compensation voltage reference 000:200mV 001:187.5mV(default) 010:225mV 110:175mV 111:162.5mV

GRF_USBPHY1_CON4

Address: Operational Base + offset (0x02b0)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1	RW	0x1	bypass_5v_tolerance_det Bypass 5V tolerance detection function, active high
0	RO	0x0	reserved

GRF_USBPHY1_CON5

Address: Operational Base + offset (0x02b4)

usbphy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RO	0x0	reserved

GRF_USBPHY1_CON6
Address: Operational Base + offset (0x02b8)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RW	0x0	session_end_con session_end reference tuning
12:10	RW	0x0	b_session_con B_sessionvalid reference tuning
9:7	RW	0x0	a_session_con A_sessionvalid reference tuning
6	RW	0x0	force_vbus_valid force output vbus_valid asserted, active high
5	RW	0x0	force_session_end_val force output session_end asserted, active high
4	RW	0x0	force_b_session_val force output B_sessionvalid asserted, active high

Bit	Attr	Reset Value	Description
3	RW	0x0	force_a_session_val force output A_sessionvalid asserted, active high
2	RW	0x1	turn_off_diff_receiver Turn off differential receiver in suspend mode to save power, active low.
1:0	RO	0x0	reserved

GRF_USBPHY1_CON7

Address: Operational Base + offset (0x02bc)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:11	RW	0xd	host_discon_con HOST disconnect detection trigger point configure, only used in HOST mode 0000: 575mV 0001: 600mV 1001:625mV 1101:650mV(default)
10:8	RO	0x0	reserved
7	RW	0x1	bypass_squelch_trigger bypass squelch trigger point auto configure in chirp modes , active high
6	RW	0x1	half_bit_pre_empha_en half bit pre-emphasize enable, active high. "1" represent half bit pre-emphasis , "0" for full bit
5:3	RO	0x0	reserved
2:0	RW	0x0	vbus_valid_con vbus_valid reference tuning

GRF_UOC_STATUS0
Address: Operational Base + offset (0x02c0)
SoC status register 0

Bit	Attr	Reset Value	Description
31:26	RW	0x00	usbhost0_stat_ehci_usbsts USB host0 ehci_usbsts bit status
25:15	RW	0x000	usbhost0_stat_ehci_xfer_cnt USB host0 ehci_xfer counter status
14	RW	0x0	usbhost0_stat_ehci_xfer_prdc USB host0 ehci_xfer_prdc bit status
13:10	RW	0x0	usbhost0_stat_ehci_lpsmc_state USB host0 ehci_lpsmc_state bit status
9	RW	0x0	usbhost0_stat_ehci_bufacc USB host0 ehci_bufacc bit status
8	RW	0x0	usbhost0_stat_ohci_globalsuspend USB host0 ohci_globalsuspend bit status
7	RW	0x0	Copy1 usbhost0_stat_dp_attached USB HOST0 dp_attached signal status
6	RW	0x0	usbhost0_stat_cp_detected USB HOST0 cp_detected signal status
5	RW	0x0	usbhost0_stat_dcp_attached USB HOST0 dcp_atteched signal status
4	RW	0x0	usbhost0_stat_ohci_bufacc USB HOST0 ohci_bufacc signal status
3	RW	0x0	usbhost0_stat_ohci_rmtwkp USB HOST0 ohci_rmtwkp signal status
2	RW	0x0	usbhost0_stat_ohci_drwe USB HOST0 ohci_drwe signal status
1	RW	0x0	usbhost0_stat_ohci_rwe USB HOST0 ohci_rwe signal status
0	RW	0x0	usbhost0_stat_ohci_ccs USB HOST0 ohci_ccs signal status

GRF_CHIP_TAG
Address: Operational Base + offset (0x0300)
chip tag register

Bit	Attr	Reset Value	Description
31:0	RO	0x0000293c	chip_tag

GRF_MMC_DET_CNT
Address: Operational Base + offset (0x0304)
mmc0 detect filter counter register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RO	0x0fdb9	mmc_det_value mmc0 detect filter counter initial value

GRF_EFUSE_PRG_EN
Address: Operational Base + offset (0x037c)

efuse program register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RO	0x0	efuse_prg_en 0: efuse program disable 1: efuse program enable
12:0	RO	0x0	reserved