RK2738

Brief Datasheet

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Chapter 1 Introduction

1.1 Overview

RK2738 is a highly-integrated, high-performance, low-power digital multimedia processor which is based on Dual Core (DSP+CPU) architecture with hardware accelerator. It is designed for mid-end multimedia product applications such as PMP, ebook and Mobile TV etc.

RK2738 can support decode and encode for various types of video standards such as H.264/RMVB/MPEG-4/AVS/VC1/MPEG-2 by software and dedicated coprocessors. Specially, highest performace for video decode will reach fluent replay for video with RMVB @ 1280x720 formats. By providing a complete set of peripheral interface, RK2738 can support very flexible applications, including SDRAM, Nor Flash, Nand Flash, LCDC, Sensor, USB OTG 2.0, SD/MMC, eMMC, High-speed ADC interface, I2C, I2S, UART, SPI, and PWM etc.

This document will provide guideline on how to use RK2738 correctly and efficiently.

1.2 Features

- **System Operation**
  - Dual Core Architecture (ARM9 + DSP) , including hardware accelerator
  - Support system boot sequentially from ARM to DSP
  - Support address remap function
  - For two cores, all modules have unified address space
  - Selectable JTAG debug method
    - ARM9 debug only (default)
    - DSP debug only
    - ARM9+DSP dual core debug
  - Selectable CPU booting method
    - Boot from Nand Flash
    - Boot from SPI nor flash
    - Boot from UART device
    - Boot from eMMc

- **Memory Organization**
  - Internal memory space for ARM processor
    - Internal 16KB SRAM for ARM9 ICache
    - Internal 16KB SRAM for ARM9 DCache
    - Internal 2KB SRAM for ARM9 ITCM
  - Internal memory space for DSP processor
    - Internal 64KB SRAM for DSP Instruction L1 Memory (Also config as 32KB Memory+32KB ICache by software)
    - Internal 64KB SRAM for DSP Data L1 Memory
    - Internal 40KB SRAM for DSP Instruction L2 Memory
    - Internal 32KB SRAM for DSP Data L2 Memory
  - Embedded 8KB ROM for CPU Boot
  - Embedded 2KB SRAM for communication between two cores

- **Processors**
  - ARM926EJC
    - RISC architecture with 32bit ARM and 16bit Thumb instruction sets
    - Include efficient execution of Java byte codes
    - Built-in MMU to provide flexible memory management needed by many mainstream OS
    - Harvard cached architecture , separate ICache and DCache
    - Separate instruction and data TCM interfaces
    - Separate instruction and data AHB bus interface

        - Support ARM debug architecture
    - DSP
        - Based on VLIW instructions with SIMD concepts , reach high level of parallelism and high code density
        - Support 16bits and 32bits variable instruction sets
        - Based on a load/store architecture, have two load-store units
        - Support Nine-stage pipeline
        - Built-in two 16x16bit MAC units

- **Communication between two cores**
    - Support share memory and interactive interrupt method to complete communication
    - Processor Interface Unit (PIU)
        - Built-in three Command/reply protocols registers and three Semaphore registers to accessed by two cores
        - Support three semaphore-related interrupts and one command-reply-related interrupt between two cores

- **Clock & Power Management**
    - Three on-chip PLLs for ARM9 subsystem, DSP subsystem and Other logic
    - Support different DSP Core and internal AHB Bus clock ratio :
      1:1, 1:2, 1:3, 1:4, up to 1:16 mode
    - Support different DSP internal AHB Bus and internal APB Bus clock ratio :
      1:1, 1:2, 1:3, 1:4, up to 1:16 mode
    - Support different ARM9 core and AHB Bus clock ratio :
      1:1, 1:2, 1:3 and 1:4 mode
    - Support different ARM AHB Bus and ARM APB Bus clock ratio :
      1:1, 1:2 and 1:4 modes
    - 6 types of work modes by clock gating to save power :
        - Normal mode : Normal operating mode
        - Slow mode : Low frequency clock (24MHz) without PLL
        - Deep Slow mode : More Low frequency clock (32.768KHz) without PLL
        - Idle mode : The clock for only CPU is stopped ,
          Wake up by any interrupts to CPU from idle mode
        - Sleep mode : The clock for only DSP is stopped ,
          Wake up from sleep mode by some interrupts to DSP or register set from CPU
        - Stop mode : All clocks will be stopped , and SDRAM into Self-refresh, all PLLs into power-down mode ,
          Wake up from stop mode by external pin or RTC Alarm interrupt

- **Video hardware accellerator**
    - Deblocking
        - Support RMVB video format, max size is 1080p
        - Support embedded DMA function with on-the-fly mode

- **External Memory Interface**
    - Support SDRAM
    - Support Nor Flash/Nand Flash/SD/MMC/eMMC interface
    - Static/SDRAM Memory controller
        - Dynamic memory interface support , including SDR-SDRAM
        - Asynchronous static memory device support including SRAM, ROM and Nor Flash with or without asynchronous page mode
        - Support 2 chip selects forSDRAM and 2 chip selects for static memory
        - Support 16bits or 32bits width data bus SDRAM and 8/16 bits data bus static memory, it is programmable.

        - ◆ Support industrial standard SDRAM with a maximum of 256MB of address space per chip select
        - ◆ 4Mbytes access space per static memory support
        - ◆ Support SDRAM and Static Memory power-down mode
        - ◆ Support SDRAM self-refresh mode
        - ◆ Programmable arbitration priority for 6 slave data ports
    - ■ Nand Flash controller
        - ◆ Standard AMBA2.0 Slave interface
        - ◆ Support 8 chip selects for nand flash
        - ◆ Only support 8bit data width
        - ◆ Flexible CPU interface support
        - ◆ Embedded 2x1KB size buffer for DMA mode to improve performace
        - ◆ 512B、2KB、4KB page size support
        - ◆ Support hardware 24bit ECC
        - ◆ Support LBA nand
        - ◆ Support FF code auto correct process
        - ◆ Support randomizer
    - ■ SD/MMC controller
        - ◆ Two Embedded SD/MMC/eMMC Controllers, one support SD/MMC, another support eMMC. Compliant with SD Memor with 1bit and 4bit data bus
        - ◆ Compliant with MMC V3.3 and V4.0 with 1/4/8bit data bus
        - ◆ Support combined single 32x32bits FIFO for both transmit and receive operations
        - ◆ Support FIFO over-run and under-run prevention by stopping card clock
        - ◆ Variable SD/MMC card clock rate 0 – 52 MHz which depends on AHB clock frequency
        - ◆ Controllable SD/MMC card clock to save power consumption
        - ◆ Support card detection and initialization , and write protection
        - ◆ Support transfer block size of 1 to 65365Bytes
        - ◆ DMA based or Interrupt based operation

- ● **VIDEO/Image interface**
    - ■ Sensor controller
        - ◆ Embedded DMA function
        - ◆ Support 24MHz 、48MHz、27MHz clock input
        - ◆ Support CCIR656 PAL/NTSC input
        - ◆ Support YUYV and UYVY format input
        - ◆ Support YUV 4:2:2 and YUV 4:2:0 format output
        - ◆ Programmable Hsync and Vsync porality
        - ◆ Support sensor bypass to LCDC interface
        - ◆ Support 5 MegaPixels
    - ■ LCD controller
        - ◆ Standard AMBA2.0 master and slave interface
        - ◆ Programmable transfer mode to meet different bus bandwidth
And transfer efficiency
        - ◆ Parallel RGB LCD Interface: 24-bit(RGB888), 18-bit(RGB666), 15-bit(RGB565)
        - ◆ Serial RGB LCD Interface: 3x8-bit(RGB delta support), 3x8-bit + dummy, 16-bit + 8-bit
        - ◆ MCU LCD interface: i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
          TV Interface: ITU-R 656
          TV encode: CVBS
        - ◆ One Background layer: programmable 24-bit color
        - ◆ One GUI layer(win1):
          1. RGB888, ARGB888, RGB565
          2. Maximum resolution is 1024x768
          3. Partial display

            4. 1/4 to 4 scaling-down and scaling-up engine
            5. 8-bit alpha blending
            6. Transparency color key
        - One Video layer(win0):
            1. RGB888, ARGB888, RGB565, YCbCr422, YCbCr420-0, YCbCr420-1, YCbCr420-M, YCbCr444
            2. Maximum resolution is 1280x720
            3. Partial display(roller support)
            4. 1/8 to 8 scaling-down and scaling-up engine
            5. 8-bit alpha blending(no scaling in ARGB mode)
            6. Transparency color key
            7. Deflicker support for interlace output
        - Hardware cursor(HWC):
            1. 32x32 resolutions.
            2. 3x24-bit color LUT for 2-bit palette
            3. 4-bit alpha blending
        - Support Virtual Display
        - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709) and RGB2YCbCr modules
        - Support MCU PANNEL Bypass Mode and SCALE Mode
        - Compatible with RGB Delta/no-Delta Pannel
        - Compatible with RGB Series/Parallel Output
        - Support Interlace and Progressive Output
        - Replication(16-bit to 24-bit) and Dithering(24-bit to 16-bit/18-bit)
        - Standby mode
        - Blank and black display
        - Support LCDC interface bypass from Host interface or VIP interface
    - Ebook Controller
        - system interface
        - AHB slave for register configuration
        - AHB master for frame data transfer（DMA）
        - Interrupt output
        - EPD interface
        - E-ink/AUO EPD compatible
        - Up to 2048x2048 resolution
        - Up to 16 level gray scale
        - LUT updateable
        - Direct mode and LUT mode
        - All-update mode and Diff-update mode
        - Single phase and multi-phase mode
        - Support window display
        - Source driver interface
        - Gate driver interface

- **DMA Controller**
    - Two DMA Controllers in chip
    - DW_DMA Controller integrated inside ARM9 subsystem
        - Three DMA Channels support to use by audio and sd/mmc and system data transfer
        - hardware request handshaking support
        - Support hardware and software trigger DMA transfer mode
        - Build-in 3 data FIFO : 32Bytes/32Bytes/16Bytes
        - Channel 0 support Scatter/Gather transfer support
        - LLP transfer support
        - Two masters for on-the-fly support
        - The master interface only support undefined length INCR transfer
    - 3D-DMA Controller(XDMA) integrated inside DSP subsystem
        - This DMA focus on data transfer for video process and mobile TV application

        - 16 configurable DMA channels , 4 channels support 3-dimensional data transfer
        - 8/16/32/64bit data transfer support and configurable burst length (INCR/INCR4/INCR8)
        - Programmable source and destination addresses with a post-modification option
        - Configurable external channel triggering (edge or level)
        - Support chaining-channels ,linked list-transfer and auto-channel initialization operating mode
        - Pause and resume operations supported to save power
        - Eight-stage memory buffer FIFO

- **Interrupt Controller**
    - Two Interrupt Controller in chip
    - DW_INTC integrated inside ARM9 subsystem
        - Support 48 IRQ normal interrupt sources and 2 FIQ fast interrupt sources
        - Vectored interrupts support
        - Software interrupts support
        - Programmable interrupt priorities
        - Fixed High Level sensitive triggered interrupts
    - ICU (Interrupt Control unit) integrated inside DSP subsystem
        - 48 interrupt sources , each may be linked to different interrupt inputs for DSP core
        - Software triggering to all 48 interrupt sources
        - Configurable source interrupt polarity (low/high)
        - External interrupt source with software configuration to edge/level sensitive

- **USB interface**
    - USB OTG 2.0 interface
        - Complies with the OTG Supplement to the USB2.0 Specification
        - Operates in High-Speed and Full-Speed mode
        - Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
        - Support 6 channels in host mode
        - 6 endpoints , 3 in and 3 out
        - Built-in one 448 x 35bits FIFO

- **High-speed ADC interface**
    - Max frequency is 64MHz
    - Standard AMBA2.0 Slave interface
    - Dual 8/10 bits A/D converter Interface
    - Support 2bit data bus from GPS tunner
    - Support TS stream data transfer

- **Low_speed Peripheral interface**
    - Serial Peripheral Interface (SPI) Master Controller
        - Support two slave devices connection
        - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National Semiconductor Microwire interface
        - Dynamic control of serial bit rate of data transfer by programmable sclk_out frequency, which is half of SPICLK in max mode
        - FIFO depth for transmit and receive are also 32x16bits
        - Programmable data item size ,from 4 to 16bits
        - Support DMA based and interrupt based operation
    - Serial Peripheral Interface (SPI) Slave & Master Controller
        - Support two slave devices connection
        - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National

  Semiconductor Microwire interface
  - Dynamic control of serial bit rate of data transfer by programmable sclk_out frequency, which max frequency is half of SPICLK in master mode.
  - Dynamic control of serial bit rate of data transfer by sclk_in from master device.
  - FIFO depth for transmit and receive are also 32x16bits
  - Programmable data item size ,from 4 to 16bits
  - Support DMA based and interrupt based operation
- UART
  - 2 UART support in chip
  - UART0 support modem function and auto flow-control function
  - UART1 support IrDA 1.0 SIR mode and Serial data transfer without auto flow-control function
  - Based on the 16550 industry standard
  - Programmable serial data baud rate, up to 3Mbps baud-rate , and main clock is 48MHz in max mode
  - Programmable baud rate generator. This enables division of the internal clock by (1 ~ 65535 x 16) and generates an internal x16 clock
  - Standard asynchronous communication bits (start, stop and parity).
  - DMA based and interrupt based operation
  - FIFO depth for data transfer is always 32x8bits
  - For UART1, In IrDA SIR mode, support configurable baud data rate up to 115.2K and a pulse duration as specified in the IrDA physical layer specification
- I2C controller
  - Multi masters operation support
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support mono/stereo audio file
  - Support audio resolution: 8, 16 bits
  - Support audio sample rate from 32KHz to 96 KHz
  - Support I2S, Left-Justified and Right-Justified digital serial data format
- PWM
  - Built-in three 32 bit timer modulers
  - Programmable counter
  - Chained timer for long period purpose
  - 4-channel 32-bit timer with Pulse Width Modulation (PWM)
  - Programmable duty-cycle, and frequency output
- General Purpose IO (GPIO)
  - Support 96 individually programmable input/output pins
  - 16 GPIOs with external interrupt capability
- Timers in CPU system
  - Built-in Three 32 bits timer modules
  - Support for two operation modes : free-running and user-defined count
- Timers in DSP system
  - Built-in two 32 bits timer modules
  - Support for 5 various counting modes : Single Count mode, Auto-restart mode , Free-running , Event Count mode and Watchdog Timer mode
  - Pulse Width Modulation(PWM) mechanism
  - Three possible input clock signals: internal , external and cascaded
- Watchdog Timer (WDT)
  - Watchdog function (Generate a system reset or an interrupt)
  - Built-in 32 bits programmable counter
  - System power off sequence with output control pin

- **Analog IP interface**
  - ADC Converter
    - 4-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
      (one channel for 1.2v)
    - Supply 2.5V to 3.6V for analog and 0.9V to 1.3V for digital interface
    - Very Low Power : <0.4mW power consumption at 1MSPS
  - Audio CODEC
    - Complete Stero/Mon Microphone interface
    - ADC SNR 95dB('A' Weighted), THD -85dB at 48kHz, 3.3V
    - DAC and On-chip Headphone Driver
      1. >10mW output power on 32Ω/3.3V
      2. THD+N at 10mW, SNR>90dB with 32Ω load
      3. No DC blocking capacitors required(capless mode)
    - Seperately mixed mono output
    - Low power consumption
      1. 40mW stero playback static power(3.3V/1.5 supplies)
      2. 20mW record& playback (1.8V/1.5 supplies)
    - Low power supply, Analogue: 1.8V to 3.6V
    - 256 x Fs/384 x Fs Master clock rates, up to 24Mz
    - Audio sample rates: 8 to 96kS/s
    - Soft mute function at DAC path
    - Less than -80dBc out-of-band Noise

- **Max Frequency**

ARM Core:	TBD
DSP Core:	TBD
SDRAM(AHB):	150M
APB:	100M

- **Package Type**

RK2738:	LQFP176

1.3 Block Diagram

The following figure shows block diagram of RK2738.
RK2738 can be divided into two sub system: DSP System and CPU System.

- DSP System
  - XDMA : three-dimensional DMA , used to data transfer for video decoder or other algorithm
  - ICU : Interrupt controller for DSP processor
  - PIU : processor interface unit, used to complete communication between DSP and CPU
  - PMU ： power management unit, used to control clock and reset to save power for modules inside DSP system
  - General reg file : focus on general control on DSP system by software method, composed of some register groups
- CPU System
  - DW_DMA : used to data transfer for audio and low-speed peripheral
  - SCU : focus on clock gating , clock frequency switch, reset control , power on/off and system mode switch for CPU system to save power
  - INTC : Interrupt controller for CPU processor
  - General reg file: focus on general control on CPU system by software method, composed of some register groups, including IO mux control, IO PAD pull up/down control and other system control signals.
  - High-Speed ADC Interface: focus on completing data reveiver from tuner in DVB-T, DAB, T-DMB, GPS application with software method.

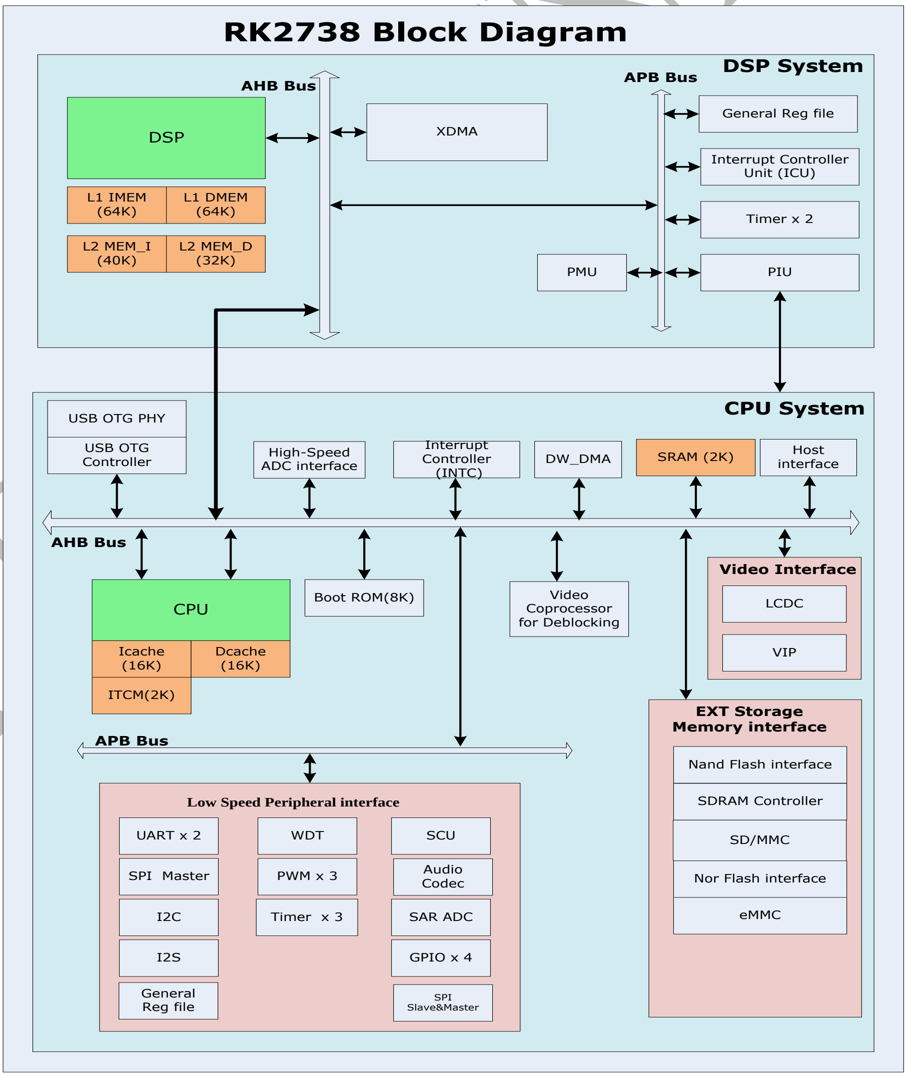


Fig. 1-1 RK2738 Block Diagram

1.4 Pin Description

The following table shows all of the pins for RK2738. According to differenct application, part of pins will be bonded out, or double/triple bonded.

The first column in the pin function description is default function after power on reset, and function in the last two columns will be implemented by software set.
The detailed register descriptions are IOMUX_A_CON and IOMUX_B_CON IOMUX_C_CON IOMUX_D_CON IOMUX_E_CON in chapter 32.

As for GPIOm_n[i] (m = 0, 1; n = A~D; i = 0~7), we can control Pull up (or Pull Down diceded by PAD type) or no resistor for them by software set. The value for Pull up/down type in the following table is default after power on reset. The detailed register descriptions are in chapter 32.

***Notes*:**

Pull Down:	**IO PULL Down**
PullUp:	**IO Pull Up**
I:	**Input IO**
O:	**Output IO**
B:	**Bi-directional IO**
A:	**Analog IO**

1.4.1 RK2738 LQFP176 Pin Description

Pin No	Pin name	Pin Function	Pin Direction	Pin Description
LEFT				
1	GPIO0_D[4]/UART0_SIN	GPIO0_D[4]	B Pull Up	gpio
		UART0_SIN	I	uart0 serial data in
2	GPIO2_B[4]/HSADC_ID4	GPIO2_B[4]	B Pull Down	gpio
		HSADC_DATA_I[4]	I	hsadc data bit4 for I path
3	GPIO2_B[5]/HSADC_ID5	GPIO2_B[5]	B Pull Down	gpio
		HSADC_DATA_I[5]	I	hsadc data bit5 for I path
4	LCDC_HSYNC	LCDC_HSYNC/RK_TCON_SDLE	O	lcdc horizontal sync signal
5	GPIO0_D[0]/LCDC_VSYNC	GPIO0_D[0]	B Pull Down	gpio
		LCDC_VSYNC/RK_TCON_SDOE	O	lcdc vertical sync signal
6	GPIO0_D[1]/LCDC_DEN	GPIO0_D[1]	B Pull Down	gpio
		LCDC_DENABLE/RK_TCON_GDCLK	O	lcdc data valid signal
7	GPIO2_B[6]/HSADC_ID6	GPIO2_B[6]	B Pull Down	gpio
		HSADC_DATA_I[6]	I	hsadc data bit6 for I path
8	GPIO2_B[7]/HSADC_ID7	GPIO2_B[7]	B Pull Down	gpio
		HSADC_DATA_I[7]	I	hsadc data bit7 for I path
9	VDDIO	VDDIO	P	IO power supply (3.3V)
10	LCDC_DATA[4]	LCDC_DATA4/RK_TCON_SDDO[4]	O	lcd data[4]
11	LCDC_DATA[5]	LCDC_DATA5/RK_TCON_SDDO[5]	O	lcd data[5]
12	LCDC_DATA[6]	LCDC_DATA6/RK_TCON_SDDO[6]	O	lcd data[6]
13	LCDC_DATA[7]	LCDC_DATA7/RK_TCON_SDDO[7]	O	lcd data[7]
14	GPIO2_A[1]/GPS_CLKI/HSADC_CLKO	GPIO2_A[1]	B Pull Down	gpio
		GPS CLK/HSADC_CLKIN	I	clock input for gps application
		HSADC_CLKOUT	O	clock out to hsadc analog
15	GPIO2_A[2]/HSADC_ID8/TS_VALID	GPIO2_A[2]	B Pull Down	gpio
		HSADC_DATA_I[8]	I	hsadc data bit8 for I Path
		TS_VALID	I	ts stream valid signal
16	GPIO1_B[0]/LCDC_D8	GPIO1_B[0]	B Pull down	gpio
		LCDC_DATA8/RK_TCON_SDCE[0]	O	lcdc data bit8
17	GPIO1_B[1]/LCDC_D9	GPIO1_B[2]	B Pull down	gpio
		LCDC_DATA9/RK_TCON_SDCE[1]	O	lcdc data bit9
18	GPIO1_B[2]/LCDC_D10	GPIO0_B[2]	B Pull down	gpio

		LCDC_DATA10/RK_TCON_SDCE[2]	O	lcdc data bit10
19	VSS	VSS	G	ground of IO and Core
20	LCDC_DCLK	LCDC_DCLK/RK_TCON_SDCLK	O	lcdc data clock
21	GPIO1_B[3]/LCDC_D11	GPIO1_B[3]	B Pull down	gpio
		LCDC_DATA11/RK_TCON_BORDER[0]	O	lcdc data bit11
22	GPIO1_B[4]/LCDC_D12	GPIO1_B[4]	B Pull down	gpio
		LCDC_DATA12/RK_TCON_BORDER[1]	O	lcdc data bit12
23	GPIO1_B[5]/LCDC_D13	GPIO1_B[5]	B Pull down	gpio
		LCDC_DATA13/RK_TCON_VOM	O	lcdc data bit13
24	GPIO1_B[6]/LCDC_D14	GPIO1_B[6]	B Pull down	gpio
		LCDC_DATA14/RK_TCON_SDSHR	O	lcdc data bit14
25	GPIO1_B[7]/LCDC_D15	GPIO1_B[7]	B Pull down	gpio
		LCDC_DATA15/RK_TCON_GDOE	O	lcdc data bit15
26	GPIO1_C[0]/LCDC_D16/UART1_SIN	GPIO1_C[0]	B Pull Up	gpio
		LCDC_DATA16//RK_TCON_GDSP	O	lcdc data bit16
		UART1_SIN	I	uart1 serial data in
27	GPIO1_C[1]/LCDC_D17/UART_SOUT	GPIO1_C[1]	B Pull Up	gpio
		LCDC_DATA17/RK_TCON_GDRL	O	lcdc data bit17
		UART1_SOUT	O	uart1 serial data out
28	GPIO1_C[2]/LCDC_D18	GPIO1_C[2]	B Pull Up	gpio
		LCDC_DATA18/RK_TCON_GDPWR[0]	O	lcdc data bit18
29	GPIO1_C[3]/LCDC_D19	GPIO1_C[3]	B Pull Up	gpio
		LCDC_DATA19/RK_TCON_GDPWR[1]	O	lcdc data bit19
30	VDDCORE	VDDCORE	P	Core power supply (1.2V)
31	GPIO1_C[4]/LCDC_D20	GPIO1_C[4]	B Pull Up	gpio
		LCDC_DATA20/RK_TCON_GDPWR[2]	O	lcdc data bit20
32	GPIO1_C[5]/LCDC_D21	GPIO1_C[5]	B Pull Up	gpio
		LCDC_DATA21/RK_TCON_SDCE[3]	O	lcdc data bit21
33	GPIO1_C[6]/LCDC_D22	GPIO1_C[6]	B Pull Up	gpio
		LCDC_DATA22/RK_TCON_SDCE[4]	O	lcdc data bit22
34	GPIO1_C[7]/LCDC_D23	GPIO1_C[7]	B Pull Up	gpio
		LCDC_DATA23/RK_TCON_SDCE[5]	O	lcdc data bit23
35	SDR_ADDR[11]	M_ADDR[11]	O	SDRAM/SRAM addr[11]
36	SDR_ADDR[12]	M_ADDR[12]	O	SDRAM/SRAM addr[12]
37	SDR_DATA[0]	M_DATA[0]	B	SDRAM/SRAM data[0]
38	SDR_DATA[1]	M_DATA[1]	B	SDRAM/SRAM data[1]
39	SDR_DATA[2]	M_DATA[2]	B	SDRAM/SRAM data[2]
40	SDR_DATA[3]	M_DATA[3]	B	SDRAM/SRAM data[3]
41	SDR_DATA[4]	M_DATA[4]	B	SDRAM/SRAM data[4]
42	SDR_DATA[5]	M_DATA[5]	B	SDRAM/SRAM data[5]
43	SDR_DATA[6]	M_DATA[6]	B	SDRAM/SRAM data[6]
44	SDR_DATA[7]	M_DATA[7]	B	SDRAM/SRAM data[7]
45	VSS	VSS	G	ground of IO and Core
Bottom				
46	SDR_PRECHARGE	M_PRECHARGE_BITS	O	SDRAM m_precharge_bits
47	SDR_ADDR[9]	M_ADDR[9]	O	SDRAM/SRAM addr[9]
48	SDR_ADDR[8]	M_ADDR[8]	O	SDRAM/SRAM addr[8]
49	SDR_ADDR[7]	M_ADDR[7]	O	SDRAM/SRAM addr[7]
50	SDR_ADDR[6]	M_ADDR[6]	O	SDRAM/SRAM addr[6]
51	SDR_ADDR[5]	M_ADDR[5]	O	SDRAM/SRAM addr[5]
52	JTAG_TCK	TCK	I Pull Up	JTAG TCK
53	JTAG_TRST_N	TRSTN	I Pull Down	JTAG TRST
54	JTAG_TDI	TDI	I Pull Up	JTAG TDI
55	JTAG_TMS	TMS	I Pull Up	JTAG TMS
56	JTAG_TDO	TDO	O	JTAG TDO
57	JTAG_RTCK	RTCK	O	JTAG RTCK

58	SDR_ADDR[4]	M_ADDR[4]	O	SDRAM/SRAM addr[4]
59	SDR_ADDR[3]	M_ADDR[3]	O	SDRAM/SRAM addr[3]
60	SDR_ADDR[2]	M_ADDR[2]	O	SDRAM/SRAM addr[2]
61	SDR_ADDR[1]	M_ADDR[1]	O	SDRAM/SRAM addr[1]
62	VDDIO	VDDIO	P	IO power supply (3.3V)
63	SDR_ADDR[0]	M_ADDR[0]	O	SDRAM/SRAM addr[0]
64	SDR_DATA[8]	M_DATA[8]	B	SDRAM/SRAM data[8]
65	SDR_DATA[9]	M_DATA[9]	B	SDRAM/SRAM data[9]
66	SDR_DATA[10]	M_DATA[10]	B	SDRAM/SRAM data[10]
67	SDRCLK_OUT	S_CLKOUT	O	SDRAM clkout
68	VDDCORE	VDDCORE	P	Core power supply (1.2V)
69	SDR_DATA[11]	M_DATA[11]	B	SDRAM/SRAM data[11]
70	SDR_DATA[12]	M_DATA[12]	B	SDRAM/SRAM data[12]
71	SDR_DATA[13]	M_DATA[13]	B	SDRAM/SRAM data[13]
72	SDR_DATA[14]	M_DATA[14]	B	SDRAM/SRAM data[14]
73	VSS	VSS	G	ground of IO and Core
74	SDR_DATA[15]	M_DATA[15]	B	SDRAM/SRAM data[15]
75	SDR_BA[0]	S_BANK_ADDR[0]	O	SDRAM ba[0]
76	SDR_BA[1]	S_BANK_ADDR[1]	O	SDRAM ba[1]
77	SDR_CASN	S_CAS_N	O	SDRAM casn
78	SDR_RASN	S_RAS_N	O	SDRAM rasn
79	SDR_WEN	SM_WE_N	O	SRAM wen
80	SDR_CS0N	S_CS0_N	O	SDRAM csn
81	SDR_CS1N	S_CS1_N	O	SDRAM csn
82	SDR_DQM[0]	S_DQM[0]	O	SDRAM dqm[0]
83	SDR_DQM[1]	S_DQM[1]	O	SDRAM dqm[1]
84	GPIO0_A[7]	GPIO0_A[7]	B Pull Up	gpio
		IO_SDR_CKE	O	SDRAM clock enable
85	GPIO1_D[2]/VIP_D2	GPIO1_D[2]	B Pull Down	gpio
		VIP_DATA2	I	vip data input2
86	GPIO1_D[3]/VIP_D3	GPIO1_D[3]	B Pull Down	gpio
		VIP_DATA3	I	vip data input3
87	GPIO1_D[4]/VIP_D4	GPIO1_D[4]	B Pull Down	gpio
		VIP_DATA4	I	vip data input4
88	GPIO1_D[5]/VIP_D5	GPIO1_D[5]	B Pull Down	gpio
		VIP_DATA5	I	vip data input5
RIGHT				
89	SARADC_REXT75K	SARADC_REXT75K	A	SAR ADC external resister
90	SARADC_AIN[2]	SARADC_AIN[2]	A	10bit adc channel2 input
91	SARADC_AIN[1]	SARADC_AIN[1]	A	10bit adc channel1 input
92	SARADC_AIN[0]	SARADC_AIN[0]	A	10bit adc channel0 input
93	VDDA_SARADC	VDDA_SARADC	P	10BIT ADC ANALOG POWER AND REFERENCE VOLTAGE (3.3V)
94	VDDA_ARMPLL	VDDA_ARMPLL	P	ARM PLL ANALOG POWER(1.2V)
95	VSSA_ARMPLL	VSSA_ARMPLL	G	ARM PLL ANALOG GROUND(0V)
96	VBUS	VBUS	P	USB DEDECT INPUT OR 5V POWER SUPPLY FOR OTG FUNCTION
97	USB_VDD33	USB_VDD33	P	USB ANALOG POWER SUPPLY (3.3V)
98	DP	DP	A	USB D+ SIGNAL
99	DM	DM	A	USB D- SIGNAL
100	USB_VSSA	USB_VSSA	G	USB ANALOG GROUND (0V)
101	RKELVIN	RKELVIN	A	TRANSMITTER RESISTOR TUNE PIN
102	VDDIO	VDDIO	P	IO power supply (3.3V)
103	USB_VDD33	USB_VDD33	P	USB ANALOG POWER SUPPLY (3.3V)
104	EXTCLK	EXTCLK	I Pull Down	EXT CLOCK INPUT
105	XOUT24M	XOUT24M	O OSC	CRYSTAL 24MHZ OUTPUT PIN

106	XIN24M	XIN24M	I OSC	CRYSTAL 24MHZ INPUT PIN
107	VDDCORE	VDDCORE	P	Core power supply (1.2V)
108	GPIO1_D[6]/VIP_D6	GPIO1_D[6]	B Pull Down	gpio
		VIP_DATA6	I	vip data input6
109	GPIO2_C[0]/VIP_D7	GPIO2_C[0]	B Pull Down	gpio
		VIP_DATA7	I	vip data input7
110	GPIO2_C[1]/VIP_D8	GPIO2_C[1]	B Pull Down	gpio
		VIP_DATA8	I	vip data input8
111	GPIO2_C[2]/VIP_D9	GPIO2_C[2]	B Pull Down	gpio
		VIP_DATA9	I	vip data input9
112	GPIO2_C[3]/VIP_D10	GPIO2_C[3]	B Pull Down	gpio
		VIP_DATA10	I	vip data input10
113	GPIO2_C[4]/VIP_D11	GPIO2_C[4]	B Pull Down	gpio
		VIP_DATA11	I	vip data input11
114	FLASH_DATA[0]	FLASH_DATA0	B Pull Up	nand flash data[0]
		SDMMC1_DATA[0]	B	SDMMC1 data bit0
115	FLASH_DATA[1]	FLASH_DATA1	B Pull Up	nand flash data[1]
		SDMMC1_DATA[1]	B	SDMMC1 data bit1
116	FLASH_DATA[2]	FLASH_DATA2	B Pull Up	nand flash data[2]
		SDMMC1_DATA[2]	B	SDMMC1 data bit2
117	FLASH_DATA[3]	FLASH_DATA3	B Pull Up	nand flash data[3]
		SDMMC1_DATA[3]	B	SDMMC1 data bit3
118	VSS	VSS	G	ground of IO and Core
119	FLASH_DATA[4]	FLASH_DATA4	B Pull Up	nand flash data[4]
		SDMMC1_DATA[4]	B	SDMMC1 data bit4
120	FLASH_DATA[5]	FLASH_DATA5	B Pull Up	nand flash data[5]
		SDMMC1_DATA[5]	B	SDMMC1 data bit5
121	FLASH_DATA[6]	FLASH_DATA6	B Pull Up	nand flash data[6]
		SDMMC1_DATA[6]	B	SDMMC1 data bit6
122	FLASH_DATA[7]	FLASH_DATA7	B Pull Up	nand flash data[7]
		SDMMC1_DATA[7]	B	SDMMC1 data bit7
123	VDDIO	VDDIO	P	IO power supply (3.3V)
124	FLASH_ALE	FLASH_ALE	O	nand flash ale
125	FLASH_CLE	FLASH_CLE	O	nand flash cle
126	FLASH_RDN	FLASH_RDN	O	nand flash rdn
		SDMMC1_POWER_EN	O	sdmmc1 power en
127	GPIO2_C[7]/VIP_CLKI	GPIO2_C[7]	B Pull Down	gpio
		VIP_CLKIN	I	vip clock input from sensor
128	GPIO1_D[7]/VIP_CLKO	GPIO1_D[7]	B Pull Down	gpio
		VIP_CLKOUT	O	sensor clk out
129	GPIO2_C[5]/VIP_VSYNC	GPIO2_C[5]	B Pull Down	gpio
		VIP_VSYNC	I	vip vertical sync signal
130	GPIO2_C[6]/VIP_HREF	GPIO2_C[6]	B Pull Down	gpio
		VIP_HREF	I	vip horizontal sync signal
TOP				
131	CODEC_AIL	AIL	A	Left line input.
132	CODEC_AIR	AIR	A	Right line input.
133	CODEC_MIC_IN	MIC_IN	A	Micphone input.
134	CODEC_VMID	VMID	A	VMID reference decoupling node (value=vdd/2)
135	CODEC_VDDA_REF	VDD_REF	A	DAC reference decoupling node(value=vdd)
136	CODEC_VSSA	VSSA	G	The power ground for the CODEC analog part.
137	CODEC_AOR	AOR	A	Right Earphone amplifier output
138	CODEC_AOM	AOM	A	MONO Earphone amplifier output
139	CODEC_AOL	AOL	A	Left Earphone amplifier output

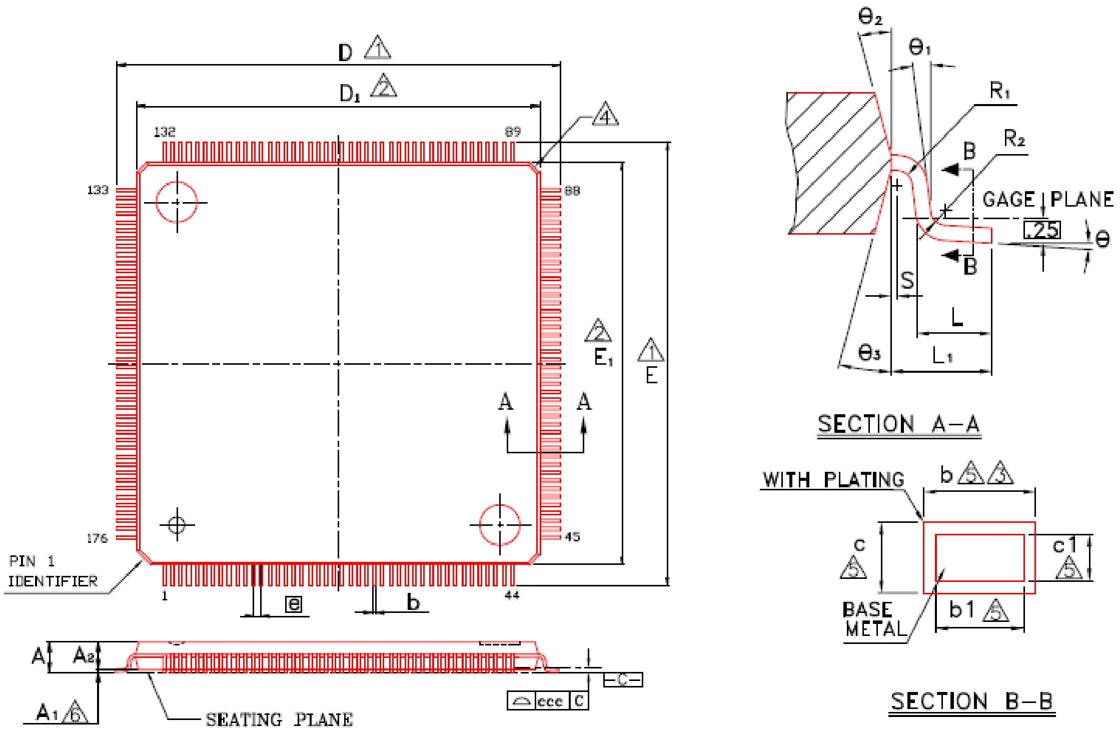
140	GPIO2_D[0]/HOST_D8	GPIO2_D[0]	B Pull Down	gpio
		HOST_DATA8	B	host_data[8]
141	GPIO0_A[2]/I2S_SDI	GPIO0_A[2]	B Pull Down	gpio
		I2S_SDI	I	i2s sdi from codec
142	GPIO0_A[5]/I2S_SCLK	GPIO0_A[5]	B Pull Up	gpio
		I2S_SCLK	B	i2s serial clock
143	GPIO0_A[4]/I2S_LRCK	GPIO0_A[4]	B Pull Up	gpio
		I2S_LRCK	B	i2s lrck
144	GPIO0_A[3]/I2S_SDO	GPIO0_A[3]	B Pull Down	gpio
		I2S_SDO	O	i2s sdo to codec
145	GPIO0_A[6]/I2S_CLK	GPIO0_A[6]	B Pull Up	gpio
		I2S_CLK	O	i2s clock out to codec
146	GPIO1_A[4]/SPI1_CS0	GPIO1_A[4]	B Pull Up	gpio
		SPI1_CS0	O	SPI1 chip select0 output
147	GPIO1_A[3]/SPI1_TXD	GPIO1_A[3]	B Pull Up	gpio
		SPI1_TXD	O	spi1 txd
148	GPIO1_A[2]/SPI1_RXD	GPIO1_A[2]	B Pull Up	gpio
		SPI1_RXD	I	spi1 rxd
149	GPIO1_A[0]/SPI1_CLKI/SPI1_CLKO	GPIO1_A[0]	B Pull Up	gpio
		SPI1_CLKIN/SPI1_CLKOUT	B	spi1 slave/master mode clock signal
150	FLASH_RDY	FLASH_RDY	I Pull Up	nand flash ready/busy
		SDMMC1_DETECT_N	I	SDMMC1_detect_n
151	FLASH_WRN	FLASH_WRN	O	nand flash wrn
		SDMMC1_CMD	I Pull Up	SD MMC command signal
152	FLASH0_CSN	FLASH_CS0	O	nand flash cs0
		SDMMC1_CLKOUT	O	SDMMC clock output signal
153	VDDCORE	VDDCORE	P	Core power supply (1.2V)
154	GPIO0_C[0]/SDMMC0_D4/PWM0	GPIO0_C[0]	B Pull Up	gpio
		SDMMC0_DATA[4]	B	sdmmc0 data bit4
		PWM0	B	pwm
155	GPIO0_B[6]/SDMMC0_DET/SPI0_CSN1	GPIO0_B[6]	B Pull UP	gpio
		SDMMC0_DETECT_N	I	sdmmc0 detect signal
		SPI0_CSN1	O	spi0 second chip select
156	FLASH1_CSN	FLASH_CS1	O	nand flash cs1
157	GPIO0_C[4]/I2C0_SDA/FLASH_CS2	GPIO0_C[4]	B Pull Up	gpio
		I2C0_SDA	B	i2c0 sda
		FLASH_CS2	O	nand flash cs2
158	GPIO0_C[5]/I2C0_SCL/FLASH_CS3	GPIO0_C[5]	B Pull Up	gpio
		I2C0_SCL	B	i2c0 scl
		FLASH_CS3	O	nand flash cs3
159	GPIO0_B[5]/SDMMC0_CLKO/SPI0_CLKO	GPIO0_B[5]	B Pull UP	gpio
		SDMMC0_CLKOUT	O	sdmmc0 clock out
		SPI0_CLKO	O	spi0 clk out
160	VSS	VSS	G	ground of IO and Core
161	GPIO0_B[1]/SDMMC0_D0/SPI0_RXD	GPIO0_B[1]	B Pull UP	gpio
		SDMMC0_DATA[0]	B	sdmmc0 data bit0
		SPI0_RXD	I	spi0 rxd
162	GPIO0_B[0]/SDMMC0_CMD/SPI0_TXS	GPIO0_B[0]	B Pull UP	gpio
		SDMMC0_CMD	B	sdmmc0 command
		SPI0_TXS	O	spi0 txd
163	GPIO0_B[4]/SDMMC0_D3	GPIO0_B[4]	B Pull UP	gpio
		SDMMC0_DATA[3]	B	sdmmc0 data bit3
164	GPIO0_B[3]/SDMMC0_D2	GPIO0_B[3]	B Pull UP	gpio
		SDMMC0_DATA[2]	B	sdmmc0 data bit2
165	GPIO0_B[2]/SDMMC0_D1	GPIO0_B[2]	B Pull UP	gpio
		SDMMC0_DATA[1]	B	sdmmc0 data bit1

166	LCDC_DATA[0]	LCDC_DATA0/RK_TCON_SDDO[0]	O	lcd data[0]
167	LCDC_DATA[1]	LCDC_DATA1/RK_TCON_SDDO[1]	O	lcd data[1]
168	LCDC_DATA[2]	LCDC_DATA2/RK_TCON_SDDO[2]	O	lcd data[2]
169	LCDC_DATA[3]	LCDC_DATA3/RK_TCON_SDDO[3]	O	lcd data[3]
170	VDDIO	VDDIO	P	IO power supply (3.3V)
171	GPIO0_D[5]/UART0_SOUT	GPIO0_D[5]	B Pull Up	gpio
		UART0_SOUT	O	uart0 serial data out
172	NPOR	NPOR	I Pull Up	Power on Reset
173	GPIO2_B[3]/HSADC_ID3	GPIO2_B[3]	B Pull Down	gpio
		HSADC_DATA_I[3]	I	hsadc data bit3 for I path
174	GPIO2_B[2]/HSADC_ID2	GPIO2_B[2]	B Pull Down	gpio
		HSADC_DATA_I[2]	I	hsadc data bit2 for I path
175	GPIO2_B[1]/HSADC_ID1	GPIO2_B[1]	B Pull Down	gpio
		HSADC_DATA_I[1]	I	hsadc data bit1 for I path
176	GPIO2_B[0]/HSADC_ID0	GPIO2_B[0]	B Pull Down	gpio
		HSADC_DATA_I[0]	I	hsadc data bit0 for I path

Note: Only GPIO0_A, GPIO1_A, GPIO2_A can used as interrupt ports.

1.5 Package outline

1.5.1 LQFP176 package outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Chapter 2 Port Multiplexer

2.1 Overview

Most of IOs have the multiple functions shared by programmable register set. And can also be pulled-up or pulled-down by reconfigurable register. As for the detailed description for these registers, please refer to register IOMUX_A_CON / IOMUX_B_CON / IOMUX_C_CON / IOMUX_D_CON/ IOMUX_E_CON / GPIO0_AB_PU_CON / GPIO0_CD_PU_CON / GPIO1_AB_PU_CON / GPIO1_CD_PU_CON in Chapter 32.

In hardware schematic, these GPIO ports also can be marks as following name:

GPIO0_A:	GPIO_A
GPIO0_B:	GPIO_B
GPIO0_C:	GPIO_C
GPIO0_D:	GPIO_D
GPIO1_A:	GPIO_E
GPIO1_B:	GPIO_F
GPIO1_C:	GPIO_G
GPIO1_D:	GPIO_H
GPIO2_A:	GPIO_I
GPIO2_B:	GPIO_J
GPIO2_C:	GPIO_K
GPIO2_D:	GPIO_L

2.2 Detailed description for IO MUX

The following table shows the detailed multiplexer for all GPIOs.

Table 2-1 RK2738 IO MUX List

PAD NAME	PORT Name	PAD Direction	Pin Description
GPIO0_A			
IO_GPIO0_A[0]	GPIO0_A[0]	B Pull Down	
	host_data16	I	host data 16
	testmode0	I	testmode0
IO_GPIO0_A[1]	GPIO0_A[1]	B Pull Down	gpio
	host_data17	I	host data 17
	testmode1	I	testmode1
IO_GPIO0_A[2]	GPIO0_A[2]	B Pull Down	gpio
	I2S_SDI	I	i2s sdi from codec
	testmode2	I	testmode2
IO_GPIO0_A[3]	GPIO0_A[3]	B Pull Down	gpio
	I2S_SDO	O	i2s sdo to codec
	testmode3	I	testmode3
IO_GPIO0_A[4]	GPIO0_A[4]	B Pull Up	gpio
	I2S_LRCK	B	i2s lrck
	scan_en	I	scan_en
IO_GPIO0_A[5]	GPIO0_A[5]	B Pull Up	gpio
	I2S_SCLK	B	i2s serial clock
IO_GPIO0_A[6]	GPIO0_A[6]	B Pull Up	gpio
	I2S_CLK	O	i2s clock out to codec
IO_GPIO0_A[7]	GPIO0_A[7]	B Pull Up	gpio

	IO_SDR_CKE	O	SDRAM clock enable
GPIO0_B			
IO_GPIO0_B[0]	GPIO0_B[0]	B Pull UP	gpio
	sdmmc0_cmd	B	sdmmc0 command
	SPI0_TXS	O	spi0 txd
IO_GPIO0_B[1]	GPIO0_B[1]	B Pull UP	gpio
	sdmmc0_data[0]	B	sdmmc0 data bit0
	SPI0_RXD	I	spi0 rxd
IO_GPIO0_B[2]	GPIO0_B[2]	B Pull UP	gpio
	sdmmc0_data[1]	B	sdmmc0 data bit1
IO_GPIO0_B[3]	GPIO0_B[3]	B Pull UP	gpio
	sdmmc0_data[2]	B	sdmmc0 data bit2
IO_GPIO0_B[4]	GPIO0_B[4]	B Pull UP	gpio
	sdmmc0_data[3]	B	sdmmc0 data bit3
IO_GPIO0_B[5]	GPIO0_B[5]	B Pull UP	gpio
	sdmmc0_clkout	O	sdmmc0 clock out
	SPI0_CLKO	O	spi0 clk out
IO_GPIO0_B[6]	GPIO0_B[6]	B Pull UP	gpio
	sdmmc0_detect_n	I	sdmmc0 detect signal
	SPI0_CSN1	O	spi0 second chip select
IO_GPIO0_B[7]	GPIO0_B[7]	B Pull UP	gpio
	sdmmc0_write_prt	I	sdmmc0 write protect
	SPI0_CSN0	O	spi0 first chip select
GPIO0_C			
IO_GPIO0_C[0]	GPIO0_C[0]	B Pull Up	gpio
	sdmmc0_data[4]	B	sdmmc0 data bit4
	pwm0	B	pwm
IO_GPIO0_C[1]	GPIO0_C[1]	B Pull Up	gpio
	sdmmc0_data[5]	B	sdmmc0 data bit5
IO_GPIO0_C[2]	GPIO0_C[2]	B Pull Up	gpio
	sdmmc0_data[6]	B	sdmmc0 data bit6
IO_GPIO0_C[3]	GPIO0_C[3]	B Pull Up	gpio
	sdmmc0_data[7]	B	sdmmc0 data bit7
IO_GPIO0_C[4]	GPIO0_C[4]	B Pull Up	gpio
	i2c0_sda	B	i2c0 sda
	flash_cs2	O	nand flash cs2
IO_GPIO0_C[5]	GPIO0_C[5]	B Pull Up	gpio
	i2c0_scl	B	i2c0 scl
	flash_cs3	O	nand flash cs3
IO_GPIO0_C[6]	GPIO0_C[6]	B Pull Up	gpio
	i2c1_sda	B	i2c1 sda
IO_GPIO0_C[7]	GPIO0_C[7]	B Pull Up	gpio
	i2c1_scl	B	i2c1 scl
GPIO0_D			
IO_GPIO0_D[0]	GPIO0_D[0]	B Pull Down	gpio
	lcdc_vsync/rk_tcon_sdoe	O	lcdc vertical sync signal
IO_GPIO0_D[1]	GPIO0_D[1]	B Pull Down	gpio
	lcdc_denable/rk_tcon_gdclk	O	lcdc data valid signal
IO_GPIO0_D[2]	GPIO0_D[2]	B Pull Down	gpio
	sm_cs1_n	O	nor flash second chip select
IO_GPIO0_D[3]	GPIO0_D[3]	B Pull Down	gpio
	sdmmc0_pwr_en	O	sdmmc0 power control

	SPI1_CS1	O	SPI1 chip select1 output
IO_GPIO0_D[4]	GPIO0_D[4]	B Pull Up	gpio
	uart0_sin	I	uart0 serial data in
IO_GPIO0_D[5]	GPIO0_D[5]	B Pull Up	gpio
	uart0_sout	O	uart0 serial data out
IO_GPIO0_D[6]	GPIO0_D[6]	B Pull Up	gpio
	uart0_cts_n	I	uart0 modem signal
IO_GPIO0_D[7]	GPIO0_D[7]	B Pull Up	gpio
	uart0_rts_n	O	uart0 modem signal
GPIO1_A			
IO_GPIO1_A[0]	GPIO1_A[0]	B Pull Up	gpio
	spi1_clkin/spi1_clkout	B	spi1 slave/master mode clock signal
IO_GPIO1_A[1]	GPIO1_A[1]	B Pull Up	gpio
	spi1_ss_n	I	spi1 slave mode select signal
IO_GPIO1_A[2]	GPIO1_A[2]	B Pull Up	gpio
	spi1_rxd	I	spi1 rxd
IO_GPIO1_A[3]	GPIO1_A[3]	B Pull Up	gpio
	spi1_txd	O	spi1 txd
IO_GPIO1_A[4]	GPIO1_A[4]	B Pull Up	gpio
	SPI1_CS0	O	SPI1 chip select0 output
IO_GPIO1_A[5]	GPIO1_A[5]	B Pull Down	gpio
	pwm1	B	pwm1
IO_GPIO1_A[6]	GPIO1_A[6]	B Pull Up	gpio
	uart1_sir_in	I	uart1_sir_in
	pwm2	B	pwm2
IO_GPIO1_A[7]	GPIO1_A[7]	B Pull Up	gpio
	uart1_sir_out_n	O	uart1_sir_out_n
	pwm3	B	pwm3
GPIO1_B			
IO_GPIO1_B[0]	gpio0_b[0]	B Pull down	gpio
	lcdc_data8/rk_tcon_sdce[0]	O	lcdc data bit8
IO_GPIO1_B[1]	gpio0_b[1]	B Pull down	gpio
	lcdc_data9/rk_tcon_sdce[1]	O	lcdc data bit9
IO_GPIO1_B[2]	gpio0_b[2]	B Pull down	gpio
	lcdc_data10/rk_tcon_sdce[2]	O	lcdc data bit10
IO_GPIO1_B[3]	gpio0_b[3]	B Pull down	gpio
	lcdc_data11/rk_tcon_border[0]	O	lcdc data bit11
IO_GPIO1_B[4]	gpio0_b[4]	B Pull down	gpio
	lcdc_data12/rk_tcon_border[1]	O	lcdc data bit12
IO_GPIO1_B[5]	gpio0_b[5]	B Pull down	gpio
	lcdc_data13/rk_tcon_vom	O	lcdc data bit13
IO_GPIO1_B[6]	gpio0_b[6]	B Pull down	gpio
	lcdc_data14/rk_tcon_sdshr	O	lcdc data bit14
IO_GPIO1_B[7]	gpio0_b[7]	B Pull down	gpio
	lcdc_data15/rk_tcon_gdoe	O	lcdc data bit15
GPIO1_C			
IO_GPIO1_C[0]	gpio1_c[0]	B Pull Up	gpio
	lcdc_data16//rk_tcon_gdsp	O	lcdc data bit16
	uart1_sin	I	uart1 serial data in

IO_GPIO1_C[1]	gpio1_c[1]	B Pull Up	gpio
	lcdc_data17/rk_tcon_gdrl	O	lcdc data bit17
	uart1_sout	O	uart1 serial data out
IO_GPIO1_C[2]	gpio1_c[2]	B Pull Up	gpio
	lcdc_data18/rk_tcon_gdpwr[0]	O	lcdc data bit18
IO_GPIO1_C[3]	gpio1_c[3]	B Pull Up	gpio
	lcdc_data19/rk_tcon_gdpwr[1]	O	lcdc data bit19
IO_GPIO1_C[4]	gpio1_c[4]	B Pull Up	gpio
	lcdc_data20/rk_tcon_gdpwr[2]	O	lcdc data bit20
IO_GPIO1_C[5]	gpio1_c[5]	B Pull Up	gpio
	lcdc_data21/rk_tcon_sdce[3]	O	lcdc data bit21
IO_GPIO1_C[6]	gpio1_c[6]	B Pull Up	gpio
	lcdc_data22/rk_tcon_sdce[4]	O	lcdc data bit22
IO_GPIO1_C[7]	gpio1_c[7]	B Pull Up	gpio
	lcdc_data23/rk_tcon_sdce[5]	O	lcdc data bit23
GPIO1_D			
IO_GPIO1_D[0]	gpio1_d[0]	B Pull Down	gpio
	vip_data0	I	vip data input0
IO_GPIO1_D[1]	gpio1_d[1]	B Pull Down	gpio
	vip_data1	I	vip data input1
IO_GPIO1_D[2]	gpio1_d[2]	B Pull Down	gpio
	vip_data2	I	vip data input2
IO_GPIO1_D[3]	gpio1_d[3]	B Pull Down	gpio
	vip_data3	I	vip data input3
IO_GPIO1_D[4]	gpio1_d[4]	B Pull Down	gpio
	vip_data4	I	vip data input4
IO_GPIO1_D[5]	gpio1_d[5]	B Pull Down	gpio
	vip_data5	I	vip data input5
IO_GPIO1_D[6]	gpio1_d[6]	B Pull Down	gpio
	vip_data6	I	vip data input6
IO_GPIO1_D[7]	gpio1_d[7]	B Pull Down	gpio
	vip_clkout	O	sensor clk out
GPIO2_A			
IO_GPIO2_A[0]	GPIO2_A[0]	B Pull Down	gpio
	hsadc_data_i[9]	I	hsadc data bit9 for I Path
	ts_fail	I	ts stream fail signal
IO_GPIO2_A[1]	GPIO2_A[1]	B Pull Down	gpio
	gps clk/HSADC_CLKIN	I	clock input for gps application
	hsadc_clkout	O	clock out to hsadc analog
IO_GPIO2_A[2]	GPIO2_A[2]	B Pull Down	gpio
	hsadc_data_i[8]	I	hsadc data bit8 for I Path
	ts_valid	I	ts stream valid signal
IO_GPIO2_A[3]	GPIO2_A[3]	B Pull Down	gpio
	host_addr0	I	host interface addr bit0
IO_GPIO2_A[4]	GPIO2_A[4]	B Pull up	gpio
	host_addr1	I	host interface addr bit1
IO_GPIO2_A[5]	GPIO2_A[5]	B Pull up	gpio
	host_csn	I	host interface chip select
IO_GPIO2_A[6]	GPIO2_A[6]	B Pull up	gpio
	host_rdn	I	host interface read valid signal
IO_GPIO2_A[7]	GPIO2_A[7]	B Pull up	gpio
	host_wrn	I	host interface write valid signal

GPIO2_B			
IO_GPIO2_B[0]	GPIO2_B[0]	B Pull Down	gpio
	hsadc_data_i[0]	I	hsadc data bit0 for I path
IO_GPIO2_B[1]	GPIO2_B[1]	B Pull Down	gpio
	hsadc_data_i[1]	I	hsadc data bit1 for I path
IO_GPIO2_B[2]	GPIO2_B[2]	B Pull Down	gpio
	hsadc_data_i[2]	I	hsadc data bit2 for I path
IO_GPIO2_B[3]	GPIO2_B[3]	B Pull Down	gpio
	hsadc_data_i[3]	I	hsadc data bit3 for I path
IO_GPIO2_B[4]	GPIO2_B[4]	B Pull Down	gpio
	hsadc_data_i[4]	I	hsadc data bit4 for I path
IO_GPIO2_B[5]	GPIO2_B[5]	B Pull Down	gpio
	hsadc_data_i[5]	I	hsadc data bit5 for I path
IO_GPIO2_B[6]	GPIO2_B[6]	B Pull Down	gpio
	hsadc_data_i[6]	I	hsadc data bit6 for I path
IO_GPIO2_B[7]	GPIO2_B[7]	B Pull Down	gpio
	hsadc_data_i[7]	I	hsadc data bit7 for I path
GPIO2_C			
IO_GPIO2_C[0]	GPIO2_C[0]	B Pull Down	gpio
	vip_data7	I	vip data input7
IO_GPIO2_C[1]	GPIO2_C[1]	B Pull Down	gpio
	vip_data8	I	vip data input8
IO_GPIO2_C[2]	GPIO2_C[2]	B Pull Down	gpio
	vip_data9	I	vip data input9
IO_GPIO2_C[3]	GPIO2_C[3]	B Pull Down	gpio
	vip_data10	I	vip data input10
IO_GPIO2_C[4]	GPIO2_C[4]	B Pull Down	gpio
	vip_data11	I	vip data input11
IO_GPIO2_C[5]	GPIO2_C[5]	B Pull Down	gpio
	vip_vsync	I	vip vertical sync signal
IO_GPIO2_C[6]	GPIO2_C[6]	B Pull Down	gpio
	vip_href	I	vip horizontal sync signal
IO_GPIO2_C[7]	GPIO2_C[7]	B Pull Down	gpio
	vip_clkin	I	vip clock input from sensor
GPIO2_D			
IO_GPIO2_D[0]	GPIO2_D[0]	B Pull Down	gpio
	host_data8	B	host_data[8]
IO_GPIO2_D[1]	GPIO2_D[1]	B Pull Down	gpio
	host_data9	B	host_data[9]
IO_GPIO2_D[2]	GPIO2_D[2]	B Pull Down	gpio
	host_data10	B	host_data[10]
IO_GPIO2_D[3]	GPIO2_D[3]	B Pull Down	gpio
	host_data11	B	host_data[11]
IO_GPIO2_D[4]	GPIO2_D[4]	B Pull Down	gpio
	host_data12	B	host_data[12]
IO_GPIO2_D[5]	GPIO2_D[5]	B Pull Down	gpio
	host_data13	B	host_data[13]
IO_GPIO2_D[6]	GPIO2_D[6]	B Pull Down	gpio
	host_data14	B	host_data[14]

IO_GPIO2_D[7]	GPIO2_D[7]	B Pull Down	gpio
	host_data15	B	host_data[15]
LCDC/EBOOK			
IO_LCDC_DATA[0]	lcdc_data0/rk_tcon_sddo[0]	O	lcd data[0]
IO_LCDC_DATA[1]	lcdc_data1/rk_tcon_sddo[1]	O	lcd data[1]
IO_LCDC_DATA[2]	lcdc_data2/rk_tcon_sddo[2]	O	lcd data[2]
IO_LCDC_DATA[3]	lcdc_data3/rk_tcon_sddo[3]	O	lcd data[3]
IO_LCDC_DATA[4]	lcdc_data4/rk_tcon_sddo[4]	O	lcd data[4]
IO_LCDC_DATA[5]	lcdc_data5/rk_tcon_sddo[5]	O	lcd data[5]
IO_LCDC_DATA[6]	lcdc_data6/rk_tcon_sddo[6]	O	lcd data[6]
IO_LCDC_DATA[7]	lcdc_data7/rk_tcon_sddo[7]	O	lcd data[7]
IO_LCDC_HSYNC	lcdc_hsync/rk_tcon_sdle	O	lcdc horizontal sync signal
IO_LCDC_DCLK	lcdc_dclk/rk_tcon_sdclk	O	lcdc data clock
FLASH/eMMC			
IO_FLASH_DATA[0]	flash_data0	B Pull Up	nand flash data[0]
	SDMMC1_data[0]	B	SDMMC1 data bit0
IO_FLASH_DATA[1]	flash_data1	B Pull Up	nand flash data[1]
	SDMMC1_data[1]	B	SDMMC1 data bit1
IO_FLASH_DATA[2]	flash_data2	B Pull Up	nand flash data[2]
	SDMMC1_data[2]	B	SDMMC1 data bit2
IO_FLASH_DATA[3]	flash_data3	B Pull Up	nand flash data[3]
	SDMMC1_data[3]	B	SDMMC1 data bit3
IO_FLASH_DATA[4]	flash_data4	B Pull Up	nand flash data[4]
	SDMMC1_data[4]	B	SDMMC1 data bit4
IO_FLASH_DATA[5]	flash_data5	B Pull Up	nand flash data[5]
	SDMMC1_data[5]	B	SDMMC1 data bit5
IO_FLASH_DATA[6]	flash_data6	B Pull Up	nand flash data[6]
	SDMMC1_data[6]	B	SDMMC1 data bit6
IO_FLASH_DATA[7]	flash_data7	B Pull Up	nand flash data[7]
	SDMMC1_data[7]	B	SDMMC1 data bit7
IO_FLASH_RDY	flash_rdy	I Pull Up	nand flash ready/busy
	SDMMC1_detect_n	I	SDMMC1_detect_n
IO_FLASH_ALE	flash_ale	O	nand flash ale
IO_FLASH_CLE	flash_cle	O	nand flash cle
IO_FLASH_RDN	flash_rdn	O	nand flash rdn
	SDMMC1_power_en	O	sdmmc1 power en
IO_FLASH_WRN	flash_wrn	O	nand flash wrn
	SDMMC1_cmd	I Pull Up	
IO_FLASH_WP	flash_wp	O	nand flash wp
	SDMMC1_write_prt	I Pull Up	
IO_FLASH0_CSN	flash_cs0	O	nand flash cs0
	SDMMC1_clkout	O	
IO_FLASH1_CSN	flash_cs1	O	nand flash cs1

Notes : B --- Bidirectional IO
I --- Input IO
O --- Output IO

Chapter 3 Hardware Information

3.1 Oscillator Connection

RK2738 will use one oscillator for input of three on-chip PLLs, for USB OTG PHY, and for I2S main clock, which should be 24MHz. The design for oscillator pad has been optimized for stability and minimum jitter, and characterized to allow a variation of 4pF to 18pF on both XI and XO pins for crystal stability. In the Fig. 3-1, the variation range for C value is 4pF to 18pF.

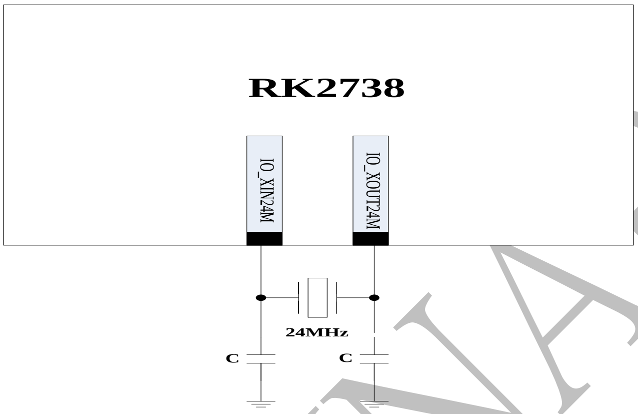


Fig. 3-1 RK2738 external oscillator connection diagram

27.2 USB PHY Connection

USB2.0 OTG PHY is used in RK2738 for USB host, USB device and otg functions. The following figure shows external connection for USB PHY interface.

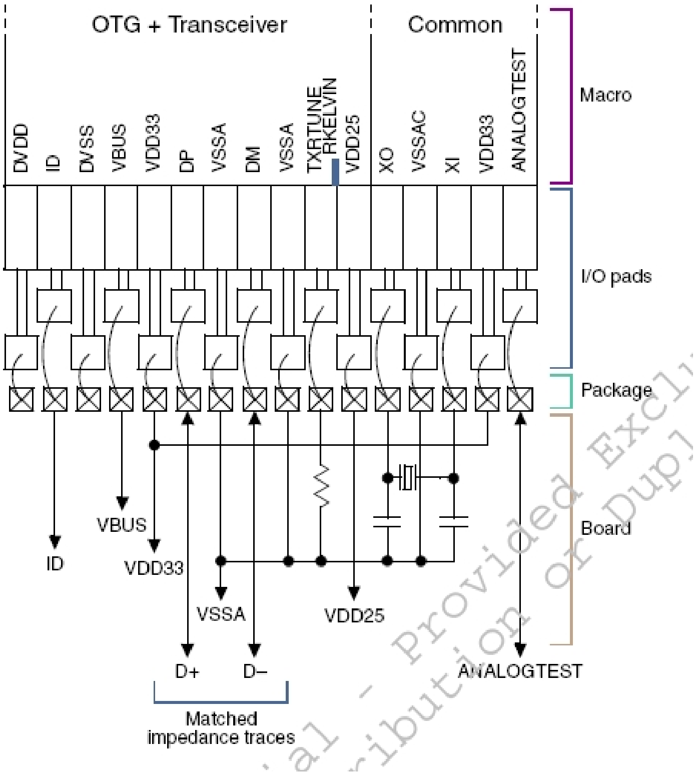


Fig. 27-2 RK2738 USB PHY connection diagram

In the above diagram, some parameters and its viariant will be shown in the following table.

External resistor (REXT)	43.2 Ω (± 1%)
Analog power supplies	3.3 V (+ 10%, – 7%) at the macro pins with respect to VSSA and VSSAC 2.5 V (+ 10%, – 7%) at the macro pins with respect to VSSA and VSSAC
Digital power supply	1.2 V (+ 10%, – 7%) at the macro pins with respect to DVSS
Junction temperature	–40° C through +125° C

27.3 Power up Sequence for power supply

For IO and core power supply of RK2738, there are no power sequence requirements, since IO is 3-state when core power is not valid.

27.4 Power on reset Descriptions

The following figure shows power-on-reset sequence and relative clock behavior. When npor (power-on-reset) is released after stabilization of oscillator clock xin24M. After about T1 timing length, power supply for on-chip PLLs will be in stable state and pll_rstn (internal reset signal for PLL) is released. Then after (T2-T1) timing length, chip_rstn (internal reset signal for chip logic) is released. Then clock for IP module inside chip will be valid . After about 15 clocks, ip_rstn (internal reset signal for all IPs) will be released, which can meet some special requirements for some IPs, reset signal will be kept valid no less than 15 clock cycles.

Notes : T1 is about 5us ; T2 is about 139us

Another, RK2738 can filter out 5 clock cycles for low pulse of npor; the clock cycle is xin24m clock, so about 208ns low pulse of npor will not be recognized as valid power-on-reset signal for RK2738.

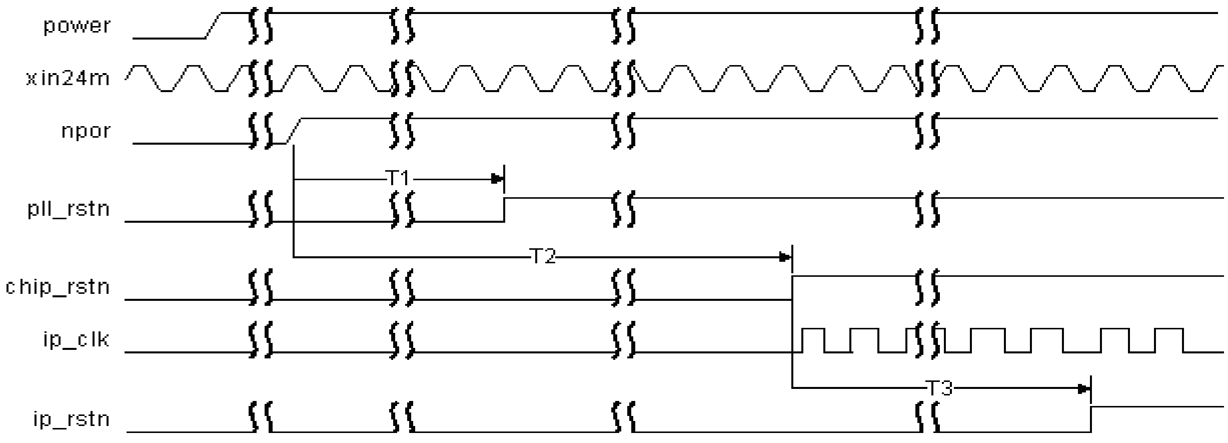


Fig. 27-3 RK2738 reset sequence timing waveform

Chapter 4 Electrical Specification

4.1 Absolute Maxinum Ratings

Paramerters	Symbol	Min	Max	Unit
Power Supply Voltage (Digital Core)	VDD	-0.5	1.8	V
Power Supply Voltage (Digital IO)	VCCIO	-0.5	4.6	V
IO Power Supply Voltage (SDRAM IO)	VDDSDR	-0.5	4.6	V
Digital IO Input Voltage	V_I	-0.5	VCCIO+0.5	V
Digital IO Output Voltage	V_o	-0.5	VCCIO+0.5	V
Operation Temperature	T_{opt}	-40	125	^{0}C
Storage Temperature	T_{stg}	-55	150	^{0}C

4.2 Recommended Operating Conditions

Symbol	Paramerters	Min	Typ	Max	Unit
VDD	Power Supply Voltage (Digital Core)	1.08	1.2	1.32	V
VCCIO	Power Supply Voltage (Digital IO)	2.97	3.3	3.63	V
VDDSDR	IO Power Supply Voltage (SDRAM IO)	2.97	3.3	3.63	V
VDDA_xPLL	Power Supply Voltage (PLL)	1.08	1.2	1.32	V
AVDD33_USB	Power Supply Voltage (USB Analog part)	2.97	3.3	3.63	V
DVDD_USB	Power Supply Voltage (USB digital part)	1.08	1.2	1.32	V
DVSS_USB	Ground Voltage (USB digital part)	N/A	0	N/A	V
VDDA_ADC	Power Supply Voltage (SAR-ADC Analog)	2.8	3	3.6	V
XIN24M	PLL Input clock frequency	N/A	24	N/A	MHz
T_{opt}	Operating Temperature	-10	25	40	^{0}C

4.3 IO DC Characteristics

Symbol	Paramerters	Min	Typ	Max	Unit
Vil	Input Low Voltage	-0.3	N/A	0.8	V
Vih	Input High Voltage	2.0	N/A	VCCIO+0.3	V
Vol	Output Low Voltage			0.4	V
Voh	Output High Voltage	2.4			V
Rpu	Pull-up Resistor	33k	41K	62K	Ohms
Rpd	Pull-down Resistor	33K	42K	68K	Ohms
Iol	Low level output Curent @Vol=0.45V	4.4	8	11.2	mA
Ioh	High level output current @VCCIO-0.45V	3.6	6	8.4	mA