RK2729
Technical Reference Manual
Brief

Revision 1.0
Mar 2010

Revision History

Date	Revision	Description
2010-3-2	1.0	Initial Release

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Chapter 1 Introduction

1.1 Overview

RK2729 is a highly-integrated, high-performance, low-power digital multimedia processor which is based on Dual Core (DSP+CPU) architecture with hardware accelerator.

RK2729 is focus on EBOOK application, it can support TFT and EPD display for various ebook formats, like PDF, EPUB, FB2,etc.. With DSP software, RK2729 also can decode various types of video formats, resolution up to 1280x720 formats. The DSP also can decoder picture for photo and ebook application.

1.2 Features

- **System Operation**
  - Dual Core Architecture (ARM926EJC + DSP)
  - Support system boot sequentially from ARM to DSP
  - Support address remap function
  - For two cores, all modules have unified address space
  - ARM9 JTAG debug method

- **Communication between two cores**
  - Support share memory and interactive interrupt method to complete communication
  - Processor Interface Unit (PIU)
    - Built-in three Command/reply protocols registers and three Semaphore registers to accessed by two cores
    - Support three semaphore-related interrupts and one command-reply-related interrupt between two cores
- **Clock & Power Management**
  - Three on-chip PLLs for ARM9 subsystem, DSP subsystem and Other logic
  - Support different DSP Core and internal AHB Bus clock ratio:
    1:1, 1:2, 1:3, 1:4, up to 1:16 mode
  - Support different DSP internal AHB Bus and internal APB Bus clock ratio:
    1:1, 1:2, 1:3, 1:4, up to 1:16 mode
  - Support different ARM9 core and AHB Bus clock ratio:
    1:1, 1:2, 1:3 and 1:4 mode
  - Support different ARM AHB Bus and ARM APB Bus clock ratio:
    1:1, 1:2 and 1:4 modes
  - 6 types of work modes by clock gating to save power :
    - Normal mode : Normal operating mode
    - Slow mode : Low frequency clock (24MHz) without PLL
    - Deep Slow mode : More Low frequency clock (32.768KHz) without PLL
    - Idle mode : The clock for only CPU is stopped ,
      Wake up by any interrupts to CPU from idle mode
    - Sleep mode : The clock for only DSP is stopped ,
      Wake up from sleep mode by some interrupts to DSP or register set from CPU
    - Stop mode : All clocks will be stopped , and SDRAM into Self-refresh, all PLLs into power-down mode,
      Wake up from stop mode by external pin or RTC alarm interrupt
  - Support power supply shut down for 4 domain separately

- **Memory Interface**
  - Static/SDRAM Memory controller

- Support industrial standard SDRAM from 16MB to 128 MB devices
- Only 16 bits SDRAM data bus.
- Support SDRAM power-down mode
- Support SDRAM self-refresh mode
- Programmable arbitration priority for 5 slave data ports

- Nand Flash controller
  - Support 4 chip selects for nand flash
  - support 8bits wide data
  - Flexible CPU interface support
  - Embedded 4x512B size buffer to improve performace
  - Support internal DMA transfer from/to flash
  - 512B、2KB、4KB page size support
  - Support hardware ECC up to 14bits
- SD/MMC controller
  - Embedded SD/MMC Controllers
  - Compliant with SD Memory/SDIO with 1bit and 4bit data bus
  - Compliant with MMC V3.3 and V4.0 with 1/4bit data bus
  - Support combined single 32x32bits FIFO for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock
  - Variable SD/MMC card clock rate 0 – 52 MHz which depends on AHB clock frequency
  - Controllable SD/MMC card clock to save power consumption
  - Support card detection and initialization , and write protection
  - Support transfer block size of 1 to 65365Bytes
  - DMA based or Interrupt based operation

- **VIDEO interface**
  - LCD controller
    - Embedded DMA function
    - Support one SCALE window and one no SCALE window
    - YUV422/YUV420/RGB565/RGB888 Input are Supported in SCALE window
    - RGB565/RGB888 Input and 4 AREAS are Supported in NO SCALE window
    - Support Virtual Display
    - Build in scaler engine from 1/8 to 8
    - Support 16 grade alpha blending and transparent operation.
    - Support Blank/Black Function
    - Support LCD Pannel resolution up to 480X272
    - Compatible with MCU Pannel
    - Support MCU PANNEL Bypass Mode and SCALE Mode
    - Compatible with RGB Delta/no-Delta Pannel
    - Compatible with RGB Series/Parallel 24bits (max) Output
    - Compatible with CCIR656 output
    - Support Interlace and Progressive Output
    - Support LCDC high-z control
    - Support LCDC interface bypass from Host interface
    - Support EPD display.

- **DMA Controller**
  - Two DMA Controllers in chip
  - DW_DMA Controller integrated inside ARM9 subsystem
    - Three DMA Channels support to use by audio , sd/mmc and system data transfer
    - 8 hardware request handshaking support
    - Support hardware and software trigger DMA transfer mode
    - Build-in 3 data FIFO：64Bytes/32Bytes/16Bytes

- Scatter/Gather transfer support
- LLP transfer support
- Two masters for on-the-fly support
- The master interface only support undefined length INCR transfer

- 3D-DMA Controller(XDMA) integrated inside DSP subsystem
  - This DMA focus on data transfer for video process and mobile TV application
  - 16 configurable DMA channels, 4 channels support 3-dimensional data transfer
  - 8/16/32/64bit data transfer support and configurable burst length (INCR/INCR4/INCR8)
  - Programmable source and destination addresses with a post-modification option
  - Configurable external channel triggering (edge or level)
  - Support chaining-channels ,linked list-transfer and auto-channel initialization operating mode
  - Pause and resume operations supported to save power
  - Eight-stage memory buffer FIFO

- **Interrupt Controller**
  - Two Interrupt Controller in chip
  - DW_INTC integrated inside ARM9 subsystem
    - Support 32 IRQ normal interrupt sources and 4 FIQ fast interrupt sources
    - Vectored interrupts support
    - Software interrupts support
    - Programmable interrupt priorities
    - Programmable High/Low Level sensitive or Negative / Positive edge triggered interrupts
  - ICU (Interrupt Control unit) integrated inside DSP subsystem
    - 48 interrupt sources , each may be linked to different interrupt inputs for DSP core
    - Software triggering to all 48 interrupt sources
    - Configurable source interrupt polarity (low/high)
    - External interrupt source with software configuration to edge/level sensitive

- **USB interface**
  - Complies with the OTG Supplement to the USB2.0 Specification
  - Operates in High-Speed and Full-Speed mode
  - Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
  - Support 6 channels in host mode
  - 6 endpoints, 3 in and 3 out
  - Built-in one 1777 x 35bits FIFO

- **Low_speed Peripheral interface**
  - Serial Peripheral Interface (SPI) Master Controller
    - Support one slave devices connection
    - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National Semiconductor Microwire interface
    - Dynamic control of serial bit rate of data transfer by programmable sclk_out frequency, which is half of PCLK in max mode
    - FIFO depth for transmit and receive are also 16x16bits
    - Programmable data item size ,from 4 to 16bits
    - DMA based and interrupt based operation
  - Serial Peripheral Interface (SPI) Slave Controller
    - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National Semiconductor Microwire interface
    - Dynamic control of serial bit rate of data transfer by sclk_in from master

device
- FIFO depth for transmit and receive are also 16x16bits
- Programmable data item size ,from 4 to 16bits
- DMA based and interrupt based operation

- UART0
  - Based on the 16550 industry standard
  - UART0 support modem function and Serial data transfer
  - Programmable serial data baud rate , up to 1.5Mbps
  - DMA based and interrupt based operation
  - FIFO depth for data transfer is 32x8bits
- UART1
  - Only IrDA SIR mode, support configurable baud data rate up to 115.2K and a pulse duration as specified in the IrDA physical layer specification
  - DMA based and interrupt based operation
  - FIFO depth for data transfer is 32x8bits
- I2C controller
  - 2 I2C controllers integrated in chip
  - Multi masters operation support
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support mono/stereo audio file
  - Support audio resolution: 8, 16 bits
  - Support audio sample rate from 32KHz to 96 KHz
  - Support I2S, Left-Justified and Right-Justified digital serial data format
- PWM
  - Built-in three 32 bit timer modulers
  - Programmable counter
  - Chained timer for long period purpose
  - 2-channel 32-bit timer with Pulse Width Modulation (PWM)
  - Programmable duty-cycle, and frequency output
- General Purpose IO (GPIO)
  - Support 96 individually programmable input/output pins
  - 16 GPIOs with external interrupt capability
- Timers in CPU system
  - Built-in Three 32 bits timer modules
  - Support for two operation modes : free-running and user-defined count
- Timers in DSP system
  - Built-in two 32 bits timer modules
  - Support for 5 various counting modes : Single Count mode, Auto-restart mode , Free-running , Event Count mode and Watchdog Timer mode
  - Pulse Width Modulation(PWM) mechanism
  - Three possible input clock signals: internal , external and cascaded
- Watchdog Timer (WDT)
  - Watchdog function (Generate a system reset or an interrupt)
  - Built-in 32 bits programmable counter

- **Analog IP interface**
  - ADC Converter
    - 2-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
    - No off-chip components required
    - DNL less than +/-1 LSB , INL less than +/-1.5 LSB
    - Supply 2.8V to 3.6V for analog interface

- **Operation Temperature Range**
  - -40°C to +125°C

- **Operation Voltage Range**
  - Core: 1.2V
  - I/O : 3.3V/2.5V (2.5V for USB OTG PHY)

- **Package Type**
  - RK2729 LQFP176 (14mmX14mm body size)

- **Power**
  - TBD

1.3 Block Diagram

The following figure shows block diagram of RK2729.
RK2729 can be divided into two sub system: DSP System and CPU System.

- **DSP System**
  - XDMA : three-dimensional DMA , used to data transfer for video decoder or other algorithm
  - High-Speed ADC Interface: focus on completing data reveiver from tuner in DVB-T, DAB, T-DMB, GPS application with software method.
  - ICU : Interrupt controller for DSP processor
  - PIU : processor interface unit, used to complete communication between DSP and CPU
  - PMU :power management unit, used to control clock and reset to save power for modules inside DSP system
  - General reg file : focus on general control on DSP system by software method, composed of some register groups
  - Share Memx : can be accessed by DSP , CPU or Demodulator, which is switched by software programm
- **CPU System**
  - DW_DMA : used to data transfer for audio and low-speed peripheral
  - SCU : focus on clock gating , clock frequency switch, reset control , power on/off and system mode switch for CPU system to save power
  - PMU : used to complete power on/off switch control for RK2729
  - INTC : Interrupt controller for CPU processor
  - General reg file: focus on general control on CPU system by software method, composed of some register groups, including IO mux control,IO PAD pull up/down control and other system control signals .

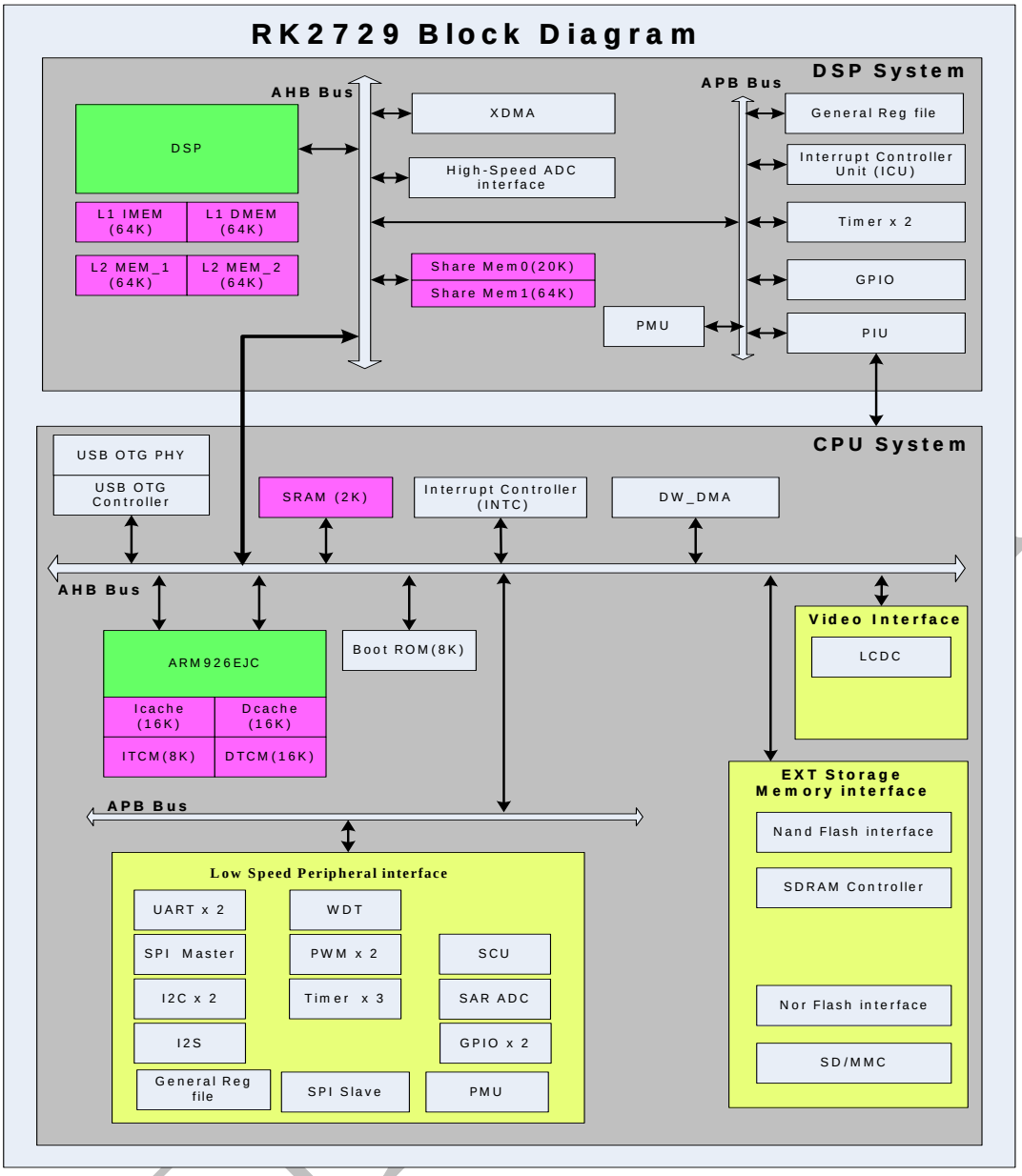

Fig. 1-1 RK2729 Block Diagram

Chapter 2 Pin Description

2.1 PIN Placement

		176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144	143	142	141	140	139	138	137	136	135	134	133		
		LCDC_VSYNC	LCDC_DE	NC	GND	LCDC_DCLK	NC	LCDC_HSYNC	NC	VCC	TCK	TRST_N	TDI	TMS	TDO	RTCK	PA3	VCC	VDD	GND	GND	NC	PA4	NPOR	PF5/PWM3/DEM_PWM	PWM0/PF2	PF7/SPI_TXD	PE1/SPI_CLKIN	PE2/SPI_SS_IN	PE3/SPI_RXD	PH6	VCC	GND	VDD	PH7	PB1/SM_CS1/SD0_PCA	PA0	PA1	PE7/UART1_SIR_OUT/I2C1_SCL	PE6/UART1_SIR_IN/I2C1_SDA	PB2/UART0_CTS	PB3/UART0_RTS	I2S_CLK	I2S_SCLK	I2S_SDO		
1	LCDC_D16/PC0																																												I2S_LRCK	132
2	LCDC_D17/PC1																																												I2S_SDI	131
3	LCDC_D15/PD7																																												VCC	130
4	LCDC_D14/PD6																																												GND	129
5	LCDC_D13/PD5																																												VDD	128
6	LCDC_D12/PD4																																												I2C0_SDA/PE4	127
7	LCDC_D23/PC7																																												I2C0_SCL/PE5	126
8	LCDC_D22/PC6																																												PB0_SPIO_CS1_SD1_PCA	125
9	LCDC_D21/PC5																																												PG1/UART0_TX/SD1_WP	124
10	VCC																																												PG0/UART0_RX/SD1_DET	123
11	LCDC_D11/PD3																																												PB6/SPI0_TXD/SD0_D6	122
12	LCDC_D10/PD2																																												PB7/SPI0_RXD/SD0_D7	121
13	LCDC_D9/PD1																																												PB5/SPI0_CLKT/SD0_D5	120
14	LCDC_D8/PD0																																												XOUT24M	119
15	LCDC_D7																																												XIN24M	118
16	LCDC_D6																																												VDDA_CODECPLL	117
17	VDD																																												VDDA_ARMPLL	116
18	LCDC_D5																																												VDDA_DSPPLL	115
19	LCDC_D4																																												SD0_CLK/PH5	114
20	LCDC_D3																																												SD0_D2/PH3	113
21	LCDC_D2																																												SD0_D3/PH4	112

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Pin	Name	Name	Pin
22	LCDC_D1	SD0_D0/PH1	111
23	LCDC_D0	SD0_D1/PH2	110
24	LCDC_D20/PC4	SD0_CMD/PH0	109
25	LCDC_D19/PC3	VDD	108
26	LCDC_D18/PC2	FLASH_CLE	107
27	SDR_CLK	FLASH_ALE	106
28	SDR_D0	FLASH_WRN	105
29	SDR_D1	FLASH_RDY	104
30	SDR_D2	FLASH_RDN	103
31	SDR_D3	GND	102
32	SDR_D4	VCC	101
33	VCC	FLASH_CS1/PA5	100
34	SDR_D5	FLASH0_CSN	99
35	SDR_D7	FLASH_CS2/PA6	98
36	SDR_D6	FLASH_CS3/PA7	97
37	SDR_D8	FLASH_D7	96
38	SDR_D9	FLASH_D6	95
39	SDR_D11	FLASH_D4	94
40	SDR_D10	FLASH_D5	93
41	SDR_D12	FLASH_D2	92
42	VDD	FLASH_D3	91
43	SDR_D13	FLASH_D1	90
44	SDR_D15	FLASH_D0	89

Pin	Name
45	SDR_D14
46	SDR_BA1
47	SDR_BA0
48	SDR_A1
49	SDR_A0
50	SDR_A3
51	SDR_A2
52	SDR_DQM0
53	SDR_DQM1
54	SDR_A4
55	SDR_A5
56	SDR_A6
57	SDR_A7
58	VCC
59	VDD
60	GND
61	SDR_A8
62	SDR_A9
63	SDR_A10
64	SDR_A11
65	SDR_A12
66	SDR_CSN
67	SDR_WEN
68	SDR_CASN
69	SDR_RASN
70	GND
71	VCC
72	VDD
73	VBUS
74	USBPHY_AVDD33
75	USBPHY_AVSS
76	DP
77	RKELVIN
78	DM
79	USBPHY_AVSS
80	USBPHY_AVDD25
81	USBPHY_DVDD
82	USBPHY_DVSS
83	SARADC_AIN0
84	SARADC_AIN1
85	VDDA_SARADC
86	VSSA_SARADC
87	VDD
88	VCC

Note:

1. Only the GPIO of port A and E can use as ARM interrupt port.

2.2 PIN Description

The following table shows all of the pins for RK2729.

The first column in the pin function description is default function after power on reset, and function in the last two columns will be implemented by software set.

The detailed register descriptions are IOMUX_A_CON and IOMUX_B_CON in chapter 34.

As for GPIO_n[i] (n = A~H; i = 0~7), we can control Pull up or Pull Down or no resistor for them by software set. The value for Pull up/down type in the following table is default after power on reset. The detailed register descriptions are in chapter 34.

Notes *I --- input pins*
O --- output pins
B --- bidirectional pins
P --- power supply pins (digital and analog)
G --- ground supply pins (digital and analog)
A --- Analog IO pins
OSC --- oscillator IO pins

Table 2-1 RK2729 Pin Description

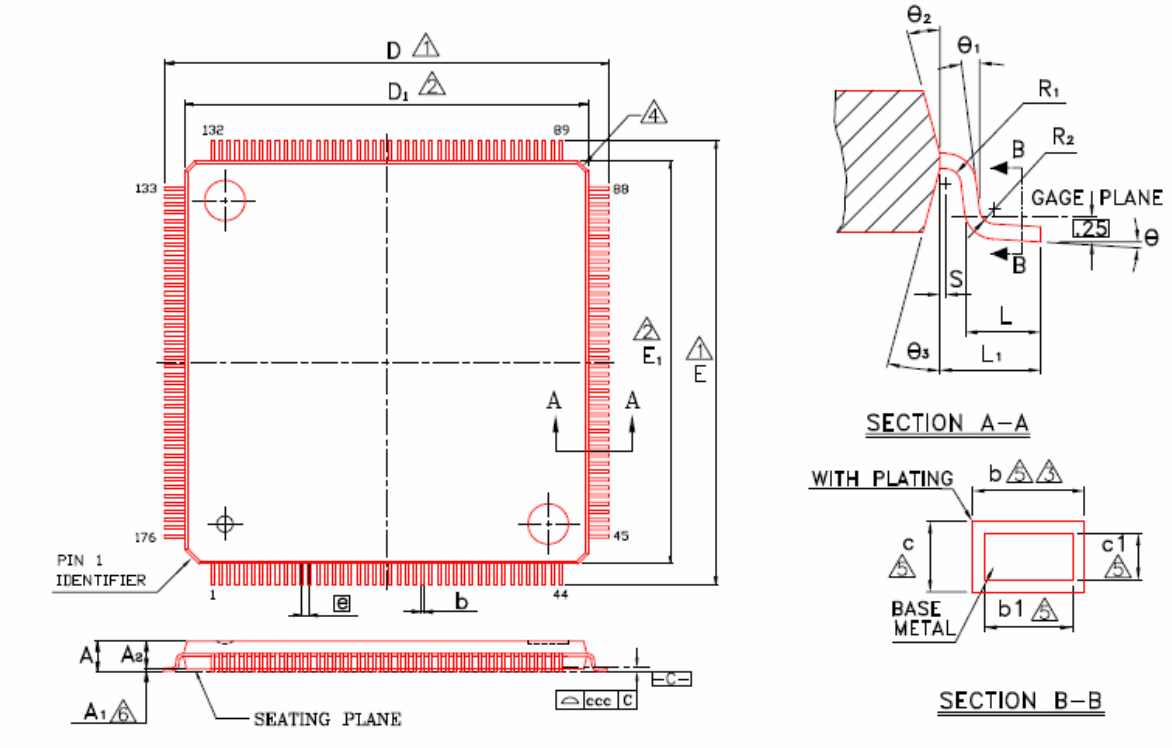
PIN NUMBER	PIN NAME	PIN TYPE (DEFAULT)	PULL UP/DOWN (DEFAULT)	PIN FUNCTION DESCRIPTION (DEFAULT)	PIN FUNCTION DESCRIPTION (FUNCTION MUX1)	PIN FUNCTION DESCRIPTION (FUNCTION MUX2)
1	LCDC_D16/PC0	B	PULL UP	GPIO PORT C BIT0	LCDC DATA BIT16	
2	LCDC_D17/PC1	B	PULL UP	GPIO PORT C BIT1	LCDC DATA BIT17	
3	LCDC_D15/PD7	B	PULL UP	GPIO PORT D BIT7	LCDC DATA BIT15	
4	LCDC_D14/PD6	B	PULL UP	GPIO PORT D BIT6	LCDC DATA BIT14	
5	LCDC_D13/PD5	B	PULL UP	GPIO PORT D BIT5	LCDC DATA BIT13	
6	LCDC_D12/PD4	B	PULL UP	GPIO PORT D BIT4	LCDC DATA BIT12	
7	LCDC_D23/PC7	B	PULL UP	GPIO PORT C BIT7	LCDC DATA BIT23	
8	LCDC_D22/PC6	B	PULL UP	GPIO PORT C BIT6	LCDC DATA BIT22	
9	LCDC_D21/PC5	B	PULL UP	GPIO PORT C BIT5	LCDC DATA BIT21	
10	VCC	P	N/A	IO POWER (3.3 V)		
11	LCDC_D11/PD3	B	PULL UP	GPIO PORT D BIT3	LCDC DATA BIT11	
12	LCDC_D10/PD2	B	PULL UP	GPIO PORT D BIT2	LCDC DATA BIT10	
13	LCDC_D9/PD1	B	PULL UP	GPIO PORT D BIT1	LCDC DATA BIT9	
14	LCDC_D8/PD0	B	PULL UP	GPIO PORT D BIT0	LCDC DATA BIT8	
15	LCDC_D7	O	N/A	LCDC DATA BIT7		
16	LCDC_D6	O	N/A	LCDC DATA BIT6		
17	VDD	P	N/A	CORE POWER (1.2V)		
18	LCDC_D5	O	N/A	LCDC DATA BIT5		
19	LCDC_D4	O	N/A	LCDC DATA BIT4		
20	LCDC_D3	O	N/A	LCDC DATA BIT3		
21	LCDC_D2	O	N/A	LCDC DATA BIT2		
22	LCDC_D1	O	N/A	LCDC DATA BIT1		
23	LCDC_D0	O	N/A	LCDC DATA BIT0		
24	LCDC_D20/PC4	B	PULL UP	GPIO PORT C BIT4	LCDC DATA BIT20	
25	LCDC_D19/PC3	B	PULL UP	GPIO PORT C BIT3	LCDC DATA BIT19	
26	LCDC_D18/PC2	B	PULL UP	GPIO PORT C BIT2	LCDC DATA BIT18	
27	SDR_CLK	O	N/A	SDRAM CLOCK OUTPUT		
28	SDR_D0	B	N/A	SDRAM DATA BIT0		
29	SDR_D1	B	N/A	SDRAM DATA BIT1		
30	SDR_D2	B	N/A	SDRAM DATA BIT2		
31	SDR_D3	B	N/A	SDRAM DATA BIT3		
32	SDR_D4	B	N/A	SDRAM DATA BIT4		
33	VCC	P	N/A	IO POWER (3.3 V)		
34	SDR_D5	B	N/A	SDRAM DATA BIT5		
35	SDR_D7	B	N/A	SDRAM DATA BIT6		
36	SDR_D6	B	N/A	SDRAM DATA BIT7		
37	SDR_D8	B	N/A	SDRAM DATA BIT8		
38	SDR_D9	B	N/A	SDRAM DATA BIT9		

39	SDR_D11	B	N/A	SDRAM DATA BIT10		
40	SDR_D10	B	N/A	SDRAM DATA BIT11		
41	SDR_D12	B	N/A	SDRAM DATA BIT12		
42	VDD	P	N/A	CORE POWER (1.2V)		
43	SDR_D13	B	N/A	SDRAM DATA BIT13		
44	SDR_D15	B	N/A	SDRAM DATA BIT15		
45	SDR_D14	B	N/A	SDRAM DATA BIT14		
46	SDR_BA1	O	N/A	SDRAM BAND ADDRESS BIT1		
47	SDR_BA0	O	N/A	SDRAM BAND ADDRESS BIT0		
48	SDR_A1	O	N/A	SDRAM/SRAM ADDR BIT1		
49	SDR_A0	O	N/A	SDRAM/SRAM ADDR BIT0		
50	SDR_A3	O	N/A	SDRAM/SRAM ADDR BIT3		
51	SDR_A2	O	N/A	SDRAM/SRAM ADDR BIT2		
52	SDR_DQM0	O	N/A	SDRAM DQM BIT0		
53	SDR_DQM1	O	N/A	SDRAM DQM BIT1		
54	SDR_A4	O	N/A	SDRAM/SRAM ADDR BIT4		
55	SDR_A5	O	N/A	SDRAM/SRAM ADDR BIT5		
56	SDR_A6	O	N/A	SDRAM/SRAM ADDR BIT6		
57	SDR_A7	O	N/A	SDRAM/SRAM ADDR BIT7		
58	VCC	P	N/A	IO POWER (3.3 V)		
59	VDD	P	N/A	CORE POWER (1.2V)		
60	GND	G	N/A	CORE and IO GROUND		
61	SDR_A8	O	N/A	SDRAM/SRAM ADDR BIT8		
62	SDR_A9	O	N/A	SDRAM/SRAM ADDR BIT9		
63	SDR_A10	O	N/A	SDRAM/SRAM ADDR BIT10		
64	SDR_A11	O	N/A	SDRAM/SRAM ADDR BIT11		
65	SDR_A12	O	N/A	SDRAM/SRAM ADDR BIT12		
66	SDR_CSN	O	N/A	SDRAM CHIP SELECT		
67	SDR_WEN	O	N/A	SDRAM WEN		
68	SDR_CASN	O	N/A	SDRAM CASN		
69	SDR_RASN	O	N/A	SDRAM RASN		
70	GND	G	N/A	CORE and IO GROUND		
71	VCC	P	N/A	IO POWER (3.3 V)		
72	VDD	P	N/A	CORE POWER (1.2V)		
73	VBUS	P	N/A	USB DEDECT INPUT OR 5V POWER SUPPLY FOR OTG FUNCTION		
74	USBPHY_AVDD33	P	N/A	USB ANALOG POWER SUPPLY (3.3V)		
75	USBPHY_AVSS	G	N/A	USB ANALOG GROUND (0V)		
76	DP	A	N/A	USB D+ SIGNAL		
77	RKELVIN	A	N/A	TRANSMITTER RESISTOR TUNE PIN		
78	DM	A	N/A	USB D- SIGNAL		
79	USBPHY_AVSS	G	N/A	USB ANALOG GROUND (0V)		
80	USBPHY_AVDD25	P	N/A	USB ANALOG POWER SUPPLY (2.5V)		
81	USBPHY_DVDD	G	N/A	USB DIGITAL POWER SUPPLY (1.2V)		
82	USBPHY_DVSS	G	N/A	USB DIGITAL GROUND (0V)		
83	SARADC_AIN0	A	N/A	10BIT ADC CHANNEL0 INPUT		
84	SARADC_AIN1	A	N/A	10BIT ADC CHANNEL1 INPUT		
85	VDDA_SARADC	P	N/A	10BIT ADC ANALOG POWER AND REFERENCE VOLTAGE (3.3V)		
86	VSSA_SARADC	G	N/A	10BIT ADC ANALOG GROUND (0V)		
87	VDD	P	N/A	CORE POWER (1.2V)		
88	VCC	P	N/A	IO POWER (3.3 V)		
89	FLASH_D0	B	N/A	NAND FLASH DATA BIT0		
90	FLASH_D1	B	N/A	NAND FLASH DATA BIT1		
91	FLASH_D3	B	N/A	NAND FLASH DATA BIT3		
92	FLASH_D2	B	N/A	NAND FLASH DATA BIT2		

93	FLASH_D5	B	N/A	NAND FLASH DATA BIT5		
94	FLASH_D4	B	N/A	NAND FLASH DATA BIT4		
95	FLASH_D6	B	N/A	NAND FLASH DATA BIT6		
96	FLASH_D7	B	N/A	NAND FLASH DATA BIT7		
97	FLASH_CS3/PA7	B	PULL UP	GPIO PORT A BIT7	NAND FLASH CHIP SELECT 3	
98	FLASH_CS2/PA6	B	PULL UP	GPIO PORT A BIT6	NAND FLASH CHIP SELECT 2	
99	FLASH0_CSN	O	N/A	NAND FLASH CHIP SELECT 0		
100	FLASH_CS1/PA5	B	PULL UP	GPIO PORT A BIT5	NAND FLASH CHIP SELECT 1	
101	VCC	P	N/A	IO POWER (3.3 V)		
102	GND	G	N/A	CORE and IO GROUND		
103	FLASH_RDN	O	N/A	NAND FLASH RDN		
104	FLASH_RDY	I	PULL UP	NAND FLASH READY/BUSY SINGAL INPUT		
105	FLASH_WRN	O	N/A	NAND FLASH WE		
106	FLASH_ALE	O	N/A	NAND FLASH ALE		
107	FLASH_CLE	O	N/A	NAND FLASH CLE		
108	VDD	P	N/A	CORE POWER (1.2V)		
109	SD0_CMD/PH0	B	PULL DOWN	GPIO PORT H BIT0	SD/MMC0 COMMAND	
110	SD0_D1/PH2	B	PULL DOWN	GPIO PORT H BIT2	SD/MMC0 DATA BIT1	
111	SD0_D0/PH1	B	PULL DOWN	GPIO PORT H BIT1	SD/MMC0 DATA BIT0	
112	SD0_D3/PH4	B	PULL DOWN	GPIO PORT H BIT4	SD/MMC0 DATA BIT3	
113	SD0_D2/PH3	B	PULL DOWN	GPIO PORT H BIT2	SD/MMC0 DATA BIT1	
114	SD0_CLK/PH5	B	PULL DOWN	GPIO PORT H BIT5	SD/MMC0 CLOCK OUT	
115	VDDA_DSPPLL	P	N/A	DSP PLL ANALOG POWER(1.2V)		
116	VDDA_ARMPLL	P	N/A	ARM PLL ANALOG POWER(1.2V)		
117	VDDA_CODECPLL	P	N/A	AUX PLL ANALOG POWER(1.2V)		
118	XIN24M	I OSC	N/A	CRYSTAL 24MHZ INPUT PIN		
119	XOUT24M	O OSC	N/A	CRYSTAL 24MHZ OUTPUT PIN		
120	PB5/SPI0_CLKT/SD0_D5	B	PULL UP	GPIO PORT B BIT5	SPI MASTER CLOCK	SD/MMC0 DATA BIT5
121	PB7/SPI0_RXD/SD0_D7	B	PULL UP	GPIO PORT B BIT7	SPI MASTER RX DATA	SD/MMC0 DATA BIT7
122	PB6/SPI0_TXD/SD0_D6	B	PULL UP	GPIO PORT B BIT6	SPI MASTER TX DATA	SD/MMC0 DATA BIT6
123	PG0/UART0_RX/SD1_DET	B	PULL DOWN	GPIO PORT G BIT0	UART0 SERIAL DATA IN	SD/MMC1 CARD DETECT
124	PG1/UART0_TX/SD1_WP	B	PULL DOWN	GPIO PORT G BIT1	UART0 SERIAL DATA OUT	SD/MMC1 WRITE PROTECT
125	PB0/SPIO_CS1/SD1_PCA	B	PULL UP	GPIO PORT B BIT0	SPI MASTER CHIP SELECT 1	SD/MMC1 POWER CONTROL
126	I2C0_SCL/PE5	B	PULL UP	I2C0 SCL	GPIO PORT E BIT5	
127	I2C0_SDA/PE4	B	PULL UP	I2C0 SDA	GPIO PORT E BIT4	
128	VDD	P	N/A	CORE POWER (1.2V)		
129	GND	G	N/A	CORE and IO GROUND		
130	VCC	P	N/A	IO POWER (3.3 V)		
131	I2S_SDI	B	PULL DOWN	I2S INPUT DATA	GPIO FOR DSP BIT27	
132	I2S_LRCK	B	PULL DOWN	I2S LRCK OUTPUT	GPIO FOR DSP BIT30	
133	I2S_SDO	O	N/A	I2S OUTPUT DATA	GPIO FOR DSP BIT28	
134	I2S_SCLK	B	PULL DOWN	I2S SERIAL DATA CLOCK	GPIO FOR DSP BIT31	
135	I2S_CLK	O	N/A	I2S MAIN CLOCK OUT	GPIO FOR DSP BIT29	
136	PB3/UART0_RTS	B	PULL UP	GPIO PORT B BIT3	UART0 MODEM RTS OUT	
137	PB2/UART0_CTS	B	PULL UP	GPIO PORT B BIT2	UART0 MODEM CTS IN	
138	PE6/UART1_SIR_IN/I2C1_SDA	B	PULL UP	GPIO PORT E BIT6	UART1 IRDA DATA IN	I2C1 SDA
139	PE7/UART1_SIR_OUT/I2C1_SCL	B	PULL UP	GPIO PORT E BIT7	UART1 IRDA DATA OUT	I2C1 SCL
140	PA1	B	PULL UP	GPIO PORT A BIT1		
141	PA0	B	PULL UP	GPIO PORT A BIT0		
142	PB1/SM_CS1/SD0_PCA	B	PULL UP	GPIO PORT B BIT0	SPI MASTER CHIP SELECT 1	SD/MMC1 POWER CONTROL
143	PH7	B	PULL DOWN	GPIO PORT H BIT7		
144	VDD	P	N/A	CORE POWER (1.2V)		
145	GND	G	N/A	CORE and IO GROUND		
146	VCC	P	N/A	IO POWER (3.3 V)		
147	PH6	B	PULL DOWN	GPIO PORT H BIT6		

148	PE3/SPI_RXD	B	PULL DOWN	GPIO PORT E BIT3	SPI SLAVE RXD	
149	PE2/SPI_SS_IN	B	PULL DOWN	GPIO PORT E BIT2	SPI SLAVE SELECT	
150	PE1/SPI_CLKIN	B	PULL DOWN	GPIO PORT E BIT1	SPI SLAVE CLOCK IN	
151	PF7/SPI_TXD	B	PULL DOWN	GPIO PORT F BIT7	SPI SLAVE TXD	
152	PWM0/PF2	B	PULL DOWN	GPIO PORT F BIT2	PWM0 OUT SIGNAL	
153	PF5/PWM3/DEM_PWM	B	PULL DOWN	GPIO PORT F BIT5	PWM3 OUT SIGNAL	
154	NPOR	I	N/A	POWER ON RESET, LOW ATIVE		
155	PA4	B	PULL UP	GPIO PORT A BIT4		
156	NC	NC				
157	GND	G	N/A	CORE and IO GROUND		
158	GND	G	N/A	CORE and IO GROUND		
159	VDD	P	N/A	CORE POWER (1.2V)		
160	VCC	P	N/A	IO POWER (3.3 V)		
161	PA3	B	PULL UP	GPIO PORT A BIT3		
162	RTCK	O	N/A	JTAG RTCK		
163	TDO	O	N/A	JTAG TDO		
164	TMS	I	PULL UP	JTAG TMS		
165	TDI	I	PULL UP	JTAG TDI		
166	TRST_N	I	PULL DOWN	JTAG TRST		
167	TCK	I	PULL UP	JTAG TCK		
168	VCC	P	N/A	IO POWER (3.3 V)		
169	NC	NC				
170	LCDC_HSYNC	O	N/A	LCDC HORIZONTAL SYNC SIGNAL OUTPUT AND WE SIGNAL FOR MCU PANEL		
171	NC	NC				
172	LCDC_DCLK	O	N/A	LCDC DOT CLOCK OUTAND RS SIGNAL FOR MCU PANEL		
173	GND	G	N/A	CORE and IO GROUND		
174	NC	NC				
175	LCDC_DE	B	PULL DOWN	GPIO2 BIT26	LCDC DATA ENABLE SIGNAL	
176	LCDC_VSYNC	B	PULL DOWN	GPIO2 BIT25	LCDC VERTICAL SYNC SIGNAL OUTPUT AND CS SIGNAL FOR MCU PANEL	

2.3 LQFP176 package outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Fig. 2-1 LQFP176 package outline

Chapter 3 Port Multiplexer

3.1 Overview

Most of IOs have the multiple functions shared by programmable register set. And can also be pulled-up or pulled-down by reconfigurable register. As for the detailed description for these registers, please refer to register IOMUX_A_CON / IOMUX_B_CON / GPIO_AB_PU_CON / GPIO_CD_PU_CON / GPIO_EF_PU_CON / GPIO_GH_PU_CON in Chapter 34.

3.2 Detailed description for IO MUX

The following table shows the detailed multiplexer for all GPIOs.

Table 3-1 RK2729 IO MUX List

PAD NAME	PORT Name	PAD Direction	Pin Description
CPU GPIO A			
IO_GPIO_A[5]	gpio0_a[5]	B Pull Up	gpio
	flash_cs1	O	nand flash cs1
IO_GPIO_A[6]	gpio0_a[6]	B Pull Up	
	flash_cs2	O	nand flash cs2
IO_GPIO_A[7]	gpio0_a[7]	B Pull Up	
	flash_cs3	O	nand flash cs3
CPU GPIO B			
IO_GPIO_B[0]	gpio0_b[0]	B Pull Up	gpio
	spi0_csn1	O	spi0 second chip select
	sdmmc1_pwr_en	O	sdmmc1 power control
IO_GPIO_B[1]	gpio0_b[1]	B Pull Up	gpio
	sm_cs1_n	O	nor flash second chip select
	sdmmc0_pwr_en	O	sdmmc0 power control
IO_GPIO_B[2]	gpio0_b[2]	B Pull Up	gpio
	uart0_cts_n	I	uart0 modem signal
IO_GPIO_B[3]	gpio0_b[3]	B Pull Up	gpio
	uart0_rts_n	O	uart0 modem signal
IO_GPIO_B[4]	gpio0_b[4]	B Pull Up	gpio
	spi0_csn0	O	spi0 first chip select
	sdmmc0_data[4]	B	sdmmc0 data bit4
IO_GPIO_B[5]	gpio0_b[5]	B Pull Up	gpio
	spi0_clkout	O	spi0 clk out
	sdmmc0_data[5]	B	sdmmc0 data bit5
IO_GPIO_B[6]	gpio0_b[6]	B Pull Up	gpio
	spi0_txd	O	spi0 txd
	sdmmc0_data[6]	B	sdmmc0 data bit6
IO_GPIO_B[7]	gpio0_b[7]	B Pull Up	gpio
	spi0_rxd	I	spi0 rxd
	sdmmc0_data[7]	B	sdmmc0 data bit7
CPU GPIO C			
IO_GPIO_C[0]	gpio0_c[0]	B Pull Up	gpio
	lcdc_data16	O	lcdc data bit16
IO_GPIO_C[1]	gpio0_c[1]	B Pull Up	gpio
	lcdc_data17	O	lcdc data bit17

IO_GPIO_C[2]	gpio0_c[2]	B Pull Up	gpio
	lcdc_data18	O	lcdc data bit18
IO_GPIO_C[3]	gpio0_c[3]	B Pull Up	gpio
	lcdc_data19	O	lcdc data bit19
IO_GPIO_C[4]	gpio0_c[4]	B Pull Up	gpio
	lcdc_data20	O	lcdc data bit20
IO_GPIO_C[5]	gpio0_c[5]	B Pull Up	gpio
	lcdc_data21	O	lcdc data bit21
IO_GPIO_C[6]	gpio0_c[6]	B Pull Up	gpio
	lcdc_data22	O	lcdc data bit22
IO_GPIO_C[7]	gpio0_c[7]	B Pull Up	gpio
	lcdc_data23	O	lcdc data bit23
CPU GPIO D			
IO_GPIO_D[0]	gpio0_d[0]	B Pull Up	gpio
	lcdc_data8	O	lcdc data bit8
IO_GPIO_D[1]	gpio0_d[1]	B Pull Up	gpio
	lcdc_data9	O	lcdc data bit9
IO_GPIO_D[2]	gpio0_d[2]	B Pull Up	gpio
	lcdc_data10	O	lcdc data bit10
IO_GPIO_D[3]	gpio0_d[3]	B Pull Up	gpio
	lcdc_data11	O	lcdc data bit11
IO_GPIO_D[4]	gpio0_d[4]	B Pull Up	gpio
	lcdc_data12	O	lcdc data bit12
IO_GPIO_D[5]	gpio0_d[5]	B Pull Up	gpio
	lcdc_data13	O	lcdc data bit13
IO_GPIO_D[6]	gpio0_d[6]	B Pull Up	gpio
	lcdc_data14	O	lcdc data bit14
IO_GPIO_D[7]	gpio0_d[7]	B Pull Up	gpio
	lcdc_data15	O	lcdc data bit15
CPU GPIO E			
IO_GPIO_E[1]	gpio1_a[1]	B Pull Down	gpio
	spi1_clkin	I	spi1 slave mode clock signal
IO_GPIO_E[2]	gpio1_a[2]	B Pull Down	gpio
	spi1_ss_n	I	spi1 slave mode select signal
IO_GPIO_E[3]	gpio1_a[3]	B Pull Down	gpio
	spi1_rxd	I	spi1 rxd
IO_GPIO_E[4]	i2c0_sda	B Pull Up	i2c0 sda
	gpio1_a[4]	B Pull UP	gpio
IO_GPIO_E[5]	i2c0_scl	B Pull UP	i2c0 scl
	gpio1_a[5]	B Pull UP	gpio
IO_GPIO_E[6]	gpio1_a[6]	B Pull UP	gpio
	uart1_sir_in	I	uart1 IR data in
	i2c1_sda	B Pull UP	i2c1 sda
IO_GPIO_E[7]	gpio1_a[7]	B Pull UP	gpio
	uart1_sir_out_n	O	uart1 IR data out
	i2c1_scl	B Pull UP	i2c1 scl
CPU GPIO F			
IO_GPIO_F[0]	gpio1_b[0]	B Pull Down	gpio
	uart1_sin	I	uart1 serial data in
	cx_timer0_pwm	O	pwm out from ceva
IO_GPIO_F[1]	gpio1_b[1]	B Pull Down	gpio
	uart1_sout	O	uart1 serial data out
	cx_timer1_pwm	O	pwm out from ceva

IO_GPIO_F[2]	gpio1_b[2]	B Pull Down	gpio
	pwm0	B	pwm
IO_GPIO_F[3]	gpio1_b[3]	B Pull Down	gpio
	pwm1	B	pwm
	sdmmc0_detect_n	I	sdmmc0 detect signal
IO_GPIO_F[4]	gpio1_b[4]	B Pull Down	gpio
	pwm2	B	pwm
	sdmmc0_write_prt	I	sdmmc0 write protect
IO_GPIO_F[5]	gpio1_b[5]	B Pull Down	gpio
	pwm3	B	pwm
	demod_pwm_out	O	pwm out from demodulator
IO_GPIO_F[6]	gpio1_b[6]	B Pull Down	gpio
	vip_clkout	O	sensor clk out
IO_GPIO_F[7]	gpio1_b[7]	B Pull Down	gpio
	spi1_txd	O	spi1 txd
CPU GPIO G			
IO_GPIO_G[0]	gpio1_c[0]	B Pull Down	gpio
	uart0_sin	I	uart0 serial data in
	sdmmc1_detect_n	I	sdmmc1 card detect
IO_GPIO_G[1]	gpio1_c[1]	B Pull Down	gpio
	uart0_sout	O	uart0 serial data out
	sdmmc1_write_prt	I	sdmmc1 card write protect
IO_GPIO_G[2]	gpio1_c[2]	B Pull Down	gpio
	sdmmc1_cmd	B	sdmmc1 command
IO_GPIO_G[3]	gpio1_c[3]	B Pull Down	gpio
	sdmmc1_data[0]	B	sdmmc1 data bit0
IO_GPIO_G[4]	gpio1_c[4]	B Pull Down	gpio
	sdmmc1_data[1]	B	sdmmc1 data bit1
IO_GPIO_G[5]	gpio1_c[5]	B Pull Down	gpio
	sdmmc1_data[2]	B	sdmmc1 data bit2
IO_GPIO_G[6]	gpio1_c[6]	B Pull Down	gpio
	sdmmc1_data[3]	B	sdmmc1 data bit3
IO_GPIO_G[7]	gpio1_c[7]	B Pull Down	gpio
	sdmmc1_clkout	O	sdmmc1 clk out
CPU GPIO1 D			
IO_GPIO_H[0]	gpio1_d[0]	B Pull Down	gpio
	sdmmc0_cmd	B	sdmmc0 command
IO_GPIO_H[1]	gpio1_d[1]	B Pull Down	gpio
	sdmmc0_data[0]	B	sdmmc0 data bit0
IO_GPIO_H[2]	gpio1_d[2]	B Pull Down	gpio
	sdmmc0_data[1]	B	sdmmc0 data bit1
IO_GPIO_H[3]	gpio1_d[3]	B Pull Down	gpio
	sdmmc0_data[2]	B	sdmmc0 data bit2
IO_GPIO_H[4]	gpio1_d[4]	B Pull Down	gpio
	sdmmc0_data[3]	B	sdmmc0 data bit3
IO_GPIO_H[5]	gpio1_d[5]	B Pull Down	gpio
	sdmmc0_clkout	O	sdmmc0 clock out
IO_GPIO_H[6]	gpio1_d[6]	B Pull Down	gpio
	ext_iq_index	I	ext_iq_index from hs_adc module
IO_GPIO_H[7]	gpio1_d[7]	B Pull Down	gpio
	hsadc_clkin	I	hsadc clock input for aysnc mode

Notes : B --- Bidirectional IO
I --- Input IO
O --- Output IO

3.3 Detailed description for LCD port

Table 3-2 RK2729 LCD port MUX List

PIN NAME	18bit MCU	16bit MCU	24bit RGB	18bit RGB	8bit RGB	CCIR656
LCD_D0	DB0	DB0	B0	B0	D0	D0
LCD_D1	DB1	DB1	B1	B1	D1	D1
LCD_D2	DB2	DB2	B2	B2	D2	D2
LCD_D3	DB3	DB3	B3	B3	D3	D3
LCD_D4	DB4	DB4	B4	B4	D4	D4
LCD_D5	DB5	DB5	B5	B5	D5	D5
LCD_D6	DB6	DB6	B6	G0	D6	D6
LCD_D7	DB7	DB7	B7	G1	D7	D7
LCD_D8	DB8	DB8	G0	G2		
LCD_D9	DB9	DB9	G1	G3		
LCD_D10	DB10	DB10	G2	G4		
LCD_D11	DB11	DB11	G3	G5		
LCD_D12	DB12	DB12	G4	R0		
LCD_D13	DB13	DB13	G5	R1		
LCD_D14	DB14	DB14	G6	R2		
LCD_D15	DB15	DB15	G7	R3		
LCD_D16	DB16		R0	R4		
LCD_D17	DB17		R1	R5		
LCD_D18			R2			
LCD_D19			R3			
LCD_D20			R4			
LCD_D21			R5			
LCD_D22			R6			
LCD_D23			R7			
LCD_VSYNC /MCU_CS	CS	CS	VSYNC	VSYNC	VSYNC	
LCD_HSYNC/ MCU_WR	WR	WR	HSYNC	HSYNC	HSYNC	
LCD_DEN			(DEN)	(DEN)	(DEN)	
LCD_CLK /MCU_RS	RS	RS	DOT_CLK	DOT_CLK	DOT_CLK	DOT_CLK

Chapter 4 Hardware Information

4.1 Oscillator Connection

RK2729 will use one oscillator for input of three on-chip PLLs, or USB OTG PHY, and for I2S main clock, which should be 24MHz. The design for oscillator pad has been optimized for stability and minimum jitter, and characterized to allow a variation of 4pF to 18pF on both XI and XO pins for crystal stability. In the Fig. 39-1, the variation range for C value is 4pF to 18pF.

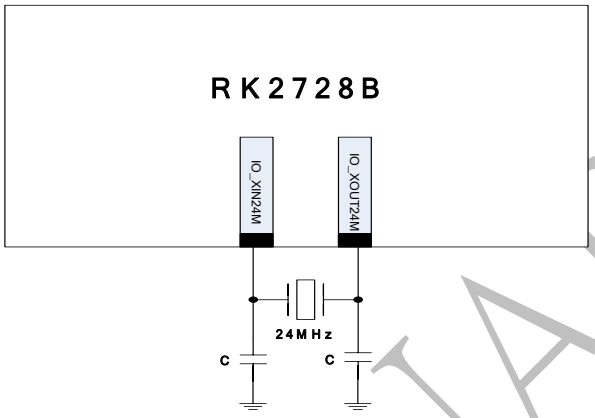


Fig. 4-1 RK2729 external oscillator connection diagram

4.2 USB PHY Connection

USB2.0 OTG PHY is used in RK2729 for USB host, USB device and otg functions. The following figure shows external connection for USB PHY interface.

In the above diagram, some parameters and its viariant will be shown in the following table.

External resistor (REXT)	44.2 Ω (± 1%)
Analog power supplies	3.3 V (+ 10%, – 10%) at the macro pins with respect to VSSA and VSSAC 2.5 V (+ 10%, – 10%) at the macro pins with respect to VSSA and VSSAC
Digital power supply	1.2 V (+ 10%, – 12.5%) at the macro pins with respect to DVSS
Junction temperature	–40º C through +125º C

4.3 Power up Sequence for power supply

For IO and core power supply of RK2729, there are no power sequence requirements, since IO is 3-state when core power is not valid.

4.4 Power on reset Descriptions

The following figure shows power-on-reset sequence and relative clock behavior. When NPOR (power-on-reset) is released after stabilization of oscillator clock XIN 24M. After about T1 timing length, power supply for on-chip PLLs will be in stable state and pll_rstn (internal reset signal for PLL) is released. Then after (T2-T1) timing length, chip_rstn (internal reset signal for chip logic) is released. Then clock for IP module inside chip will be valid. After about 15 clocks, ip_rstn (internal reset signal for all IPs) will be released, which can meet some special requirements for some IPs , “ reset signal will be kept valid no less than 15 clock cycles” .

Notes: T1 is about 5us; T2 is about 139us

Another, RK2729 can filter out 5 clock cycles for low pulse of npor, the clock cycle is xin24m clock, so about 208ns low pulse of npor will not be recognized as valid power-on-reset signal for RK2729.

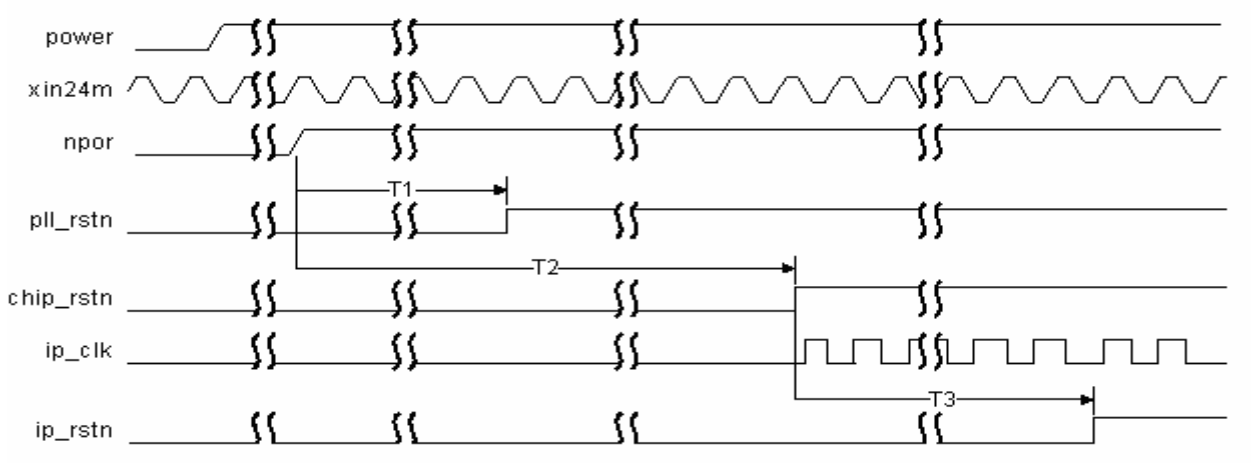


Fig. 4-1 RK2729 reset sequence timing waveform

Chapter 5 Electrical Specification

5.1 Recommended Operating Conditions

TBD

5.2 Electrical Characteristics

TBD