Rockchip RK2106 Datasheet

Revision 1.1
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Revision History

Date	Revision	Description
2019-1-7	1.1	Update the diagram
2018-11-29	1.0	Initial Release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

1.1 Overview

RK2106 is a ARM Cortex-M3 based microcontroller for Wireless Audio, MP3 player and IOT applications.

RK2106 includes two M3 cores , up to 1M Bytes Ram, internal power management unit, high quality audio codec, dedicated hardware MP3 decode accelerator, hardware lossless audio decode accelerator and rich peripheral interface. RK2106 can support Wi-Fi and Bluetooth protocol without external memory, support 24 bits 192k Hz sample rate lossless audio decoding with low power consumption, and support three power modes.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Boot Option

- Boot from eMMC flash
- Boot from SPI Nand/Nor flash
- Boot from USB

1.2.2 Memory Organization

- 16KB boot ROM
- 64KB PMU SRAM for low power sleep mode
- 320KB SYSRAM0 and 256KB SYSRAM1
- 128KB HIGHRAM0 and 256KB HIGHRAM1
- 64KB/bank clock-gate control for reduce power consumption

1.2.3 Processor

- Dual ARM Cortex-M3 core
  - A Thumb instruction set subset
  - Banked Stack Pointer (SP) only
  - Hardware divide instructions, SDIV and UDIV (Thumb 32-bit instructions)
  - Handler and Thread modes
  - Thumb and Debug states
  - Interruptible-continued LDM/STM, PUSH/POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for ARMv6 unaligned accesses
- Nested Vectored Interrupt Controller (NVIC)
  - 32-level priority of interrupt
  - Dynamic reprioritization of interrupts
  - Priority grouping. This enables selection of pre-empting interrupt levelsand non pre-empting interrupt levels
  - Support for tail-chaining and late arrival of interrupts. This enablesback-to-back interrupt processing without the overhead of state saving andrestoration between interrupts
  - Processor state automatically saved on interrupt entry, and restored oninterrupt exit, with no instruction overhead.
- Mail box
  - Support dual-core system: system core and calculation core
  - Support APB interface
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt

- Four interrupts to system core
- Four interrupts to calculation core

1.2.4 Power Management Unit

- Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
- 2 voltage domains and 3 separate power domains, which can be power up/down by software based on different application scenes

1.2.5 CRU (clock & reset unit)

- Support clock gating control for individual components
- One oscillator with 24MHz clock input and 1 embedded general purpose PLL
- Support global soft-reset control for whole SOC, also individual soft-reset for every components

1.2.6 Hardware Accelerator for MP3 decode

- MP3 imdct36 calculation module
- MP3 sub-band synthesize module

1.2.7 Watch Dog

- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period

1.2.8 Memory Interface

- SD/MMC controller
  - SD/MMC SPI mode/1bit mode/4bit mode
  - Support Multi Media Card Specification Version 4.41
  - Support SD Memory Card Specification Version 2.0
  - Cards Clock Rate up to PCLK, Re-scaling the SD/MMC clock (PCLK) with the 8-bits pre-scale register in SCU block
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection

- eMMC Interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - 8bits data bus width

- SFC Interface
  - Support transfer data from/to SPI flash device
  - Support x1,x2,x4 data bits mode
  - Support interrupt output, interrupt maskable
  - Support Spansion, MXIC, Gigadevice vendor's nor flash memory

1.2.9 DISPLAY interface

- Support source data format: RGB565, YUV420
- Support UV swap
- Support YUV2RGB
- Support BT601 limited range
- Support BT709 limited range
- Support BT601 full range
- Support allegro dither down for RGB888 to RGB565
- Support RGB565 display data format
- Support display data swap
- Support max output resolution 400x400
- Built-in i8080 MCU interface

1.2.10 DMA Controller

- Two DMA Controllers in chip
  - DMAC1 Support 6 DMA channels
  - DMAC2 Support 2 DMA channels
  - Support incremental and fixed addressing mode
  - Support hardware and software trigger DMA transfer mode
  - Support error interrupt, transport-complete interrupt
  - When transport data is not align with source burst, the last data will be transported in single burst mode
  - Support LLP mode and auto-reload

1.2.11 USB interface

- USB 2.0 OTG controller and PHY
- Operates in High-Speed and Full-Speed mode
- Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
- Support 6 endpoints, one control endpoint,two IN/OUT endpoints,one IN endpoint
- Support 4 channels at Host mode,support bulk transfer

1.2.12 Low speed Peripheral interface

- I2C controller
  - Support 3 I2C controllers
  - Supports master modes of I2C bus
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support 2 I2S controllers

- Support mono/stereo audio file
- Support16 ~ 32 bits audio data transfer
- Support audio sample rate up to 192 KHz
- Support I2S, Left-Justified and Right-Justified digital serial data format

- PWM
  - 2 PWMs with interrupt-based operation
  - Programmable counter and duty cycle
  - Chained timer for long period purpose
  - Support single counter mode and reload mode
  - Configurable polarity
  - Support interrupt output
- SPI master
  - 2 on-chip SPIs
  - Serial-master operation – Enables serial communication with serial-slave peripheral devices
  - DMA Controller Interface – Enables interface to a DMA controller using a handshaking interface for transfer requests
  - Support interrupt interface to interrupt controller, and independently masking of interrupts
  - One hardware slave-select lines
  - Dynamic control of the serial bit rate of the data transfer
- GPIO
  - 3 groups of GPIO (GPIO0~GPIO2) , 32 GPIOs per group
  - All of GPIOs can be used to generate interrupt to CPU
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset
- Timer
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
- UART
  - 6 on-chip UARTs
  - AMBA APB interface
  - DMA Controller Interface – Enables interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
  - Support interrupt interface to interrupt controller.

1.2.13 Analog IP interface

- AUDIO-CODEC
  - High Digital to Analog Convert SNR.
  - High Analog to Digital Convert SNR.
  - Differential analog input microphone input with boost pre-amplify and low-noise microphone bias.
  - Stereo line input.

- PLL internal.
- Stereo virtual-ground headphone amplifier with ultra low power.
- One 24bit/8k~192K I2S/PCM interface for stereo DAC and ADC.
- ALC (Automatic Level Control) in ADC path and DRC (Dynamic Range control) in DAC path.
- The high-pass filter in ADC path.
- Soft pop noise suppression.

- SAR-ADC(Successive Approximation Register)
  - 2-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL less than1 LSB , INL less than 2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface, power dissipation is less than 900uW

1.3 Block Diagram

The following diagram shows the basic block diagram.

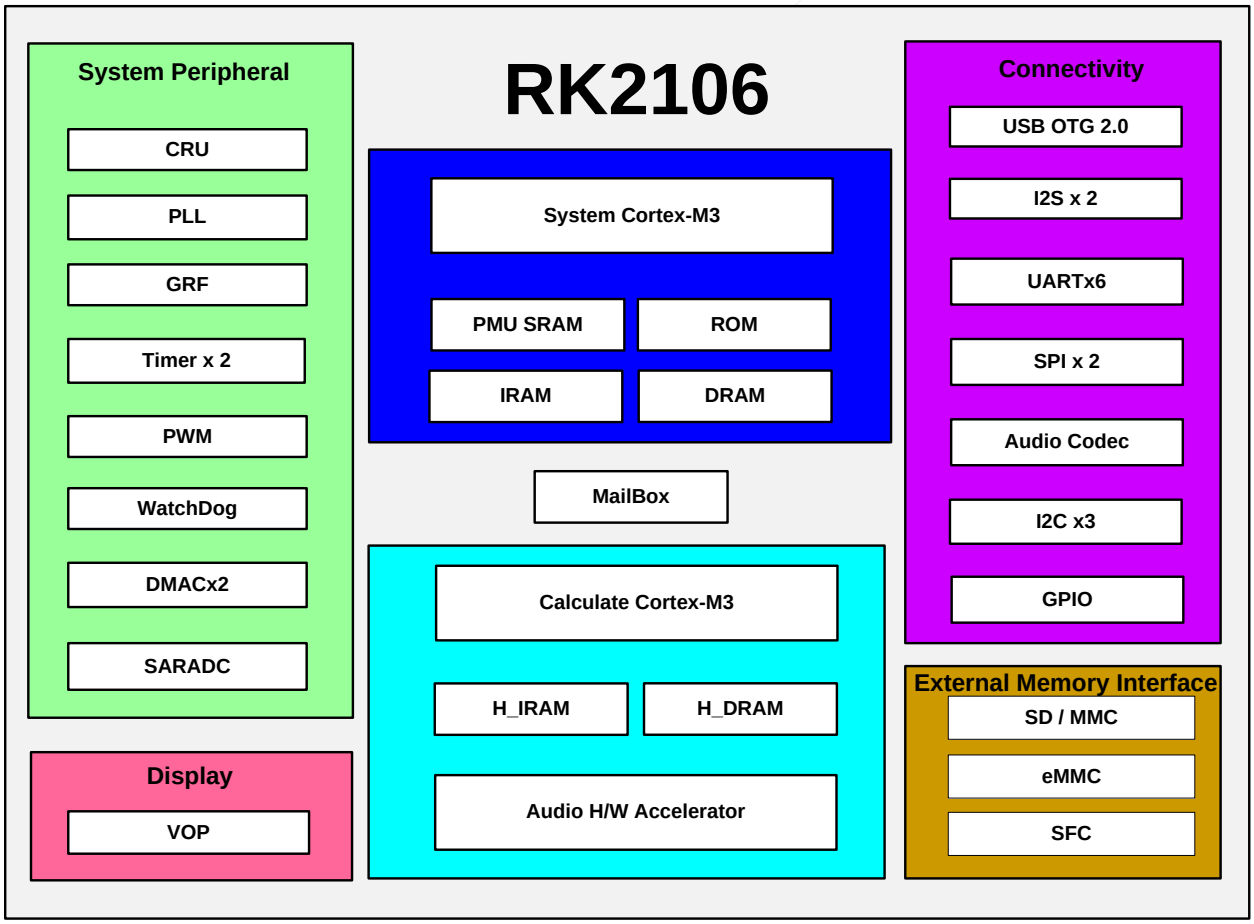


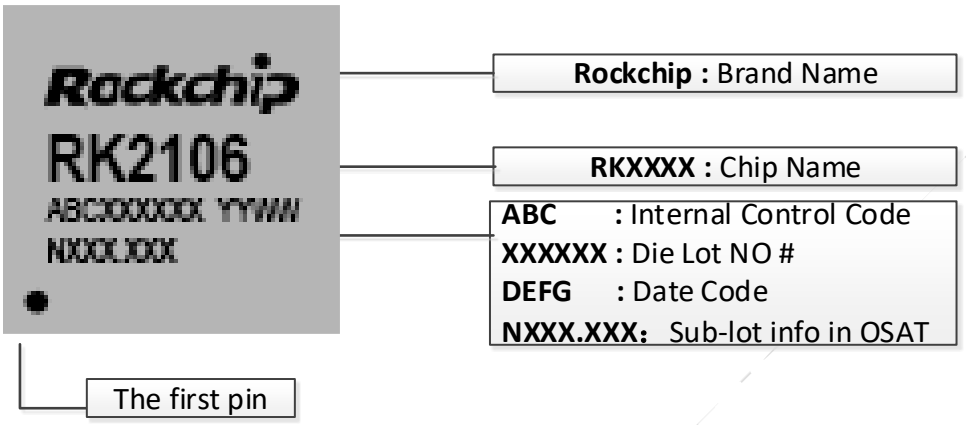
Fig. 1-1 Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RK2106	RoHS	QFN68	2600 by tray	Dual Cortex-M3 embed controller

2.2 Top Marking



2.3 Dimension

2.3.1 QFN68 Package

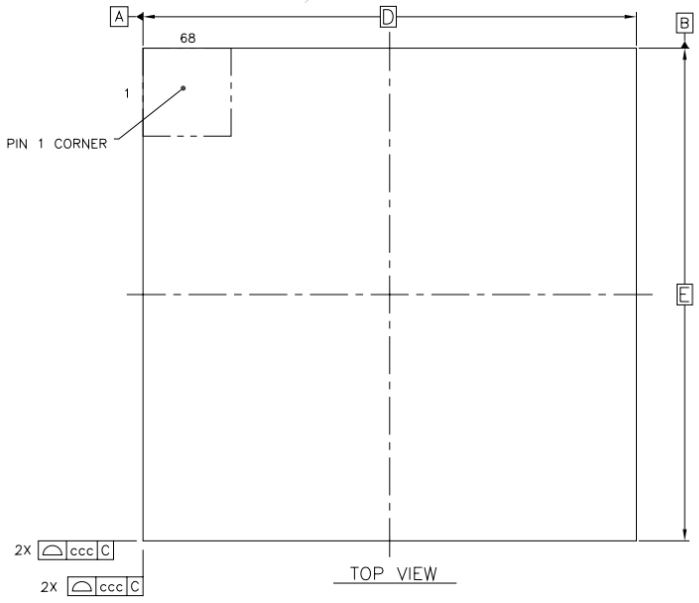


Fig. 2-1 RK2106 QFN68 Package Top View

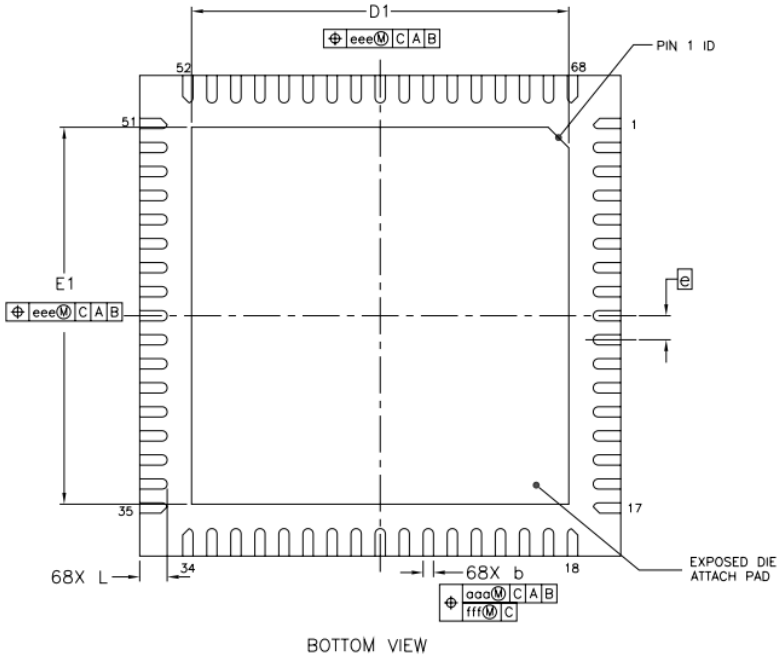


Fig. 2-2 RK2106 QFN68 Package Bottom View

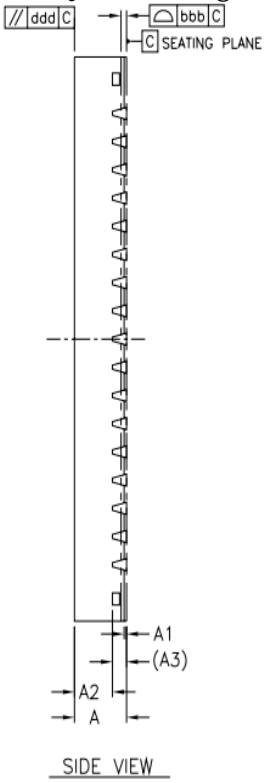


Fig. 2-3 RK2106 QFN68 Package Side View

FOR CUSTOMER ONLY				
PACKAGE TYPE	QFN			
PIN COUNT	68			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	–	0.55	0.57
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	–	7 BSC	–
	E	–	7 BSC	–
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.40	0.50
LEAD PITCH	e	0.35 BSC		
LEAD WIDTH	b	0.10	0.15	0.20
LEAD POSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

Fig. 2-4 RK2106 QFN68 Package Dimension

2.4 RK2106 PIN Description

2.4.1 RK2106 PIN Description

Table 2-1 RK2106 Pin Information

PIN	PIN_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull ②	Pin types ①	Power Domain④
1	I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6	GPIOP2_A6	I2C2C_SDA	JTG0_TRST	POWERHOLD	down	I/O	IO
2	UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1	GPIOP2_C1	UART1A_RX	I2C0B_SCL	SPI1B_TX	up	I/O	IO
3	UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0	GPIOP2_C0	UART1A_TX	I2C0B_SDA	SPI1B_CLK	up	I/O	IO
4	VDD	VDD					DP	
5	XOUT24M	XOUT24M					O	IO
6	XIN24M	XIN24M					I	IO
7	VDD_PLL	VDD_PLL					AP	PLL
8	VCC_PLL	VCC_PLL					AP	PLL
9	VCC	VCC					DP	IO
10	SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5	GPIO1_A5	SDMMC_CMD	SPI1A_CS	UART3_TX	up	I/O	IO
11	SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6	GPIO1_A6	SDMMC_CLK	SPI1A_CLK	UART3_RX	up	I/O	IO
12	SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7	GPIO1_A7	SDMMC_D0	SPI1A_RX	UART4_TX	up	I/O	IO
13	SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0	GPIO1_B0	SDMMC_D1	SPI1A_TX	UART4_RX	up	I/O	IO
14	SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1	GPIO1_B1	SDMMC_D2	I2C1B_SCL	UART5_TX	up	I/O	IO
15	SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2	GPIO1_B2	SDMMC_D3	I2C1B_SDA	UART5_RX	up	I/O	IO
16	VDD	VDD					DP	
17	USB_DM	USB_DM	UART0B_RX				A	USB
18	USB_DP	USB_DP	UART0B_TX				A	USB
19	VBUS	VBUS					I	USB
20	USB_VDD12	USB_VDD12					DP	USB

PIN	PIN_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull ②	Pin types ①	Power Domain ④
21	USB_EXTR	USB_EXTR					I	USB
22	AVDD_IO/USB_VCC33	AVDD_IO	USB_VCC33				AP	USB
23	AVSS_IO	AVSS_IO					AG	USB
24	HPL_OUT	HPL_OUT					A	ACODEC
25	HP_SENSE	HP_SENSE					A	ACODEC
26	HP_VGND	HP_VGND					A	ACODEC
27	HPR_OUT	HPR_OUT					A	ACODEC
28	VREF	VREF					A	ACODEC
29	MICBIAS_L	MICBIAS_L					A	ACODEC
30	MIC1N	MIC1N					A	ACODEC
31	MIC1P	MIC1P					A	ACODEC
32	IN1R	IN1R	MIC2N				A	ACODEC
33	IN1L	IN1L	MIC2P				A	ACODEC
34	AVSS	AVSS					AG	ACODEC
35	AVDD	AVDD					AP	ACODEC
36	ADC0	ADC0					A	IO
37	ADC1	ADC1					A	IO
38	VCC/ADC_VCC33	VCC	ADC_VCC33				DP	IO
39	EMMC_PWREN/I2S1B_CLK/GPIO0_A0	GPIO0_A0	EMMC_PWREN	I2S1B_CLK		down	I/O	IO
40	EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0A1	GPIO0A1	EMMC_CLK	I2S1B_LRCK	UART2C_TX	down	I/O	IO
41	EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2	GPIO0_A2	EMMC_CMD	I2S1B_SCLK	UART2C_RX	up	I/O	IO
42	EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3	GPIO0_A3	EMMC_D0	I2S1B_SDO	UART2C_CTS	up	I/O	IO
43	EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4	GPIO0_A4	EMMC_D1	I2S1B_SDI	UART2C_RTS	up	I/O	IO
44	EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5	GPIO0_A5	EMMC_D2	SFC_D3	I2C0C_SDA	up	I/O	IO
45	EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6	GPIO0_A6	EMMC_D3	SFC_D2	I2C0C_SCL	up	I/O	IO
46	EMMC_D4/SFC_D1/GPIO0_A7	GPIO0_A7	EMMC_D4	SFC_D1		up	I/O	IO
47	EMMC_D5/SFC_D0/JTG1_TDI/GPIO0_B0	GPIO0_B0	EMMC_D5	SFC_D0	JTG1_TDI	up	I/O	IO
48	EMMC_D6/SFC_CLK/JTG1_TDO/GPIO0_B1	GPIO0_B1	EMMC_D6	SFC_CLK	JTG1_TDO	up	I/O	IO
49	EMMC_D7/SFC_CS/JTG1_TRST/GPIO0_B2	GPIO0_B2	EMMC_D7	SFC_CS	JTG1_TRST	up	I/O	IO
50	VDD	VDD					DP	
51	LCD_D0/SPI0A_TX/GPIO0_C0	GPIO0_C0	LCD_D0	SPI0A_TX		up	I/O	IO
52	LCD_D1/SPI0A_RX/GPIO0_C1	GPIO0_C1	LCD_D1	SPI0A_RX		up	I/O	IO
53	LCD_D2/SPI0A_CLK/GPIO0_C2	GPIO0_C2	LCD_D2	SPI0A_CLK		up	I/O	IO
54	LCD_D3/SPI0A_CS/GPIO0_C3	GPIO0_C3	LCD_D3	SPI0A_CS		up	I/O	IO
55	LCD_D4/UART2B_RX/GPIO0_C4	GPIO0_C4	LCD_D4	UART2B_RX		up	I/O	IO
56	LCD_D5/UART2B_TX/GPIO0_C5	GPIO0_C5	LCD_D5	UART2B_TX		up	I/O	IO
57	LCD_D6/UART2B_RTS/GPIO0_C6	GPIO0_C6	LCD_D6	UART2B_RTS		up	I/O	IO
58	LCD_D7/UART2B_CTS/GPIO0_C7	GPIO0_C7	LCD_D7	UART2B_CTS		up	I/O	IO
59	LCD_WRN/I2C2B_SCL/GPIO0_D0	GPIO0_D0	LCD_WRN	I2C2B_SCL		up	I/O	IO
60	LCD_RS/I2C2B_SDA/GPIO0_D1	GPIO0_D1	LCD_RS	I2C2B_SDA		up	I/O	IO
61	VDD	VDD					DP	
62	VCC	VCC					DP	IO
63	UART1A_RTS/JTG0_TMS/SPI1B_CS/GPIOP2_B6	GPIOP2_B6	UART1A_RTS	JTG0_TMS	SPI1B_CS	up	I/O	IO
64	UART1A_CTS/JTG0_TCK/SPI1B_RX/GPIOP2_B7	GPIOP2_B7	UART1A_CTS	JTG0_TCK	SPI1B_RX	up	I/O	IO
65	RESET	RESET					I	IO
66	PWM1/CLK_OBS/EBC_GDPWR1/GPIOP2_A3	GPIOP2_A3	PWM1	CLK_OBS		up	I/O	IO
67	PWM0/JTG0_TDI/PMU_ST2/GPIOP2_A4	GPIOP2_A4	PWM0	JTG0_TDI	PMU_ST2	down	I/O	IO
68	I2C2C_SCL/JTG0_TDO/PMU_ST1/GPIOP2_A5	GPIOP2_A5	I2C2C_SCL	JTG0_TDO	PLAYON	down	I/O	IO
69	GND						DG	

Note:

①:Pintypes: I = input, O = output, I/O = input/output (bidirectional),
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
②: The pull up/pull down can be disabled.
③:POWERHOLD and PLAYON are defined by software.
④: Power domain
IO: power supply for system and logic
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core

2.5 RK2106 Power/ground IO descriptions

Table 2-2 RK2106 Power/Ground IO information

Pin Name	Pin Number	Descriptions
VDD	4,16,50,61	Internal core Power
VCC	9,38,62	Digital IO Power Supply
VDD_PLL	7	PLL Analog Power Supply
VCC_PLL	8	PLL Analog Power Supply
USB_VDD12	20	USB Analog Power Supply
AVDD_IO/USB_VCC33	22	Codec and USB Analog Power Supply
AVSS_IO	23	Codec and USB Analog Ground
AVDD	35	Codec Analog Power Supply
AVSS	34	Codec and USB Analog Ground
GND	69	Digital Ground

2.6 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-3 RK2106 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	RESET	I	Chip hardware reset
	CLK_OBS	O	Clock select output

Interface	Pin Name	Direction	Description
JTAG0	JTG0_TRST	I	JTAG0 interface reset input
	JTG0_TCK	I	JTAG0 interface clock input/SWD interface clock input
	JTG0_TDI	I	JTAG0 interface TDI input
	JTG0_TMS	I/O	JTAG0 interface TMS input/SWD interface data out
	JTG0_TDO	O	JTAG0 interface TDO output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	emmcflash clock.
	EMMC_CMD	I/O	emmcflash command output and response input.
	EMMC_Di (i=0~7)	I/O	emmcflash data input and output.
	EMMC_PWREN	O	emmcflash power-enable control signal
	EMMC_RSTN	O	emmcflash reset signal

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC_CLK	O	sdmmc card clock.
	SDMMC_CMD	I/O	sdmmc card command output and responseinput.
	SDMMC_Di (i=0~3)	I/O	sdmmc card data input and output.

Interface	Pin Name	Direction	Description
SFC Host Controller	SFC_CS	O	Serial flash chip select
	SFC_CLK	O	Serial flash clock output
	SFC_Di (i=0~3)	I/O	Serial flash data input/output

Interface	Pin Name	Direction	Description
LCDC	LCD_Di (i=0~7)	O	LCDC i8080 interface data output
	LCD_WRN	O	LCDC i8080 interface write enable
	LCD_RS	O	LCDC i8080 interface command/data signal

Interface	Pin Name	Direction	Description
SPI Interface	SPI0A_CLK	I/O	Spi0 port A serial clock
	SPI0A_CS	I/O	spi0 port A chip select signal,low active
	SPI0A_TX	O	spi0 port A serial data output
	SPI0A_RX	I	spi0 port A serial data input
	SPI1A_CLK	I/O	Spi1 port A serial clock
	SPI1A_CS	I/O	Spi1 port A chip select signal,low active
	SPI1A_TX	O	Spi1 port A serial data output
	SPI1A_RX	I	Spi1 port A serial data input
	SPI1B_CLK	I/O	Spi1 port B serial clock
	SPI1B_CS	I/O	Spi1 port B chip select signal, low active
	SPI1B_TX	O	Spi1 port B serial data output
	SPI1B_RX	I	Spi1 port B serial data input

Interface	Pin Name	Direction	Description
I2C master	I2C0B_SDA	I/O	I2C0 port B_ data
	I2C0B_SCL	O	I2C0 portBclock
	I2C0C_SDA	I/O	I2C0 port C_ data
	I2C0C_SCL	O	I2C0 portCclock
	I2C1B_SDA	I/O	I2C1 port B_ data
	I2C1B_SCL	O	I2C1 portBclock
	I2C2B_SDA	I/O	I2C2 port B_ data
	I2C2B_SCL	O	I2C2 portBclock

Interface	Pin Name	Direction	Description
UART	UART0B_RX	I	UART0 port Bserial data input
	UART0B_TX	O	UART0 port B serial data output
	UART1A_RX	I	UART1 port Aserial data input
	UART1A_TX	O	UART1 port A serial data output
	UART1A_CTS	O	UART1 port A clear to send
	UART1A_RTS	I	UART1 port A request to send
	UART2B_RX	I	UART2 port Bserial data input
	UART2B_TX	O	UART2 port B serial data output
	UART2B_CTS	O	UART2 port C clear to send
	UART2B_RTS	I	UART2 port C request to send
	UART2C_RX	I	UART2 port Cserial data input
	UART2C_TX	O	UART2 port C serial data output
	UART2C_CTS	O	UART2 port C clear to send
	UART2C_RTS	I	UART2 port C request to send
	UART3_RX	I	UART3serial data input
	UART3_TX	O	UART3 serial data output
	UART4_RX	I	UART4serial data input
	UART4_TX	O	UART4 serial data output
	UART5_RX	I	UART5serial data input
	UART5_TX	O	UART5 serial data output

Interface	Pin Name	Direction	Description
I2S Controller	I2S1B_CLK	O	I2S1port B clock source
	I2S1B_SCLK	I/O	I2S1port B serial clock
	I2S1B_LRCK	I/O	I2S1port B left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1B_SDI	I	I2S1port B serial data input
	I2S1B_SDO	O	I2S1port B serial data output

Interface	Pin Name	Direction	Description
PWM	PWM1	O	Pulse Width Modulation output
	PWM0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
SAR-ADC	ADC [i] (i=0~1)	I	SAR-ADC input signal

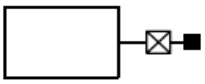
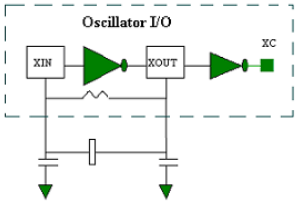
Interface	Pin Name	Direction	Description
ACODEC	HP_SENSE	I	The HP ground signal sense pin
	HPL_OUT	O	The HP left channel output pin
	HP_VGND	O	The HP virtual ground pin
	HPR_OUT	O	The HP right channel output pin
	VREF	O	The Codec IP reference voltage pin, should connect 1uf cap for stable
	MICBIAS_L	O	The Mic-phone left channel bias voltage pin
	MIC1P	I	The Mic-phone 1 differential input plus pin
	MIC1N	I	The Mic-phone 1 differential input minus pin
	IN1L	I	The Line-in 1 left channel input pin
	MIC2N	I	The Mic-phone 2 differential input minus pin
	MIC2P	I	The Mic-phone 2 differential input plus pin
	IN1R	I	The Line-in 1 right channel input pin

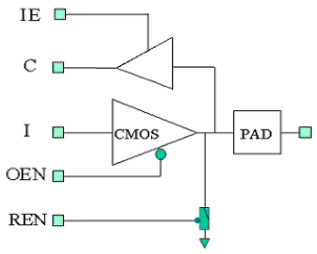
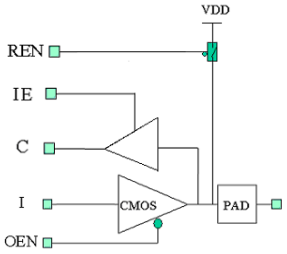
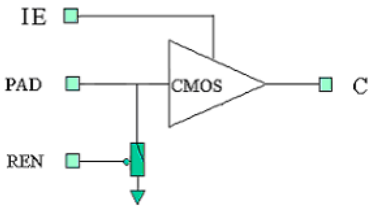
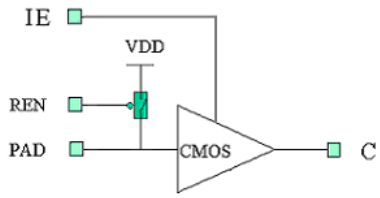
Interface	Pin Name	Direction	Description
USB OTG 2.0	USB_DM	I/O	USB OTG 2.0 Data signal DM
	USB_EXTR	N/A	Reference external resistance
	USB_DP	I/O	USB OTG 2.0 Data signal DP
	VBUS	N/A	USB OTG 2.0 5V power supply pin

2.7 IO Type

The following list shows IO type except Power/Ground IO.

Table 2-4 RK2106 IO Type List

Type	Diagram	Description	Pin Name
A		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
B		Crystal Oscillator with internal register	XIN24M/XOUT24M

Type	Diagram	Description	Pin Name
C		CMOS 3-state output pad with controllable input and controllable pull-down	Part of digital GPIO (PBCDxRN)
D		CMOS 3-state output pad with controllable input and controllable pull-up	Part of digital GPIO (PBCUxRN)
E		controllable input pad with controllable pull-down	Part of digital GPIO (PICDRN)
F		controllable input pad with controllable pull-up	Part of digital GPIO (PICURN)

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK2106 absolute maximum ratings

Parameters	Min	Max①	Unit
DC supply voltage for Internal digital logic	-0.3	1.32	V
DC supply voltage for Digital GPIO(except for SAR-ADC, PLL, USB)	-0.3	3.6	V
DC supply voltage for Analog part of SAR-ADC	-0.3	3.6	V
DC supply voltage for Analog part of PLL	-0.3	3.63	V
DC supply voltage for Analog part of USB OTG	-0.3	3.63	V
Analog Input voltage for SAR-ADC	-0.3	2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG	-0.3	5	V
Digital input voltage for input buffer of GPIO	-0.3	3.6	V
Digital output voltage for output buffer of GPIO	-0.3	3.6	V
Storage Temperature	-40	125	℃
Max Junction Temperature	N/A	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 3-2 RK2106 recommended operating conditions①

Parameters	Min	Typ	Max	Units
Internal digital logic Power	1.08	1.2	1.32	V
Digital GPIO Power(3.3V)	2.97	3.3	3.6	V
Digital GPIO Power(1.8V)	1.62	1.8	1.98	V
PLL Analog Power	1.35	3.3	3.63	V
PLL Analog Power	1.08	1.2	1.32	V
SAR-ADC Analog Power	2.97	3.3	3.63	V
SAR-ADC external reference Power	0.2* SAR_AVDD33		0.9* SAR_AVDD33	
USB OTG Analog Power(3.3V)	2.97	3.3	3.63	V
USB OTG external resistor	40.5	45	49.5	Ohm
Acodec Analog Power	2.97	3.3	3.63	V
PLL input clock frequency	N/A	24	N/A	MHz
Ambient Operating Temperature ②	-10	25	85	℃

Note:

① Recommended operating conditions update with real test after chip arrived.

② with the reference software setup, the reference software will limit the chipset temperature about 85℃

3.3 DC Characteristics

Table 3-3 RK2106 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol	N/A	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	N/A	V
	Pull-up Resistor	Rpu	33	41	62	Kohm
	Pull-down Resistor	Rpd	33	42	68	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	0.63	V
	Input High Voltage	Vih	1.17	1.8	2.1	V
	Output Low Voltage	Vol	N/A	0	0.45	V
	Output High Voltage	Voh	1.35	1.8	N/A	V
	Pull-up Resistor	Rpu	67	93	152	Kohm
	Pull-down Resistor	Rpd	64	92	170	Kohm
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V

3.4 Electrical Characteristics for General IO

Table 3-4 RK2106 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Il	Vin = 3.3V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-10	N/A	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	-10	N/A	10	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RK2106 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input clock frequency	Fin	Fin = FREF @3.3V/1.2V①	1/10	24	800	MHz
Comparison frequency	Fref	FREF = Fin/REFDIV @3.3V/1.2V	1	N/A	40	MHz
VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.2V	400	N/A	1600	MHz

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.2V	1	N/A	1600	MHz
Lock time②	Tlt	@ 3.3V/1.2V, FREF=24M,REFDIV=1	N/A	41.7	62.5	us
VDDHV Power consumption ③ (normal mode)	N/A	Fvco = 1000MHz, @3.3V, 25 ℃	N/A	1	1.2	mA
VDD Power consumption (normal mode)	N/A	@3.3V/1.2V, 25 ℃	N/A	3	4	uW/MHz
Power consumption (power-down mode)	N/A	PD=HIGH, @27 ℃	N/A	10	N/A	uA

Notes :

① REFDIV is the input divider value; FBDIV is the feedback div POSTDIV is the output divider value ider value;

② Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.

③ Current scale as (Fvco/1GHz)1.5

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 RK2106 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Input Range	CH[2:0]	3-channel single-ended input	0.01*SAR_AVDD33	N/A	0.99*SAR_AVDD33	V
Input Capacitance	CIN		N/A	1	N/A	pF
Sampling Clock			N/A	N/A	200	KHz
Main Clock Frequency	CLK		N/A	N/A	2.2	MHz
Data Latency			N/A	10	N/A	Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=10K Fin=99K	N/A	61.49 60.58	N/A	dB
Spurious-Free Dynamic Range	SFDR	Fin=10K Fin=99K	N/A	66.29 67.14	N/A	dB
Second-Harmonic Distortion	2HD	Fin=10K Fin=99K	N/A	-72.64 -69.94	N/A	dB
Third-Harmonic Distortion	3HD	Fin=10K Fin=99K	N/A	-74.79 -68.85	N/A	dB
Effective Number of Bits	ENOB	Fin=10K Fin=99K	N/A	9.92 9.77	N/A	Bits
Positive Reference	VREF		0.5*SARADC_AVDD33		0.99*SARADC_AVDD33	V
Analog Supply Current(SARADC_VDDA)			N/A	278	N/A	uA
Digital Supply Current			N/A	10	N/A	uA
Reference Supply Current			N/A	55	N/A	uA

3.7 Electrical Characteristics for USB Interface

Table 3-7 RK2106 Electrical Characteristics for USB Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit,(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33	USB_AVDD33 = 3.3V USB_DVDD12 = 1.2V	N/A	N/A	0.1	mA
	Current From USB_DVDD12		N/A	N/A	20	mA
Classic mode active(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33		N/A	N/A	0.5	mA
	Current From USB_DVDD12		N/A	N/A	0.5	mA
HS mode(CL=10pF) Active supply current	Current From USB_AVDD33		N/A	0.1	N/A	mA
	Current From USB_DVDD12		N/A	2.22	N/A	mA
FS transmit,(CL=50pF) Active supply current	Current From USB_AVDD33		N/A	10	30	mA
	Current From USB_DVDD12		N/A	5	10	mA
LS transmit(CL=50 to 350pF) Active supply current	Current From USB_AVDD33		N/A	2	25	mA
	Current From USB_DVDD12		N/A	2	5	mA
Suspend mode	Current From USB_AVDD33		N/A	N/A	50	uA
	Current From USB_DVDD12		N/A	N/A	5	uA

3.8 Electrical Characteristics for Audio Codec Interface

Table 3-8 RK2106 Electrical Characteristics for Audio Codec Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Full Scale Input Voltage Line Input	N/A		1N/A	1	N/A	Vpeak
Full Scale Input Voltage Mic Input (signal)	N/A		N/A	1	N/A	Vpeak
Full Scale Input Voltage Mic Input (differential)	N/A		N/A	1	N/A	Vpeak
Full Scale Output Voltage HP (for 32ohm Loading)	N/A		N/A	1	N/A	Vpeak
Full Scale Output Voltage HP (for 16ohm Loading)	N/A		N/A	1	N/A	Vpeak
S/N Ratio Stereo DAC to HP with 10k/32/16 ohm loading	N/A	With A-weight Filter	N/A	100	N/A	dB
S/N Ratio Line in to Stereo ADC	N/A	With A-weight Filter	N/A	90	N/A	dB
S/N Ratio Mic in to Stereo ADC with 0db gain (single end)	N/A	With A-weight Filter	N/A	90	N/A	dB
S/N Ratio Mic in to Stereo ADC with 0db signal (differential end)	N/A	With A-weight Filter	N/A	90	N/A	dB
Total Harmonic Distortion + Noise Stereo DAC to HP（32ohm loading）	N/A		N/A	67	N/A	dB
Total Harmonic Distortion + Noise Line in to Stereo ADC	N/A		N/A	72	N/A	dB
Total Harmonic Distortion + Noise Mic to Stereo ADC with 0db gain (differential or single end)	N/A		N/A	72	N/A	dB
MicBias Output Voltage	N/A		1.5	N/A	AVDD	V
MicBias Drive Current	N/A		N/A	3	N/A	mA

