

Rockchip

RK1608

Datasheet

Revision 1.7
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Revision History

Date	Revision	Description
2020-06-08	1.7	<ul style="list-style-type: none">● Remove RK1608A and add RK1608A1 & RK1608A2
2017-06-22	1.6	<ul style="list-style-type: none">● Update clock jitter requirements
2017-06-06	1.5	<ul style="list-style-type: none">● Update power-up sequence
2017-04-19	1.4	<ul style="list-style-type: none">● Add input clock requirements
2017-02-14	1.3	<ul style="list-style-type: none">● Update Mark definition● Add power description in chapter 5
2016-12-05	1.2	<ul style="list-style-type: none">● Add description for PLL_AVDD_1V8 in section 3.2● Updated DC characteristics for GPIO and LPDDR2● Updated Section 3.1 "Absolute Ratings"
2016-11-14	1.1	<ul style="list-style-type: none">● Add power sequence description
2016-10-14	1.0	<ul style="list-style-type: none">● Initial released

Table of Content

Table of Content	3
Figure Index	4
Table Index	5
Warranty Disclaimer.....	6
Chapter 1 Introduction	7
1.1 Overview	7
1.2 Features	7
1.3 Block Diagram	11
Chapter 2 Package information	12
2.1 Ordering information	12
2.2 Top Marking.....	12
2.3 Dimension.....	13
2.4 Ball Map.....	15
2.5 Ball Pin Number Order	16
2.6 Power/ground IO descriptions	16
2.7 Function IO description	17
2.8 IO pin name descriptions.....	17
2.9 IO Type.....	19
Chapter 3 Electrical Specification	20
3.1 Absolute Ratings	20
3.2 Recommended Operating Conditions	20
3.3 DC Characteristics.....	21
3.4 Electrical Characteristics for General IO	22
3.5 Electrical Characteristics for PLL	22
3.6 Input Clock Requirements.....	22
3.7 Electrical Characteristics for MIPI PHY	23
3.8 Recommended Power Sequence	23
3.9 SPI0 Timing Diagram	24
3.10 I ² C Timing Diagram	26
Chapter 4 Thermal Management	27
4.1 Overview	27
4.2 Package Thermal Characteristics.....	27
Chapter 5 Power Consumption	28
5.1 Overview	28
5.2 Details.....	28

Figure Index

Fig 2-1 Top Markin13
Fig 2-2 Package Top View13
Fig 2-3 Package Bottom View13
Fig 2-4 Ball Mapping Diagram.....15
Fig 3-1 power sequence.....23
Fig 3-2 SPI timing after power up24
Fig 3-3 SPI controller timing diagram in master mode.....24
Fig 3-4 SPI controller timing diagram in slave mode25
Fig 3-5 I²C timing diagram.....26

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Table Index

Table 2-1 Ordering information12

Table 2-2 Package Dimension14

Table 2-3 Ball Pin Number Order Information.....16

Table 2-5 IO function description list17

Table 2-6 IO Type List19

Table 3-1 Absolute maximum ratings.....20

Table 3-2 Recommended operating conditions.....20

Table 3-3 DC Characteristics.....21

Table 3-4 Electrical Characteristics for Digital General IO22

Table 3-5 Electrical Characteristics for PLL.....22

Table 3-6 Electrical Characteristics for MIPI PHY23

Table 3-7 Timing parameter description-125

Table 3-8 Timing parameter description-225

Table 3-9 I²C timing parameters26

Table 4-1 Thermal Resistance Characteristics.....27

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Chapter 1 Introduction

1.1 Overview

RK1608 is a low-power, high performance DSP based SoC for vision processing applications. Which can be applied for 3DNR, EIS, HDR etc. in Smart Phone. There are 4 model available RK1608B, RK1608B2, RK1608A1, RK1608A2, mainly different with capacity of embedded DRAM.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third-party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 DSP core

- Dual-core DSP
- 2 separate power domains for system to support internal power switch and externally turn on/off based on different application scenario
 - PD_DSP0: DSP0 + L1 I Cache, I/D-TCM
 - PD_DSP1: DSP1 + L1 I Cache, I/D-TCM

1.2.2 Memory Organization

- Internal on-chip memory
 - Boot Rom
 - SRAM
 - LPDDR2

1.2.3 Internal Memory

- Internal Boot Rom
 - Support system boot from the following device:
 - ◆ SPI NOR flash
 - ◆ SPI slave interface
- Internal SRAM
 - Size: 8KB
- Internal DRAM
 - RK1608B: LPDDR2-1066, 2Gb KGD
 - RK1608B2: LPDDR2-1066, 2Gb KGD
 - RK1608A1: LPDDR2-1066, 1Gb KGD
 - RK1608A2: LPDDR2-1066, 1Gb KGD

1.2.4 System Component

- CRU (clock & reset unit)
 - Support clock gating control for individual components
 - One oscillator is for clock input and 2 embedded PLLs
 - Support global soft-reset control for whole SoC, also individual soft-reset for every component
- PMU (power management unit)
 - Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
 - Lots of wakeup sources in different mode
 - 2 separate voltage domains

- 2 separate power domains for two DSP cores, which can be powered up/down by software based on different application scenes
- Bus Architecture
 - 128-bit/64-bit/32-bit AXI/AHB/APB composite bus architecture
 - 1 embedded AXI interconnect
 - For the interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
 - Flexible different QoS solution to improve the utility of bus bandwidth
- Interrupt Controller
 - Support 3 interrupt controllers for two DSPs and AP
 - Support 64 SPI interrupt sources input from different components
 - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMA Controller
 - Support AMBA 2.0 AHB slave interface for accessing internal registers and LUT memories, 32bit data bus width
 - Support AMBA 3.0 AXI master read interface for loading frame data
 - There is a high-level indicated interrupt signal for each channel
 - DMA channels are based on chain table
 - Support 2-D transmission, 3 type of DMA operation mode:
 - ◆ Normal mode, the data is being transferred without change
 - ◆ 10-bit compact RAW mode: data from RAW10 will be reordered to be continuous 10-bit data, each pixel will only occupy 10 bits storage space in memory
 - ◆ 10-bit redundant RAW mode: data from RAW10 will be reordered to be continuous 10 bits data, each pixel will only occupy 16 bits storage space in memory, the upper 6 bits or the little 6 bits will be padding with 0
 - Target address alignment:
 - ◆ Normal mode, byte alignment is supported
 - ◆ 10-bit compact RAW mode: destination address may be byte alignment; source address need to be 2-byte alignment
 - ◆ 10-bit redundant RAW mode: destination address need to be 2-byte alignment, source address may be byte alignment and the valid data may be configured from bit 0/2/4/6 in the 16 bits storage unit
 - Only support software program it, not from peripheral
- Timer
 - One 64-bit Timer in SoC with interrupt-based operation for application
 - Provide two operation modes: free-running and user-defined count
 - Support timer work state checkable
- MailBox
 - One MailBox in SoC to serve communication between two DSP cores or between DSP core and AP
 - Support four elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
 - Provide 32 lock registers for software to use to indicate whether mailbox is occupied

1.2.5 Video IN/OUT

- VIP (Video Input Processor)
 - Support sampling image RAW data and PDAF data
 - Support raw 8/10 bit
 - Support reordering the sampling data or not reordering

- Support 1/4、1/16、1/64、1/256 scaling in the gray domain and RGB domain
- Support combined interrupt output
- Support ping-pong mode
- Support virtual line
- Support debug mode
- VOP (Video Output Processor)
 - Display interface
 - ◆ Parallel RGB Interface
 - ◇ RAW8/10
 - ◆ Parallel PDAF Interface
 - ◇ RAW8/10
 - ◆ Support IDI interface
 - Layer process
 - ◆ Background layer
 - ◇ programmable RAW10 data
 - ◆ Win layer – win0
 - ◇ Support data format
 - RAW8/RAW10
 - ◇ Support virtual display
 - ◇ Support display offset
 - ◇ Master Address 64-bit aligned
 - ◇ Stride 64-bit aligned
 - Bus interface
 - ◆ Support AMBA 2.0 AHB slave interface for accessing internal registers and LUT memories, 32bit data bus width
 - ◆ Support AMBA 3.0 AXI master read interface for loading frame data
 - ◆ 64-bit data bus width
 - ◆ Support NOC hurry for higher bus priority for win0
 - ◆ Support bypass path from Rx to Tx

1.2.6 MIPI CSI-2 Transmitter Controller

CSI-2 Transmitter Features

- Compliant with MIPI CSI-2 v1.3 specification
- CSI2 TX lane configuration: Programmable 1, 2 or 4 Data Lane Configuration
- Operate in continuous clock mode
- Supported YUV Data Types: YUV420_8bit, YUV420_10bit, YUV422_8Bit, YUV422_10bit, YUV420_8Bit_CSPS, YUV420_10bit_CSPS and LEGACYYUV420_8bit
- Supported RGB Data Types: RGB888, RGB565, RGB666, RGB555, and RGB444
- Supported RAW Data Types: RAW8, RAW10
- Supported User defined (8-bit) Data Types
- Camera Interface: 8, 16 and 24 bit per pixel
- Data rate: CSI-2 with DPHY: up to 1.5Gbps per lane
- Supports VC interleaving

1.2.7 MIPI CSI-2 Receiver Controller

- The CSI-2 Host Controller implements the CSI-2 protocol on the host side
- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Support Frame formats
 - General Frame or Digital Interlaced Video with or without accurate sync timing
 - Data Type (Packet or Frame Level) and Virtual Channel interleaving

- Support data formats
 - RGB, YUV, and RAW color space definitions
 - From 24-bit down to 6-bit per pixel
 - Generic or user-defined byte-based data types
- Error detection and correction

1.2.8 MIPI D-PHY

- Compliant with the MIPI D-PHY interface specification, revision 1.1
- There are totally 5 MIPI D-PHY for RK1608B
- Flexible input clock reference – 5MHz to 500MHz
- 50% DDR output clock duty-cycle
- Embedded 1 MIPI_CSI TX PHY
 - Support 4 data lanes in this PHY
 - Providing up to 1.5Gbps data rate per lane
- Embedded 3 MIPI_CSI RX PHY
 - Support 4 data lanes per RX PHY
 - Providing up to 1.5Gbps data rate per lane
- Embedded 1 MIPI_CSI TX and RX Combo PHY
 - The PHY can be configured as TX or RX. TX and RX could not work concurrently.
 - Support 4 data lanes in this PHY
 - Providing up to 1.5Gbps data rate per lane

1.2.9 Connectivity

- SPI Controller
 - One on-chip SPI controller
 - Support serial-master and serial-slave mode, software-configurable
 - DMA-based or interrupt-based operation
 - Embedded two 32x16bits FIFO for TX and RX operation respectively
 - Support 1 chip-select output in serial-master mode
- UART Controller
 - 1 on-chip UART interface
 - DMA-based or interrupt-based operation
 - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
 - Support 5bit,6bit,7bit,8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity
 - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
 - Support non-integer clock divides for baud clock generation
 - Auto flow control mode is for all UART, except UART_DBG
- I²C interface
 - Compliant with I²C bus Specification, Version 3.0. But high-speed mode is not supported.
 - Data on the I²C-bus can be transferred at rates of up to 100 kbps in the Standard-mode, up to 400 kbps in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus mode
 - Four I²C master controllers and one I²C slave controller
 - Support 7-bit and 10-bit address mode
 - Software programmable clock frequency and transfer rate
- GPIO
 - All of GPIOs can be used to generate interrupt to DSP
 - The pull direction (pullup or pulldown) for all of GPIOs are software-programmable
 - All of GPIOs are always in input direction in default after power-on-reset

- The drive strength for all of GPIOs is software-programmable

Notes:

- ① Actual maximum frame rate will depend on the clock frequency and system bus performance
- ② Actual maximum data rate will depend on the clock frequency

1.3 Block Diagram

The following diagram shows the basic block diagram.

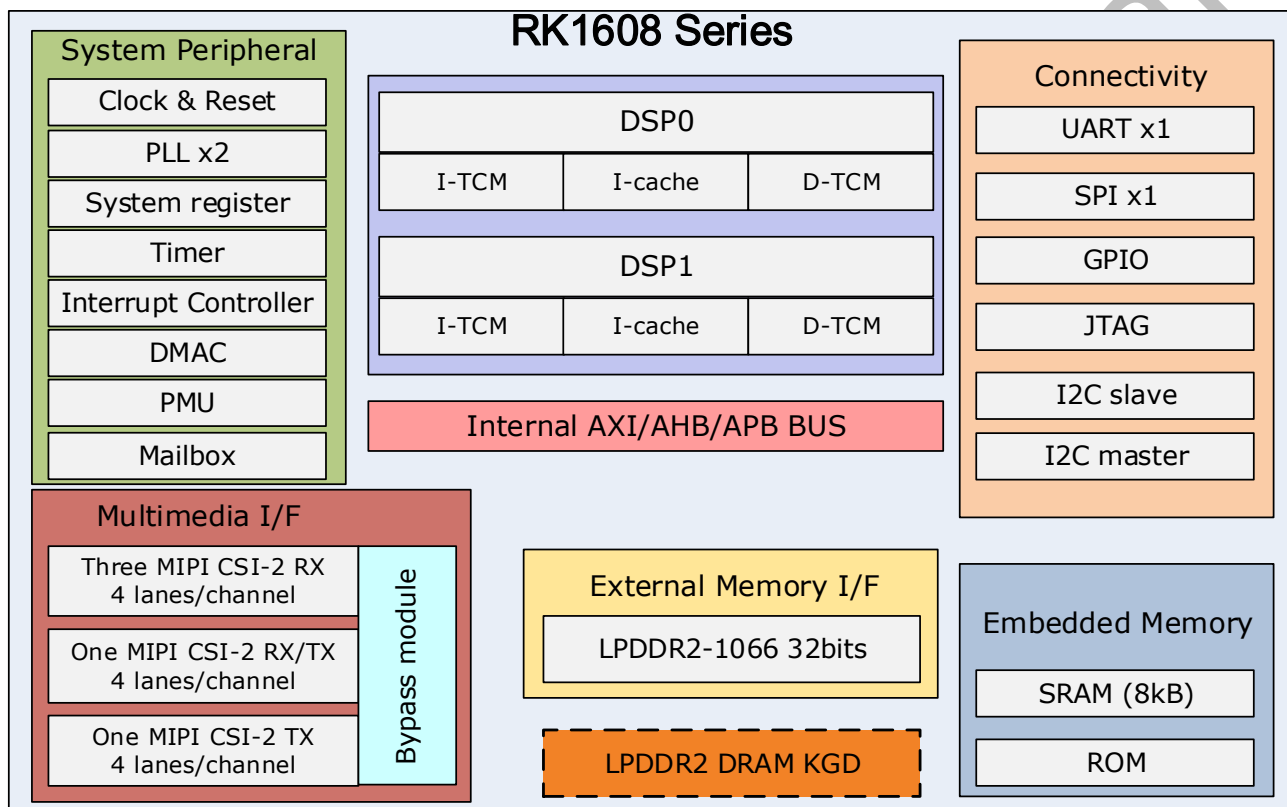


Fig 1-2 Block Diagram

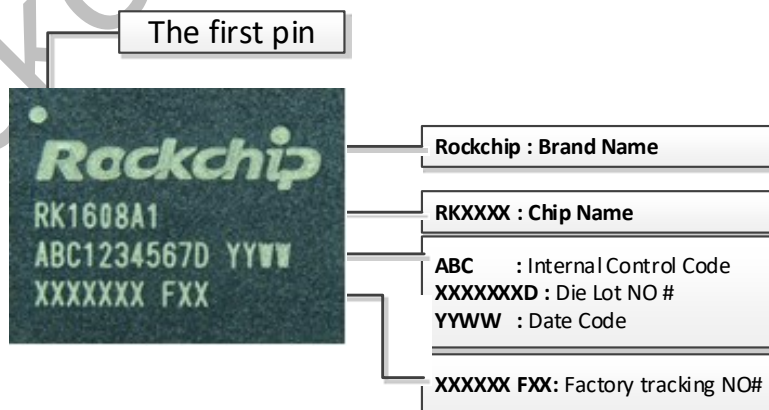
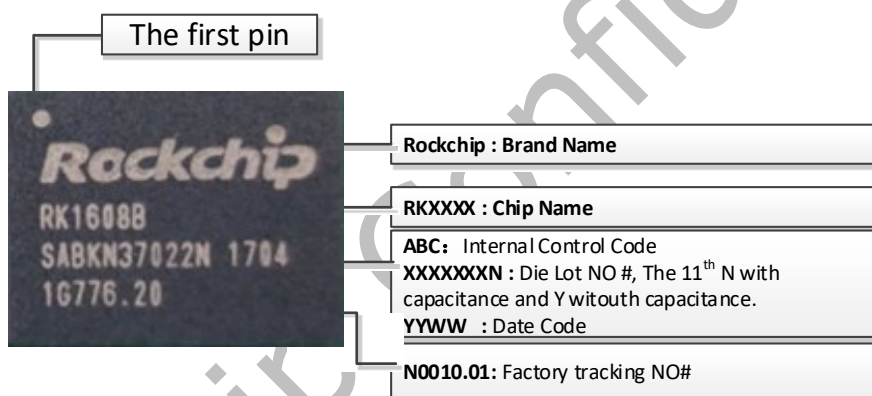
Chapter 2 Package information

2.1 Ordering information

Table 2-1 Ordering information

Orderable Device	RoHS status	Package	Package QTY	Device special feature	Status
RK1608A1	RoHS	BGA217	3000	Built-in 1Gb LPDDR2 KGD with external clock source	MP
RK1608A2	RoHS	BGA217	3000	Built-in 1Gb LPDDR2 KGD with external crystal/clock source	MP
RK1608B	RoHS	BGA217	3000	Built-in 2Gb LPDDR2 KGD with external clock source	MP
RK1608B2	RoHS	BGA217	3000	Built-in 2Gb LPDDR2 KGD with external crystal/clock source	MP

2.2 Top Marking



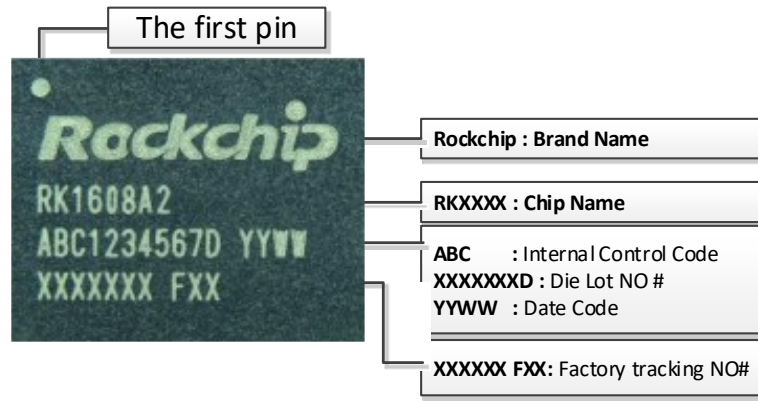


Fig 2-1 Top Markin

2.3 Dimension

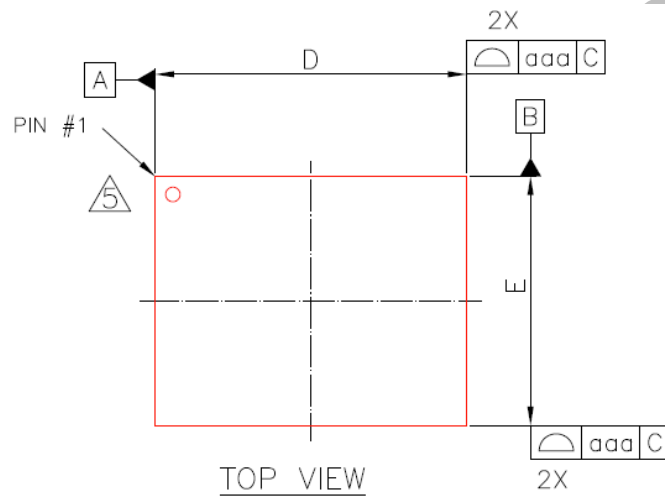


Fig 2-2 Package Top View

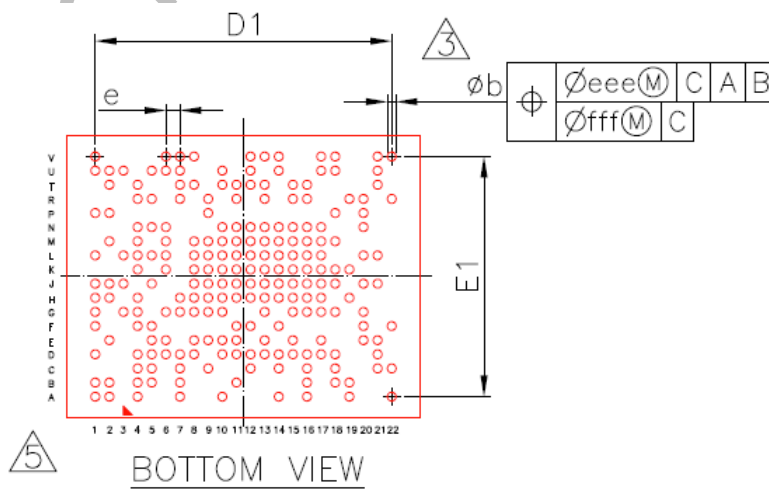


Fig 2-3 Package Bottom View

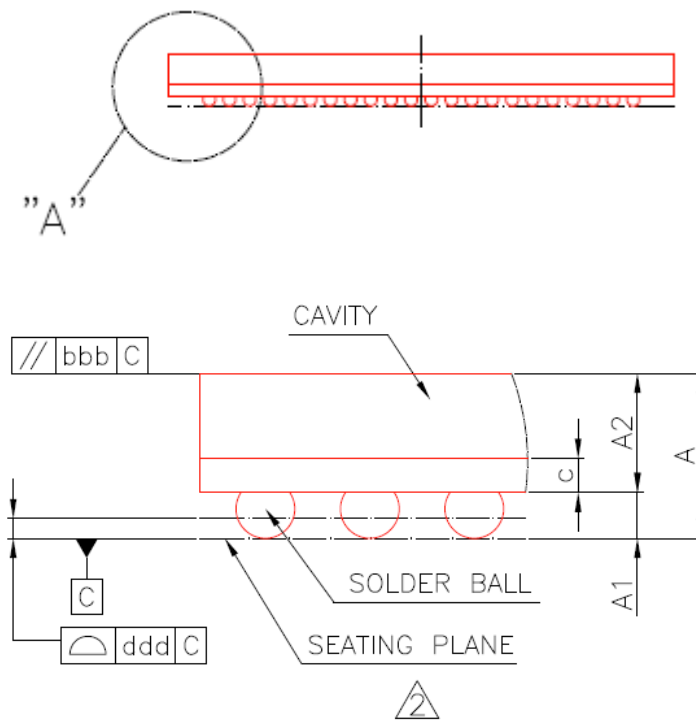


Fig 2-5 Package Side View

Table 2-2 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.97	1.04	1.10	0.038	0.041	0.043
A1	0.13	0.18	0.23	0.005	0.007	0.009
A2	0.81	0.86	0.91	0.032	0.034	0.036
c	0.22	0.26	0.30	0.009	0.010	0.012
D	9.90	10.00	10.10	0.390	0.394	0.398
E	7.90	8.00	8.10	0.311	0.315	0.319
D1	----	8.40	----	----	0.331	----
E1	----	6.80	----	----	0.268	----
e	----	0.40	----	----	0.016	----
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa		0.15			0.006	
bbb		0.15			0.006	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME	22/18					

2.4 Ball Map

Fig 2-4 Ball Mapping Diagram

21	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
7																							
A	NC_1	VSS_1	NP	MIPI_CSI_RX0_D0N	NP	NP	MIPI_CSI_RX0_AVDD_1V8	NP	NP	MIPI_CSI_RX3_AVDD_1V8	NP	NP	NP	MIPI_CSI_RX2_AVDD_1V8	NP	AVSS2_3	NP	NP	VSS_3	NP	NP	NC_2	
B	GPI00_A2/I2C1_SDA_M/JTAG_TDI	GPI00_A3/I2C1_SCL_M/JTAG_TMS	NP	MIPI_CSI_RX0_D0P	MIPI_CSI_RX0_D1P	NP	AVSS2_1	NP	NP	NP	NP	NP	NP	NP	NP	AVSS2_4	NP	VDDIO_3	CORE_VD_D_5	NP	NP	NP	
C	NP	NP	NP	VSS_2	MIPI_CSI_RX0_D1N	NP	MIPI_CSI_RX0_D2N	NP	MIPI_CSI_RX3_REXT	NP	NP	MIPI_CSI_RX3_D1N	NP	MIPI_CSI_RX2_D3P	NP	MIPI_CSI_RX2_CLKN	NP	MIPI_CSI_RX2_D0N	NP	NP	DDR_VD_D2_3	VSS_4	
D	CORE_VD_D_1	NP	NP	GPI00_A4/I2C0_SDA_M	GPI00_A0/I2C3_SDA_M/I2C2_SDA_S/JTAG_RTCK	MIPI_CSI_RX0_CLKN	MIPI_CSI_RX0_D2P	MIPI_CSI_RX0_D3N	NP	MIPI_CSI_RX3_D3P	MIPI_CSI_RX3_D2N	MIPI_CSI_RX3_D1P	MIPI_CSI_RX3_D0P	MIPI_CSI_RX2_D3N	MIPI_CSI_RX2_D2P	MIPI_CSI_RX2_CLKP	MIPI_CSI_RX2_D1P	MIPI_CSI_RX2_D0P	NP	NP	DDR_VD_D1_3	NP	
E	NP	VDDIO_1	NP	NP	GPI00_A1/I2C3_SCL_M/I2C2_SCL_S/JTAG_TDO	MIPI_CSI_RX0_CLKP	NP	MIPI_CSI_RX0_D3P	MIPI_CSI_RX0_REXT	MIPI_CSI_RX3_D3N	MIPI_CSI_RX3_D2P	NP	MIPI_CSI_RX3_D0N	NP	MIPI_CSI_RX2_D2N	NP	MIPI_CSI_RX2_D1N	NP	NP	NP	VSS_5	DDR_VD_DQ_1	NP
F	DDR_VD_DCA_3	NP	NP	DDR_VD_D2_1	GPI00_A5/I2C0_SCL_M	NP	NP	NP	NP	NP	MIPI_CSI_RX3_CLKP	MIPI_CSI_RX3_CLKN	NP	MIPI_CSI_RX2_REXT	NP	NP	NP	NP	NP	NP	DDR_VD_DQ_2	NP	VSS_6
G	VSS_7	NP	GPI00_B3/UART0_SIN/MCLK_OUT2/JTAG_TCK	GPI00_B4/UART0_SOUT/MCLK_OUT	NP	DDR_PZQ	VSS_8	VSS_9	VSS_10	VSS_11	NP	NP	VSS_12	NP	VSS_13	VSS_14	VSS_15	VSS_16	NP	VSS_17	NP	NP	
H	DDR_VD_DCA_4	CORE_VD_D_2	NP	DDR_CAVREF	NP	NP	VSS_18	VSS_19	VSS_20	VSS_21	VSS_22	VSS_23	VSS_24	VSS_25	VSS_26	VSS_27	VSS_28	NP	DDR_VD_DQ_3	NP	NP	NP	
J	CORE_VD_D_3	DDR_VD_DCA_1	DDRC_PZQ	NP	VSS_29	NP	NP	VSS_30	VSS_31	VSS_32	VSS_33	VSS_34	VSS_35	VSS_36	VSS_37	VSS_38	VSS_39	DDR_DQ_VREF	NP	DDR_VD_DQ_4	DDR_VD_DQ_5	NP	
K	NP	NP	NP	GPI01_B0/SPI0_RXD	NP	DDR_VD_DCA_2	NP	VSS_40	VSS_41	VSS_42	VSS_43	VSS_44	VSS_45	VSS_46	VSS_47	VSS_48	VSS_49	VSS_50	DDR_VD_DQ_6	NP	NP	NP	
L	VDDIO_2	NP	GPI01_B1/SPI0_CS0	GPI01_A7/SPI0_CLK	GPI01_A5/SLEEP_ST	VSS_51	NP	VSS_52	VSS_53	VSS_54	VSS_55	VSS_56	VSS_57	VSS_58	VSS_59	VSS_60	VSS_61	NP	NP	DDR_VD_DQ_8	DDR_VD_DQ_7	NP	
M	NP	DDR_VD_DCA_5	NP	GPI01_A6/SPI0_TXD	NP	GPI01_A4/IRQ_MONITOR	NP	VSS_62	VSS_63	VSS_64	VSS_65	VSS_66	VSS_67	VSS_68	VSS_69	VSS_70	VSS_71	VSS_72	NP	NP	NP	NP	
N	NP	NP	NP	GPI01_A3/TEST_CLKOUT	NPOR	GPI01_A2	NP	NP	NP	VSS_73	VSS_74	VSS_75	VSS_76	VSS_77	VSS_78	VSS_79	VSS_80	NP	NP	DDR_VD_DQ_9	NP	NP	
P	VSS_81	DDR_VD_D2_2	NP	NP	NP	NP	NP	NP	MIPI_CSI_TX1/RX1_CLKP	NP	NP	NP	NP	NP	NP	NP	NP	VSS_82	NP	DDR_VD_DQ_10	NP	NP	
R	NP	NP	NP	PVCCIO	PDVDD	NP	MIPI_CSI_TX1/RX1_D1P	NP	MIPI_CSI_TX1/RX1_CLKN	NP	MIPI_CSI_TX1/RX1_D3N	NP	MIPI_CSI_TX0_D3N	NP	MIPI_CSI_TX0_D2P	MIPI_CSI_TX0_CLKP	NP	NP	VDDIO_4	VSS_83	NP	VSS_84	
T	NP	VSS_85	NP	DDR_VD_D1_1	NP	NP	MIPI_CSI_TX1/RX1_D0P	MIPI_CSI_TX1/RX1_D1N	NP	MIPI_CSI_TX1/RX1_D2N	MIPI_CSI_TX1/RX1_D3P	MIPI_CSI_TX1/RX1_REXT	MIPI_CSI_TX0_D3P	NP	MIPI_CSI_TX0_D2N	MIPI_CSI_TX0_CLKN	NP	NP	NP	NP	NP	DDR_VD_D1_2	NP
U	VSS_86	XIN24M/MCLK_IN	XOUT24M/MCLK_SEL	NP	AVSS1_2	PLL_AVDD_1V0	MIPI_CSI_TX1/RX1_D0N	NP	NP	MIPI_CSI_TX1/RX1_D2P	NP	MIPI_CSI_TX0_REXT	NP	AVSS1_5	NP	NP	MIPI_CSI_TX0_D1N	MIPI_CSI_TX0_D0P	NP	NP	VSS_87	NP	
V	OSC_VSS	NP	NP	NP	NP	PLL_AVDD_1V8	MIPI_CSI_TX1/RX1_AVDD_1V8	AVSS1_3	NP	NP	NP	AVSS1_4	MIPI_CSI_TX0_AVDD_1V8	AVSS1_1	NP	NP	MIPI_CSI_TX0_D1P	MIPI_CSI_TX0_D0N	NP	NP	CORE_VD_D_4	NC_3	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Notes: (Difference from Netlist.xlsx)
 ● "MIPI_" here is same as "MIPI_CSI_" in Netlist.xlsx;

2.5 Ball Pin Number Order

Table 2-3 Ball Pin Number Order Information

Pin Number	Pin Name
D5	GPIO0_A0/I2C3_SDA_M/I2C2_SDA_S/JTAG_RTCK
E5	GPIO0_A1/I2C3_SCL_M/I2C2_SCL_S/JTAG_TDO
B1	GPIO0_A2/I2C1_SDA_M/JTAG_TDI
B2	GPIO0_A3/I2C1_SCL_M/JTAG_TMS
D4	GPIO0_A4/I2C0_SDA_M
F5	GPIO0_A5/I2C0_SCL_M
G3	GPIO0_B3/UART0_SIN/MCLK_OUT2/JTAG_TCK
G4	GPIO0_B4/UART0_SOUT/MCLK_OUT3
N6	GPIO1_A2
N4	GPIO1_A3/TEST_CLKOUT
M6	GPIO1_A4/IRQ_MONITOR
L5	GPIO1_A5/SLEEP_ST
M4	GPIO1_A6/SPI0_TXD
L4	GPIO1_A7/SPI0_CLK
K4	GPIO1_B0/SPI0_RXD
L3	GPIO1_B1/SPI0_CS0

RK1608B and RK1608B2 support different clock source as below:

Pin Number	RK1608B2 /RK1608A2	RK1608B/ RK1608A1	Description
U3	XOUT24M	MCLK_SEL	Set MCLK_SEL to be low for RK1608B.
U2	XIN24M	MCLK_IN	Clock for MCLK_IN need to be between 16MHz and 27MHz.

2.6 Power/ground IO descriptions

Table 2-5 Power/Ground IO information

Group	Ball #	Descriptions
VSS	A2 A16 A19 B7 B11 B16 C4 C22 E20 F22 G1 G7 G8 G9 G10 G13 G15 G16 G17 G18 G20 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 J5 J8 J9 J10 J11 J12 J13 J14 J15 J16 J17 K8 K9 K10 K11 K12 K13 K14 K15 K16 K17 K18 L6 L8 L9 L10 L11 L12 L13 L14 L15 L16 L17 M8 M9 M10 M11 M12 M13 M14 M15 M16 M17 M18 N10 N11 N12 N13 N14 N15 N16 N17 P1 P18 R20 R22 T2 U1 U5 U14 U21 V1 V8 V12 V14	Internal Logic Ground and Digital IO Ground
MIPI_CSI_RX0_AVDD_1V8	A7	MIPI RX0 PHY 1.8V Power Supply
MIPI_CSI_RX3_AVDD_1V8	A10	MIPI RX3 PHY 1.8V Power Supply
MIPI_CSI_RX2_AVDD_1V8	A14	MIPI RX2 PHY 1.8V Power Supply
MIPI_CSI_TX1/RX1_AVDD_1V8	V7	MIPI TX1/RX1 PHY 1.8V Power Supply
MIPI_CSI_TX0_AVDD_1V8	V13	MIPI TX0 PHY 1.8V Power Supply
PLL_AVDD_1V0	U6	PLL Analog Power Supply
PLL_AVDD_1V8	V6	PLL Analog Power Supply
DDR_VDD	C21 D21 E21 F1 F4 F20 H1 H19 J2 J20 J21 K6 K19 L20 L21 M2 N20 P2 P20 T4 T21	LPDDR2/3 Digital IO Power Supply
VDDIO	B18 E2 L1 R19	Digital IO Power Supply
PVCCIO	R4	Digital IO in PMU domain Power Supply
PDVDD	R5	Digital Power Supply for PMU Domain
CORE_VDD	B19 D1 V21 H2 J1	Core digital power supply for DSP

2.7 Function IO description

Table 2-6 Function IO description

Func 1	Func 2	Func 3	Func 4	Pin name	Type	Def	PD/PU	Def	INT	Power Domain
				XIN24M						PLL_1V0
				XOUT24M						PLL_1V0
				NPOR			up			PVCCIO
				MCLK_SEL			up			PVCCIO
				MCLK_IN			down			PVCCIO
pmu_gpio1a2				GPIO1_A2	I/O	I	down	4mA	✓	PVCCIO
pmu_gpio1a3	test_clkout			GPIO1_A3/TEST_CLKOUT	I/O	I	up	4mA	✓	PVCCIO
pmu_gpio1a4	irq_monitor			GPIO1_A4/IRQ_MONITOR	I/O	I	up	4mA	✓	PVCCIO
pmu_gpio1a5	sleep_st			GPIO1_A5/SLEEP_ST	I/O	I	down	4mA	✓	PVCCIO
pmu_gpio1a6	spi0_txd			GPIO1_A6/SPI0_TXD	I/O	I	down	4mA	✓	PVCCIO
pmu_gpio1a7	spi0_clk			GPIO1_A7/SPI0_CLK	I/O	I	down	4mA	✓	PVCCIO
pmu_gpio1b0	spi0_rxd			GPIO1_B0/SPI0_RXD	I/O	I	down	4mA	✓	PVCCIO
pmu_gpio1b1	spi0_cs0			GPIO1_B1/SPI0_CS0	I/O	I	up	4mA	✓	PVCCIO
top_gpio0a0	i2c3_sda_m	i2c2_sda_s	jtag_rtck	GPIO0_A0/I2C3_SDA_M/I2C2_SDA_S/JTAG_RTCK	I/O	I	up	4mA	✓	VDDIO
top_gpio0a1	i2c3_scl_m	i2c2_scl_s	jtag_tdo	GPIO0_A1/I2C3_SCL_M/I2C2_SCL_S/JTAG_TDO	I/O	I	up	4mA	✓	VDDIO
top_gpio0a2	i2c1_sda_m		jtag_tdi	GPIO0_A2/I2C1_SDA_M/JTAG_TDI	I/O	I	up	4mA	✓	VDDIO
top_gpio0a3	i2c1_scl_m		jtag_tms	GPIO0_A3/I2C1_SCL_M/JTAG_TMS	I/O	I	up	4mA	✓	VDDIO
top_gpio0a4	i2c0_sda_m			GPIO0_A4/I2C0_SDA_M	I/O	I	up	4mA	✓	VDDIO
top_gpio0a5	i2c0_scl_m			GPIO0_A5/I2C0_SCL_M	I/O	I	up	4mA	✓	VDDIO
top_gpio0b3	uart0_sin	mclk_out2	jtag_tck	GPIO0_B3/UART0_SIN/MCLK_OUT2/JTAG_TCK	I/O	I	down	4mA	✓	VDDIO
top_gpio0b4	uart0_sout	mclk_out3		GPIO0_B4/UART0_SOUT/MCLK_OUT3	I/O	I	up	4mA	✓	VDDIO

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,

AP = Analog Power , AG = Analog Ground

DP = Digital Power , DG = Digital Ground

A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

③: Reset state: I = input without any pull resistor O = output

④: It is die location. For examples, "Left side" means that all the related IOs are always in left side of die

⑤: Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring

⑥: The pull up/pull down is configurable.

2.8 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	MCLK_IN	I	Clock input (16MHz ~ 27MHz)
	MCLK_SEL	I	Choose clock resource from crystal or external clock
	SLEEP_ST	O	Notify signal to indicate RK1608 Series is ready to sleep, then clock to RK1608 Series can be stop

Interface	Pin Name	Direction	Description
	IRQ_MONITOR	O	Internal interrupts in RK1608 Series are dump to AP
	TEST_CLKOUT	O	Test pin to dump RK1608 Series internal clock

Interface	Pin Name	Direction	Description
JTAG	jtag_rtck	O	JTAG return test clock (tck synchronized to ceva_free_clk)
	jtag_tck	I	JTAG interface clock input/SWD interface clock input
	jtag_tdi	I	JTAG interface TDI input
	jtag_tms	I	JTAG interface TMS input/SWD interface data out
	jtag_tdo	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
SPI Controller	spix_clk(x=0)	I/O	spi serial clock
	spix_csny (x=0)(y=0,1)	I/O	spi chip select signal, low active
	spix_txd(x=0)	O	spi serial data output
	spix_rxd(x=0)	I	spi serial data input

Interface	Pin Name	Direction	Description
I2C	i2cx_sda_m (x=0,1,3)	I/O	I2C data of master controller x (x=0,1,3)
	i2cx_scl_m (x=0,1,3)	I/O	I2C clock of master controller x (x=0,1,3)
	I2C2_SDA_S	I/O	I2C data of slave controller
	I2C2_SCL_S	I/O	I2C clock of slave controller

Interface	Pin Name	Direction	Description
UART	UART0_SIN	I	UART serial data input
	UART0_SOUT	O	UART serial data output

Interface	Pin Name	Direction	Description
MIPI CSI-2 RX	MIPI_CSI_RXi_DiN (i=0,2,3, j=0~3)	I/O	MIPI RX negative differential data line transceiver output
	MIPI_CSI_RXi_DiP (i=0,2,3, j=0~3)	I/O	MIPI RX positive differential data line transceiver output
	MIPI_CSI_RXi_CLKP (i=0,2,3)	I/O	MIPI RX positive differential clock line transceiver output
	MIPI_CSI_RXi_CLKN (i=0,2,3)	I/O	MIPI RX negative differential clock line transceiver output
	MIPI_CSI_RXi_REXT (i=0,2,3)	I/O	MIPI RX external resistor connection

Interface	Pin Name	Direction	Description
MIPI CSI-2 TX0	MIPI_CSI_TX0_DiN(i=0~3)	I/O	MIPI TX0 negative differential data line transceiver output
	MIPI_CSI_TX0_DiP(i=0~3)	I/O	MIPI TX0 positive differential data line transceiver output
	MIPI_CSI_TX0_CLKP	I/O	MIPI TX0 positive differential clock line transceiver output
	MIPI_CSI_TX0_CLKN	I/O	MIPI TX0 negative differential clock line transceiver output
	MIPI_CSI_TX0_REXT	I/O	MIPI TX0 external resistor connection

Interface	Pin Name	Direction	Description
MIPI CSI-2 TX1/RX1	MIPI_CSI_TX1/RX1_DiN(i=0~3)	I/O	MIPI TX1/RX1 negative differential data line transceiver output
	MIPI_CSI_TX1/RX1_DiP(i=0~3)	I/O	MIPI TX1/RX1 positive differential data line transceiver output
	MIPI_CSI_TX1/RX1_CLKP	I/O	MIPI TX1/RX1 positive differential clock line transceiver output
	MIPI_CSI_TX1/RX1_CLKN	I/O	MIPI TX1/RX1 negative differential clock line transceiver output
	MIPI_CSI_TX1/RX1_REXT	I/O	MIPI TX1/RX1 external resistor connection

2.9 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 IO Type List

Type	Diagram	Description	Pin Name
A		Crystal Oscillator with high enable	XIN24M/XOUT24M
B		Tri-state output pad with input, which pullup/pulldown, slew rate and drive strength is configurable	Part of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Absolute minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute minimum ratings conditions may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameters	Related Power Group	Min	Max	Unit
DC supply voltage for Internal digital logic	CORE_VDD, PDVDD,	-0.4	1.30	V
DC supply voltage for Digital GPIO (DDR, MIPI PHY)	PVCCIO VDDIO	-0.4	2.18	V
DC supply voltage for DDR IO	DDR_VDD	-0.4	1.81	V
DC supply voltage for Analog part of PLL	PLL_AVDD_1V0	-0.4	1.21	V
DC supply voltage for Analog part of MIPI PHY	MIPI_TX/RX_AVDD_1V8 MIPI_TX_AVDD_1V8 MIPI_RX_AVDD_1V8	-0.4	2.18	V
Digital input voltage for input buffer of GPIO		-0.4	2.18	V
Digital output voltage for output buffer of GPIO		-0.4	2.18	V
Storage Temperature	Tstg	-40	125	°C
Max Conjunction Temperature	Tj	N/A	125	°C

3.2 Recommended Operating Conditions

This section describes the recommended operating condition for every clock domain.

Table 3-2 Recommended operating conditions

Parameters	Symbol	Min	Typ.	Max	Units
Internal digital logic Power	CORE_VDD, PDVDD	0.95	1.1	1.2	V
Digital GPIO Power(1.8V)	PVCCIO VDDIO	1.62	1.8	1.98	V
DDR IO (LPDDR2 mode) Power	DDR0_VDD	1.08	1.2	1.32	V
DDR reference supply (VREF) Input	VREF	0.49* DDR_VDD	0.5* DDR_VDD	0.51*DDR_VDD	V
DDR External termination voltage		VREF- 40mV	VREF	VREF+ 40mV	V
LPDDR2 power supply	VDD1 VDD2 VDDCA VDDQ	1.70 1.14 1.14 1.14	1.8 1.2 1.2 1.2	1.95 1.30 1.30 1.30	V
PLL Analog Power	PLL_AVDD_1V0	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD_1V8	1.62	1.8	1.98	V
MIPI PHY Analog Power	MIPI_TXRX_AVDD_1V8 MIPI_TX_AVDD_1V8 MIPI_RX_AVDD_1V8	1.62	1.8	1.98	V
PLL input clock frequency		16	24	27	MHz
Max DSP frequency			600	TBD	MHz
Ambient Operating Temperature \varnothing	Ta	-10	25	80	°C

Notes:

- ① Symbol name is same as the pin name in the io descriptions
- ② with the reference software setup, the reference software will limit the chipset temperature about 80 °C

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ.	Max	Units
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDIO	V
	Input High Voltage	Vih	0.65*VDDIO	NA	VDDIO+0.3	V
MIPI PHY	Input signal voltage range	Vi	-50	NA	1350	mV
	Input leakage current	Ileak	-10	NA	10	uA
	Ground	Vgndsh	-50	NA	50	mV
	Maximum transient output voltage level	Voh(absmax)	-0.15	NA	1.45	V
	Maximum transient time above Voh(absmax)	tVoh(absmax)	NA	NA	20	ns
	HS transmit differential output voltage magnitude	Vod	140	200	270	mV
	Change in differential output voltage magnitude between logic states	Δ Vod	NA	NA	14	mV
	Steady-state common-mode output voltage	Vcmtx	150	200	250	mV
	Change in steady-state common-mode output voltage between logic states	ΔVcmtx(1,0)	NA	NA	5	mV
	HS output high voltage	Vohhs	NA	NA	360	mV
	Single-ended output impedance	Zos	40	50	62.5	Ω
	Single-ended output impedance mismatch	ΔZos	NA	NA	10	Ω
	Output low-level SE output	Vol	-50	NA	50	mV
	Output high-level SE output	Voh	1.1	1.2	1.3	V
	Single-ended output impedance	Zolp	110	NA	NA	Ω
	Single-ended output impedance mismatch driving opposite level	ΔZolp(01,10)	NA	NA	20	%
	Single-ended output impedance mismatch driving same level	ΔZolp(00,11)	NA	NA	5	%
	Differential input high volvtage threshold	Vidth	NA	NA	70	mV
	Differential input low volvtage threshold	Vidtl	-70	NA	NA	mV
	Single ended input high voltage	Vihhs	NA	NA	460	mV
	Single ended input low voltage	Vilhs	-40	NA	NA	mV
	Input common mode voltage	Vcmrxdc	70	NA	330	mV
	Differential input impedance	Zid	80	NA	125	Ω
	Input low voltage	Vil	NA	NA	550	mV
	Input high voltage	Vih	880	NA	NA	mV
	Input hysteresis	Vhyst	25	NA	NA	mV
	Input low fault threshold	Vilf	NA	NA	200	mV
	Input high fault threshold	Vihf	450	NA	NA	mV

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ.	Max	Units
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ.	Max	Units
PLL	Divided reference frequency range	Fin		0.269	NA	2200	MHz
	output frequency range	Fout		0.440	N/A	2200	MHz
	Lock time	Tlt		N/A	NA	500	Cycles of divided reference clock
	Power consumption (normal mode)	N/A		N/A	3	N/A	mW
	Period jitter (P-P)	N/A		N/A	NA	+/-2.5	%
	Junction temperature	N/A			70	125	°C

3.6 Input Clock Requirements

Parameters	Info	Min	Typ.	Max	Units
External MCLK level	RK1608B/RK1608A1	1.62	1.8	1.98	V
	RK1608B2/RK1608A2 (compatible)	TBD	1.0	TBD	V
External MCLK frequency range		16	24	27	MHz
Frequency accuracy requirement		-10	-	10	ppm
duty cycle requirement			50		%
Phase noise requirement	Offset ≥ 1MHz			-120	dBc/Hz
Jitter requirement	MCLK ≥ 8MHz			500	ps

The package RK1608B2&RK1608A2 (with external OSC) has been verified to compatible with RK1608B &RK1608A1(with external MCLK), but the MCLK should satisfy the property list in the upper table

3.7 Electrical Characteristics for MIPI PHY

Table 3-6 Electrical Characteristics for MIPI PHY

Parameters	Symbol	Test condition	Min	Type	Max	Units
HS Transmitter AC specifications						
Common-mode variations above 450 MHz	$\Delta V_{CMTX}(HF)$	$80\Omega \leq RL \leq 125\Omega$	NA	NA	15	mVrms
Common-mode variations between 50MHz - 450MHz	$\Delta V_{CMTX}(LF)$	$80\Omega \leq RL \leq 125\Omega$	NA	NA	25	mVp
Differential output signal rise time	tr	20% to 80%, $RL=50\Omega$	100	NA	NA	ps
Differential output signal fall time	tf	20% to 80%, $RL=50\Omega$	100	NA	NA	ps
LS Transmitter AC specifications						
Single ended output rise/fall time	trlp, tflp	15% to 85%, $CL < 70pF$	NA	NA	25	ns
	treop	30% to 85%, $CL < 70pF$	NA	NA	35	ns
Signal slew rate		15% to 85%, $CL < 70pF$	NA	NA	150	mV/ns
Load capacitance	CL		0	NA	70	pF
HS Receiver AC specifications						
Common mode interference beyond 450MHz	$\Delta V_{CMRX}(HF)$		NA	NA	200	mVpp
Common mode interference between 50MHz and 450MHz	$\Delta V_{CMRX}(LF)$		-50	NA	50	mVpp
Common-mode termination amplitude	CCM		NA	NA	60	pF
LP Receiver AC Specifications						
Input pulse rejection	eSPIKE		NA	NA	300	V.ps
Minimum pulse response	TMIN		20	NA	NA	ns
Pk-to-Pk interference voltage	VINT		NA	NA	400	mVpp
interference frequency	fINT		450	NA	NA	MHz

3.8 Recommended Power Sequence

1. Power up/down timing:

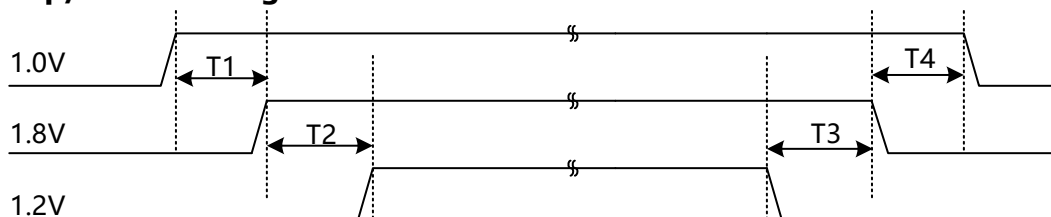


Fig 3-1 power sequence

$T1 \geq 0, T2 \geq 0, T3 \geq 0, T4 \geq 0$

2. SPI timing after power up

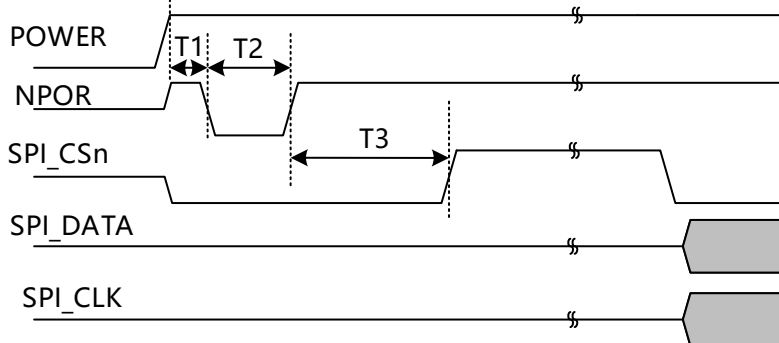


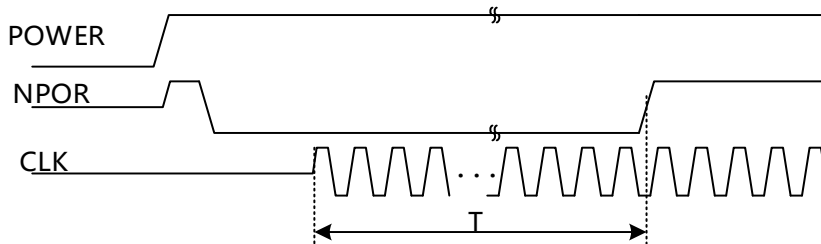
Fig 3-2 SPI timing after power up

$T1 > 0$, $T2 \geq 1\text{ms}$, $T3 \geq 3\text{ms}$

After power up, SPI is in master mode by default, if the system need SPI to enter slave mode, then the following step is expected.

- 1) AP sets SPI IO to GPIO mode
- 2) RK1608 power up
- 3) AP sets to make SPI_CS_n low, and after T₀, asserts NPOR, wait for T₁, then de-assert NPOR
- 4) After NPOR de-asserted, wait for T₂, then make SPI_CS_n high
- 5) AP release the control of SPI_CS_n, and sets SPI IO to SPI mode

3. Clock and reset



$T \geq 64$ clock cycles

3.9 SPI0 Timing Diagram

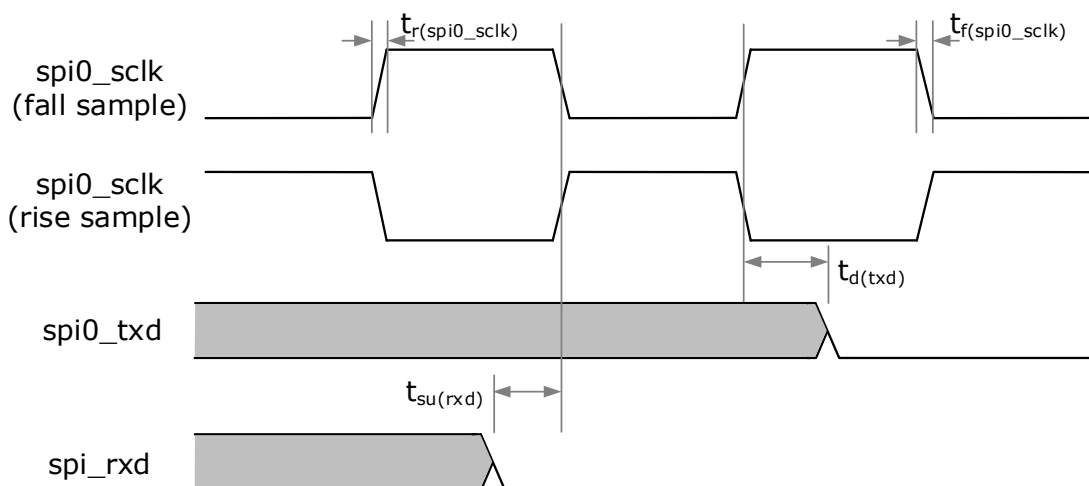


Fig 3-3 SPI controller timing diagram in master mode

Table 3-7 Timing parameter description-1

Parameter		Min.	Typ.	Max.	Unit
$t_{r(spi0_sclk)}$	rise time for spi0_sclk	-	-	3.8	ns
$t_{f(spi0_sclk)}$	fall time for spi0_sclk	-	-	2.9	ns
$t_{d(tx)}$	Spi0_txd propagation delay from spi0_sclk drive edge	-	-	1.2	ns
$t_{su(rx)}$	Spi0_rxd setup time to spi0_sclk sample edge	-	-	-	ns

*timing condition: $V_{CCIO}=1.8V, C_{LOAD} \leq 10pF$, drive strength 6mA

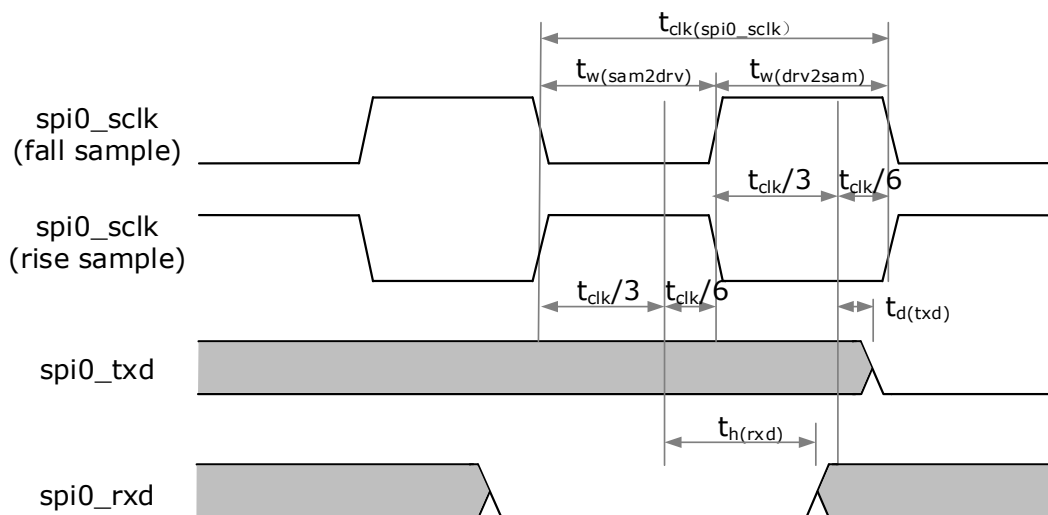


Fig 3-4 SPI controller timing diagram in slave mode

Table 3-8 Timing parameter description-2

Parameter		Min.	Typ.	Max.	Unit
$t_{clk(spi0_clk)}$	Spi0_sclk cycle time	20	-	-	ns
$t_{w(sam2drv)}$	Spi0_sclk pulse width from sample edge to drive edge	9.9	-	-	ns
$t_{w(drv2sam)}$	Spi0_sclk pulse width from drive edge to sample edge	10.1	-	-	ns
$t_{d(tx)}$	Spi0_txd propagation delay from $t_{clk}/3$ after spi0_sclk drive edge	-2	-	-	ns
$t_{h(rx)}$	Spi0_rxd hold time from $t_{clk}/3$ after spi0_sclk sample edge	-	-	-	ns
$f_{maxclk(spix_clk)}$	Spi0_sclk maximum clock frequency based on ideal peripheral	-	-	50	MHz

*timing condition: $V_{CCIO}=1.8V, C_{LOAD} \leq 10pF$, drive strength 6mA

3.10 I²C Timing Diagram

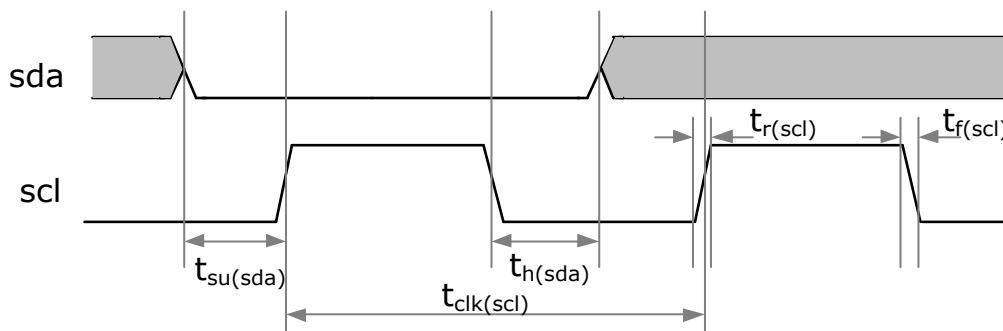


Fig 3-5 I²C timing diagram

Table 3-9 I²C timing parameters

Parameter	Min.	Typ.	Max.	Unit
100KHz mode				
t _{clk(scl)}	-	10	-	us
t _{r(scl)}	-	3.9	-	ns
t _{f(scl)}	-	2.9	-	ns
t _{h(sda)}	-	2.5	-	us
t _{su(sda)}	-	2.5	-	us
400KHz mode				
t _{clk(scl)}	-	2.5	-	us
t _{r(scl)}	-	3.9	-	ns
t _{f(scl)}	-	2.9	-	ns
t _{h(sda)}	-	0.6	-	us
t _{su(sda)}	-	0.6	-	us
1MHz mode				
t _{clk(scl)}	-	1.0	-	us
t _{r(scl)}	-	3.9	-	ns
t _{f(scl)}	-	2.9	-	ns
t _{h(sda)}	-	0.25	-	us
t _{su(sda)}	-	0.25	-	us

*timing condition: V_{CCIO}=1.8V, C_{LOAD}≤10pF, drive strength 6mA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125°C.

4.2 Package Thermal Characteristics

This section provides the thermal resistance characteristics for the package used on RK1608B. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Package (BGA)	Power(W)	θ_{JA} ($^{\circ}C/W$)	θ_{JB} ($^{\circ}C/W$)	θ_{JC} ($^{\circ}C/W$)
RK1608B①	2.0	25.2	11.1	6.6
RK1608A1	2.0	TBD	TBD	TBD
RK1608A2	2.0	TBD	TBD	TBD

Note:

- ① The testing PCB is based on 6 layers, 80x140 mm, 1 mm Thickness, ambient temperature is 25°C.

Chapter 5 Power Consumption

5.1 Overview

Here we place the issues should be pay more attention to during the new hardware design and product developing progress. This chapter will be make up along the mass production. Developers should read this chapter carefully.

5.2 Details

Power consumption of digital logic(VDD_CORE) depending on both frequency and the real algorithm it's running. The peak current would reach 2.5A with a purposely designed case which would hardly appear in the normal algorithms, typical algorithms implemented for now consumes no more than 1.0A. It means that the CF (crest factor) of VDD_CORE may be high when the algorithm is running.

For stability, we recommend using a 3A DC/DC converter and it should have good transient load response parameters. LDO is not recommended.

If full performance is not required, lower current rating design is also acceptable.

Parameters	Test condition	Min	Typ	Max	Units
VDD_CORE Current	VDD_CORE=1.1V DSP Freq=600M (Dual-core) DDR Freq=528M ①	-	-	2.5	A
PDVDD Current	-	-	16	50	mA
AVDD_10_PLL Current	-	-	1.6	10	mA
AVDD_18_PLL Current	-	-	5.5	10	mA
MIPI_AVDD Current	MIPI_TX1/RX1_AVDD_1V8 MIPI_TX0_AVDD_1V8 MIPI_RX0_AVDD_1V8 MIPI_RX2_AVDD_1V8 MIPI_RX3_AVDD_1V8 Total current	-	20 ②	50	mA
DDR_VDD 1V8 Current	DDR_VDD1	-	2	15	mA
DDR_VDD 1V2 Current	DDR_VDD2 DDR_VDDCA DDR_VDDQ Total current	-	-	500	mA

Notes:

- ① Due to different leakage and test temperature, there is about $\pm 10\%$ error.
- ② 4-ways D-PHY in use.